CS 2204, Final Exam Instructions, **Digital Logic**
Fall 2021 NYU ECE
Time: Thursday December 16th 2021, 3:30 PM – 5:30PM.

- *Maximum time:* 120 minutes : **3:30 PM - 5:30 PM** [+ 10 min to assemble PDF and upload]
- *Open Book, Open Notes,*
- *Calculators allowed.*
- *The Final will be visible as an assignment on NYU Brightspace at 3:30 PM on Thursday December 16th 2021*
- *You Must show your work in steps – to get any credit*

Instructor/CAs available online if you have questions on the Final, during the Final – Please enter question in Zoom chat box at any time during Final

You **may not communicate with anyone** during the Final except with Course Staff

By University rules, **students are required to open Zoom and turn on their video and audio**.

If you are a student approved by MOSES, your portal will remain open until 6:45 PM instead of the 5:45 PM deadline to upload your PDF

This Test has **3 problems**. Please attempt all of them. Please show **all work**. Please write **legibly**

1. Please be sure to have 5-10 sheets of white or ruled Paper, a Pen/Pencil & Eraser
2. Please write down your solutions on 8.5 x 11 sheets of white paper, single-sided with your name printed in top right corner of each sheet and with Page Number and Problem number identified clearly on each sheet
3. **Please stop working on your Quiz at 5:30 PM** (6:30 PM for MOSES students) – you have 10 minutes to scan/take pictures of each sheet and upload them as completed PDF assignment to NYU Classes **by 5:40 PM** (6:40 PM for MOSES students)– you may use any of several smartphone apps to integrate your scans/pictures of sheets into a PDF file.
4. Please take pictures of each sheet and **upload** the PDF of all sheets after checking you have all sheets in the right order **by 5:45 PM latest (6:45 PM for MOSES Students).**
5. You may use iPAD to write down your solutions directly rather than on paper
6. Portal **will close at 5:45 PM** (6:45 PM for MOSES Students) not allowing upload of your quiz after 5:45 PM (6:45 PM for MOSES students)

1a. Assume the following 3 pairs of input operands are *unsigned 6-bit numbers*.

(i) What is the range of representation of these operands?

(ii) Does overflow occur when they are added?

(iii) What is their sum if there is no overflow?

001101 + 11010

010000 + 10101

100010 + 01101

1b. Assume the above 3 pairs of input operands are 6-bit long 2s complement representations.

(i) What is the range of representation of these operands?

(ii) Does overflow occur when they are added?

(iii) What is their sum if there is no overflow?

1c Implement the logic function f using only 2-input NAND gates

(i) f = w'y'+ xyz + wyz'+ x'y'z

(ii) f = b'd'e' + ace + c'e'+ bcde

(iii) f' = (w' + x)(y + z)(w' + y)(x + y' + z)

1d.For the following functions,

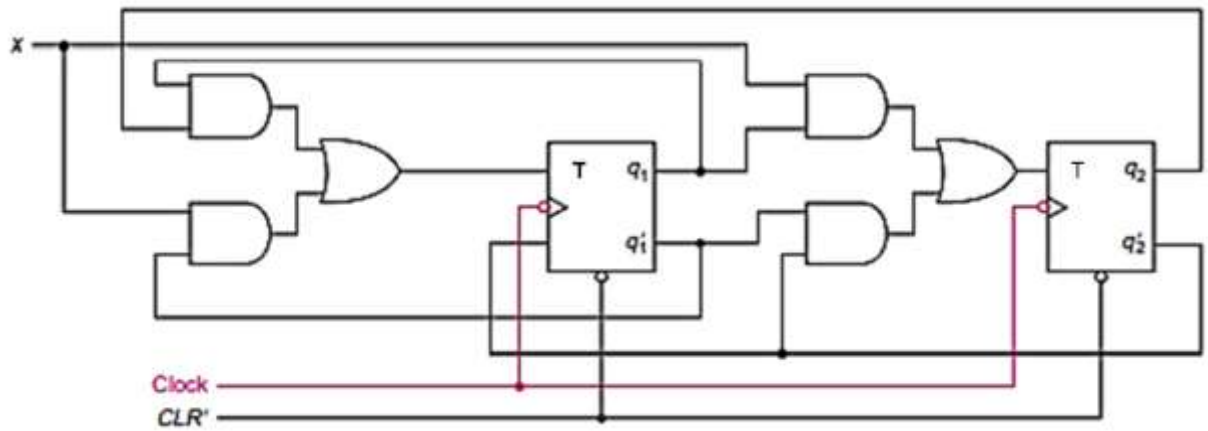
(i) List all prime implicants, indicating which are essential by first identifying minterms that cannot be covered by more than 1 prime implicant.

(ii) Show at least one of the minimum sum of products expression(s).

a. G(A, B, C, D) = Σm(0, 1, 4, 5, 7, 8, 10, 13, 14, 15)

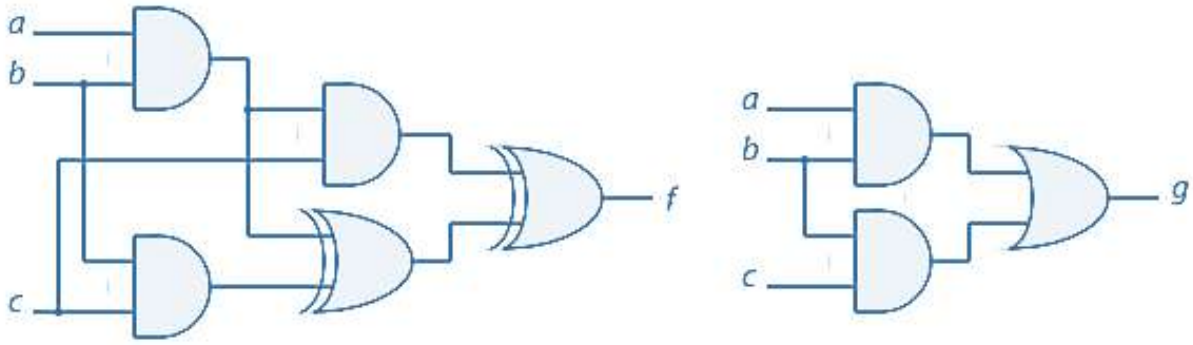
b. f (w, x, y, z) = Σm(2, 3, 4, 5, 6, 7, 9, 10, 11, 13)

2 (i). For the following Circuit of an FSM, ignore the CLR input. Find a state diagram and a state table.



(ii) Assume that the flip flops are each initially in state 0 (and there is no CLR), complete the timing trace for the states of the flip flops as far as possible. x 101110

3 (i). Consider the two circuits shown below. Do they implement the same function? *Support your response with algebraic manipulations or truth tables or a K-map*



3 (ii) Consider the function f(a, b, c, d) implemented in the schematic shown below. *Re-design the circuit in using two-input NAND gates only*