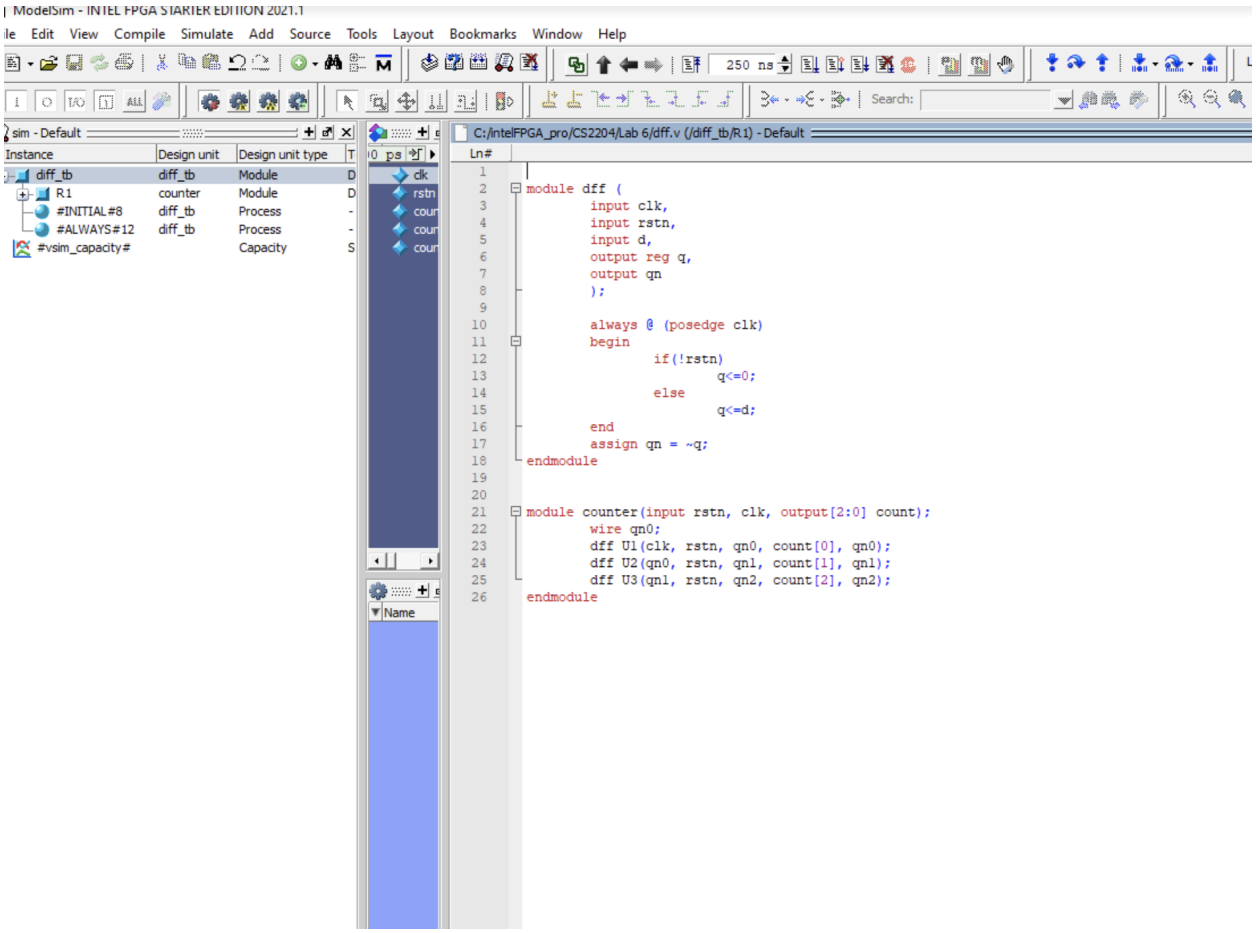
Lab 6

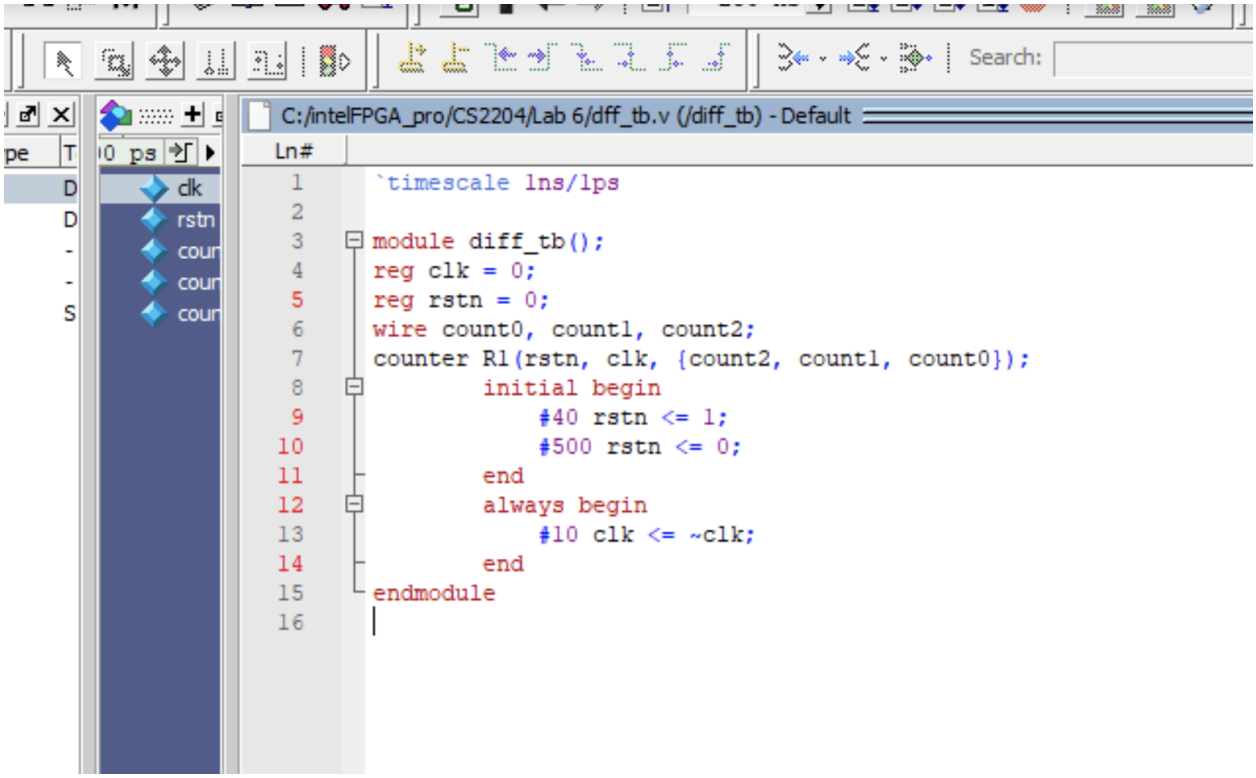
1) Write the Verilog module that modifies the given D Flip-Flop module by adding a complementary output Qn.
2) Use this modified D Flip-Flop module to implement a schematic of a 3-bit ripple counter that loops back to ‘000’
3) Write the Verilog Testbench that sweeps through enough Clock input pulses and show waveforms that verify the 3 bit ripple counter is operating correctly.

First, I will discuss my code and then my waveform. My code had 3 modules.

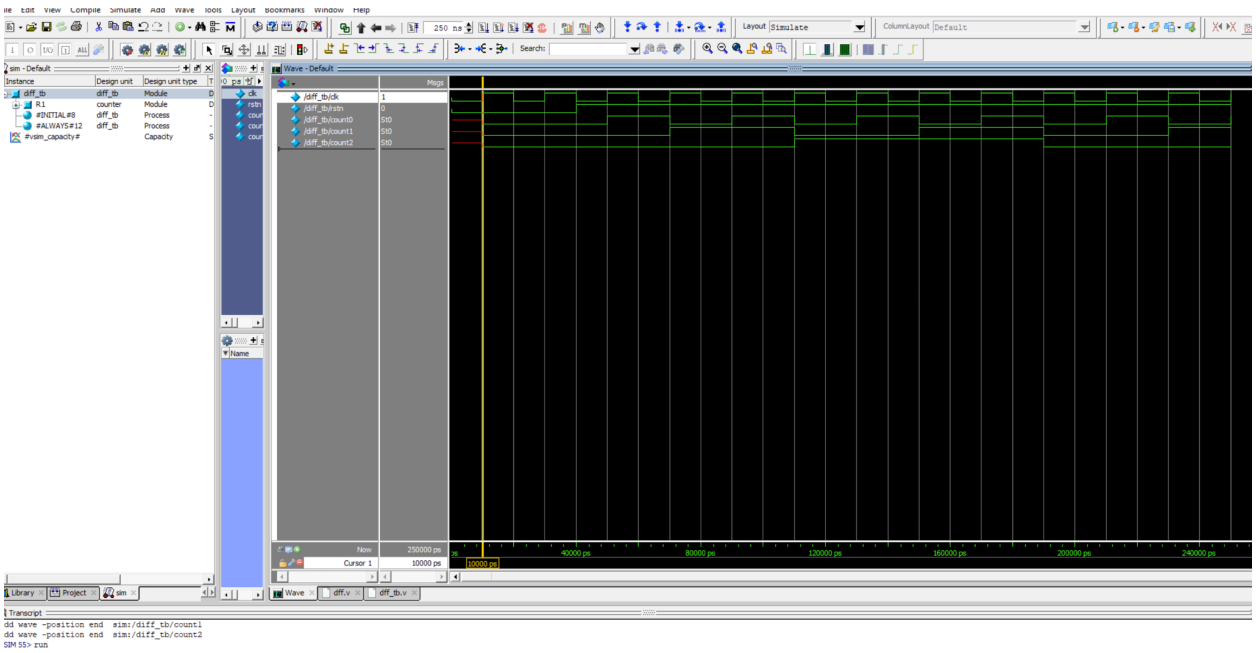


The above code shows the dff module and the counter module. The counter module is code that translates how the wires are connected. To understand this better, I drew a graph of how the wires are connected.

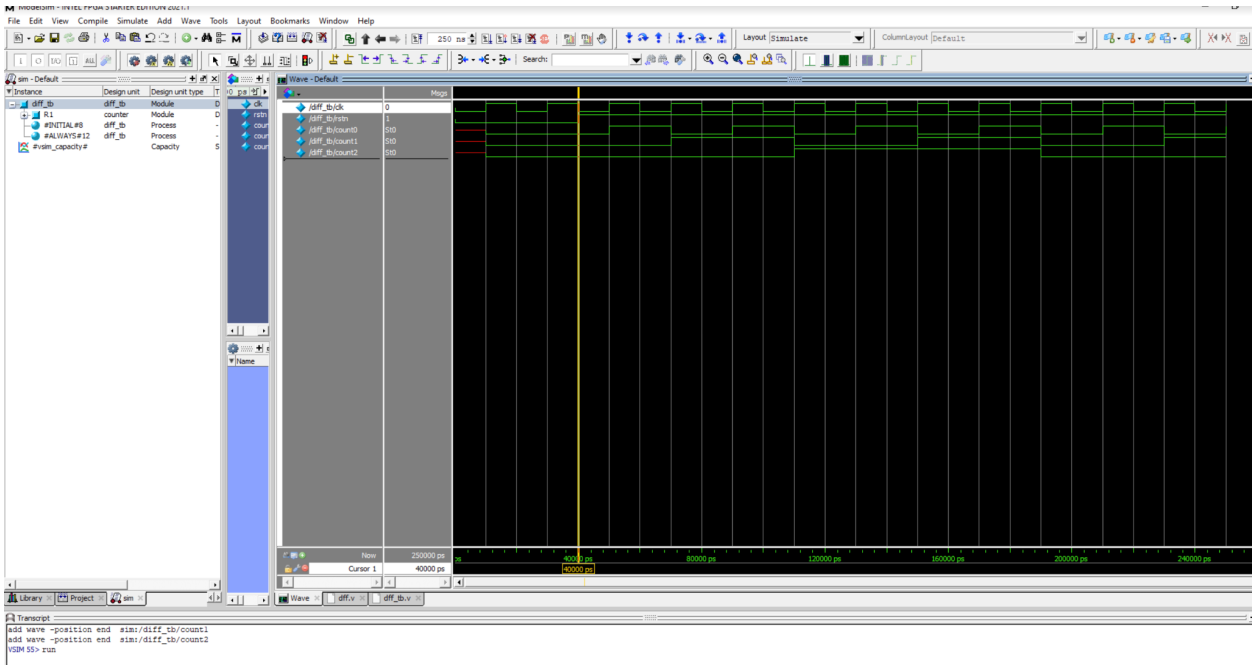
This is my testbench code.



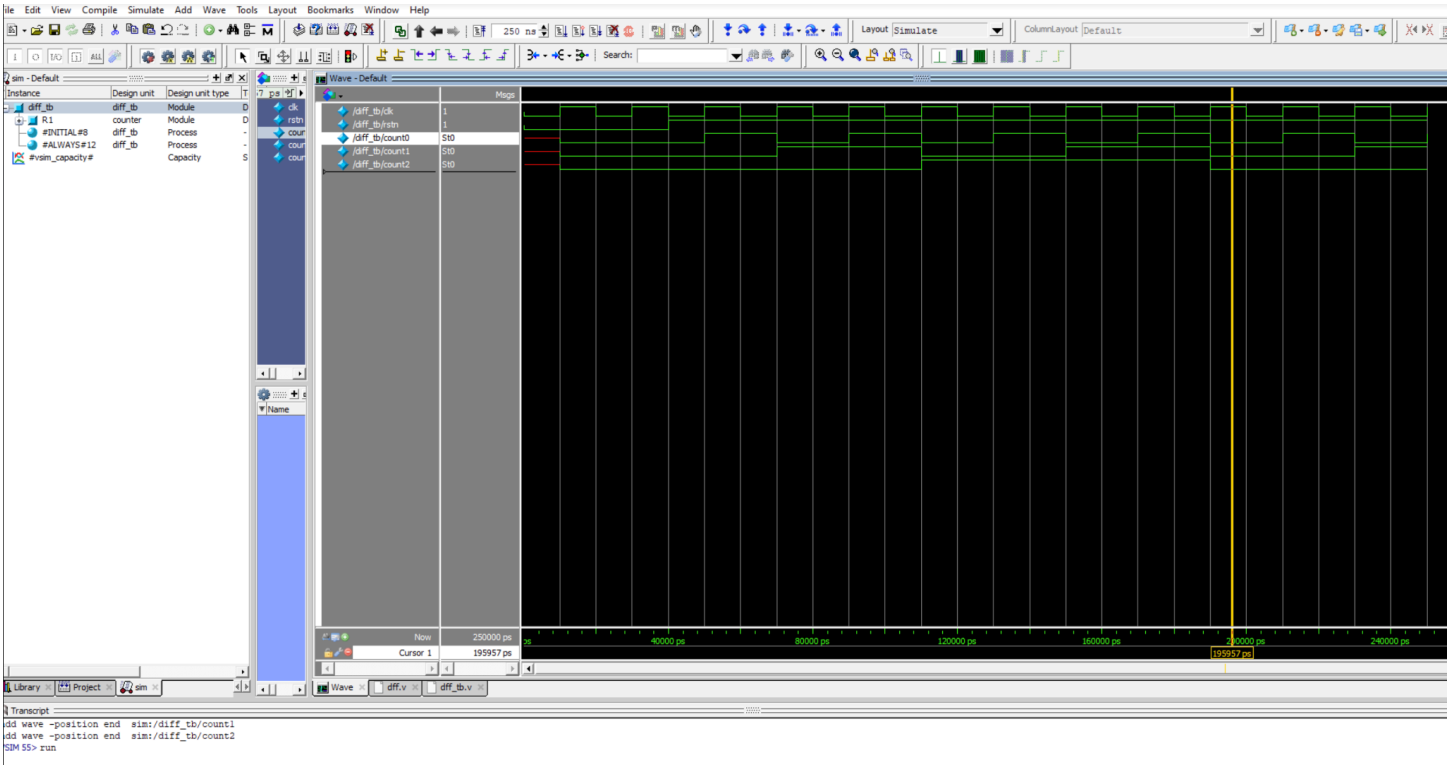
I get the resulting waveforms once I simulate my test bench.



The wave form above is the result of my code. The yellow bar is something I want to highlight. It results in an output of 000. Later on, in the next loop it results in something else. Let me highlight it below.



Ok so now the output is ‘000’. I can clearly see that to the left of the wave form. The objects have 0, 0, 0 as the output. This change in output demonstrates that the testbench is working correctly.



The waveform displayed shows how the output returns to 000 again. This ensures that the code works and loops back to 000 from 1.