RTC6222 FM Tuner

Description

The RTC6222 is a single-chip broadcast FM radio tuner with fully integrated building blocks as LNA, VCO with digital synthesizer, digital channel selection filter and digital FM demodulator. The RTC6222 integrates the tuner function from antenna input to mono audio output. The FM tuner only requires a minimum amount of small and low cost external components to be a very attractive solution for portable devices. With a powerful audio engine, the RTC6222 is able to deliver optimum sound quality under hostile channel conditions.

Feature

- Worldwide FM band support (64–108 MHz)
- Digital frequency synthesizer
- On-chip VCO
- On-chip loop filter
- Autonomous search tuning
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Signal strength measurement
- Programmable de-emphasis (50/75 μs)
- Digital adaptive noise suppression
- Volume control
- 32.768 kHz, 12M, 24M, 13M, 26M, 19.2M, 38.4MHz reference clock
- MONO Audio Output
- 2.0 V to 3.6 V supply voltage
- Integrated LDO regulator
- SOP-8 package
- Pb-free / RoHS compliant
- Built in audio amp for 32ohm load

Application

- MP3 players
- BT & MP3 Boom Box
- Gift

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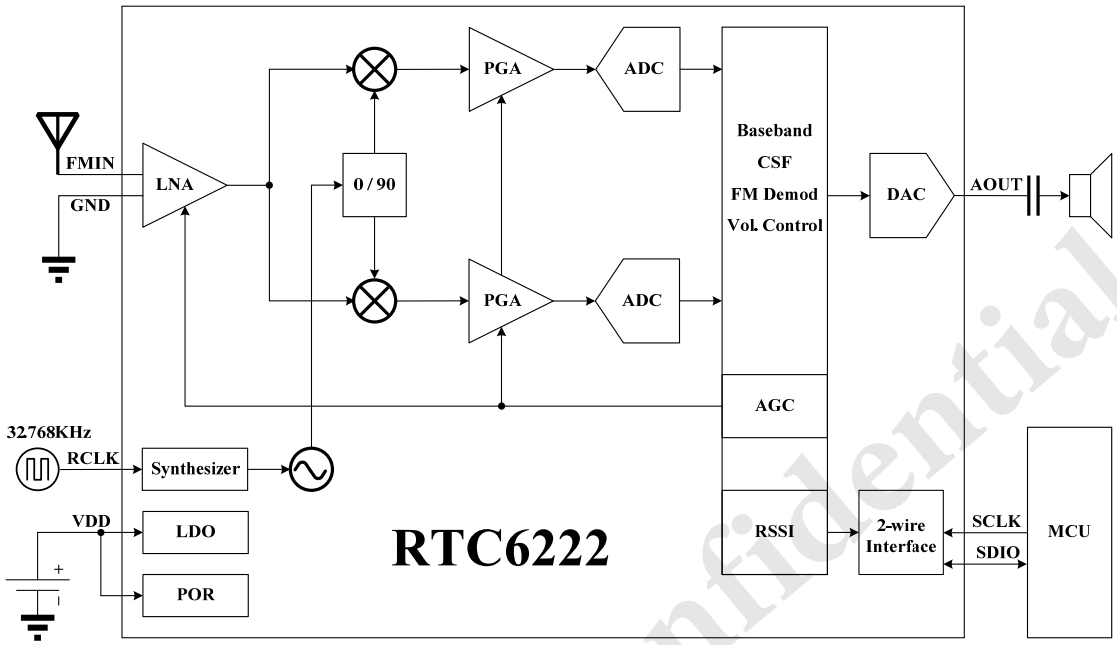
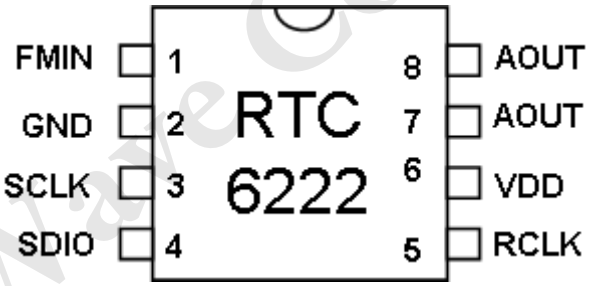
◆ Functional Block Diagram & Pin Out (top view through package)





Pin Function Description

Pin Number	Name	Description
1	FMIN	FM RF input. For single-ended operation
2	GND	Chip RF ground. Connect to ground plane on PCB.
3	SCLK	2-wire serial clock input.
4	SDIO	2-wire serial data input/output.
5	RCLK	External reference clock input.
6	VDD	Power supply voltage.
7	AOUT	Audio output.
8	AOUT	Audio output.

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1. Overview

RTC6222 is a monolithic FM receiver which is allowed to directly supply 2.0V ~ 3.6V from battery. It requires only one external bypass capacitor to minimize BOM cost and design easily for the miniature application.

1.1. FM Receiver

It uses optimized system architecture to lower the system cost and area, and recovers FM broadcast signal with low power consumption and to eliminate environmental noise with soft-mute algorithm.

It integrates a low-noise amplifier (LNA), an automatic gain control (AGC) circuit, a quadrature mixer, two programmable amplifiers (PGA), a pair of analog to digital converters (ADCs). The LNA supports FM broadcast band (64MHz~108MHz). The AGC controls the gain of the LNA and PGA to adjust the input power to optimum signal level for demodulation automatically. Proceeded by LNA, the quadrature mixer down-converts the RF signal to IF signal. The IF signal is amplified, filtered, digitized, and then passed to a baseband processor to perform FM demodulation. RTC6222 provides mono digital audio signals to a digital to analog converters (DACs) for generating high-quality mono analog sound. RTC6222 also integrates a frequency synthesizer and a voltage-controlled-oscillator (VCO), where the synthesizer reference to external clock source.

1.2. Audio Processing

High-frequency interferences and noise can be reduced by pre-emphasis and de-emphasis technology to improve SNR. Since the high audio frequency is accentuated by pre-emphasis universally when FM signal is transmitted, the received FM signal is applied to attenuate high audio frequency using a de-emphasis filter. The CSR0_DEEM bit can be programmed for either 50 or 75us for de-emphasis time constant.

The audio output could be muted by CSR0_DMUTE bit. Volume can be adjusted digitally through CSR0_VOLUME[3:0] bits.

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Audio output can be attenuated and audible noise can be minimized during weak-signal level by the software mute function. Four levels of soft-mute tuning (fastest, fast, slow and slowest) are defined in register bits CSR0_SMUTERATE[1:0]. In addition, 4 levels of attenuation (16,14,12 and 10dB) are defined in register bits CSR0_SMUTEATT[1:0]. The soft-mute function can be disabled by register CSR0_DSMUTE.

1.3. Tuning and Seeking

The tuning frequency is defined as:

Frequency (KHz) = CSR0_CH *10kHz

The Channel Spacing is selected by ctl_fm_seek_step [1:0]. The Channel Number is defined by CSR0_CH[14:0]. Setting CSR0_TUNE bit is to enable tuning operation. The seek/tune done (STD) bit set when tuning process is done and RSSI level is available.

When seeking process is initiated by setting CSR0_SEEK, the tuning frequency will be seek up or seek down depending on the setting of CSR0_SEEKUP. The RSSI and tuned channel are readable in RSSI[7:0] and STOP_CH[14:0] respectively when the STD bit is set to high to indicate the completion of seek operation. The SF bit is set to high to indicate that the tuned channel is seek failure when the seeking parameter of all seeking channel is not meet seeking criteria. Seek channel can be read by STOP_CH[14:0] during the entire seek operation.

The seek operation can always be deactivated by setting CSR0_SEEK bit to low.

1.4. Reset and Power-up

1.4.1. Reset

RTC6222 is reset by power-on-reset (POR), and the internal registers are reset to their default values. Upon POR asserting from low to high, RTC6222 will leave out reset state.

1.4.2. Power-up

Power-up can be set by CSR0_ENABLE defined in register 06h. When RTC6222 is reset, CSR0_ENABLE is set to default 0. To enable RTC6222 into power-up mode setting CSR0_ENABLE = 1 and the following chip programming can be performed.

1.5. Initialization Sequence

The initialization sequence can be referenced in Figure 1.

1.5.1. To initialize the device

1. Supply voltage to VDD.
2. Wait 50ms then write 0x96AA to address 0 to power on the device.
3. Wait 100ms then provide RCLK.
4. Write initial patch.
5. Set CSR0_ENABLE=1 to enable FM as defined in Figure 1.
6. Wait 300ms.
7. Start to tune channel.

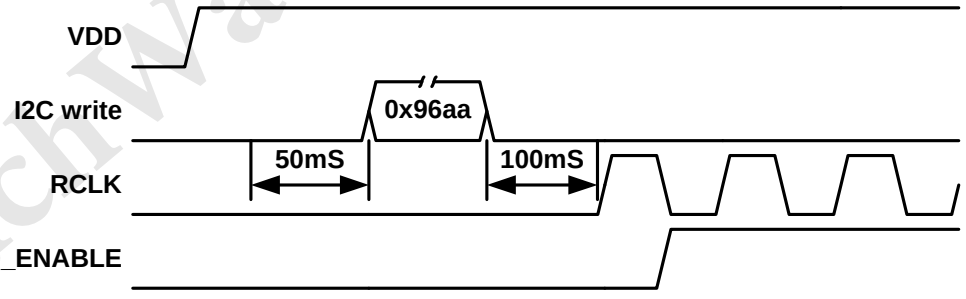

Figure 1. Initialization sequence

1.5.2. To power down the device

1. Write 0x16AA to address 0 to power down the device. See Figure 2.

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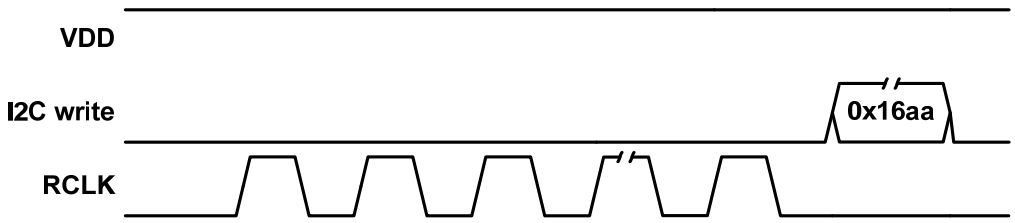

Figure 2. Power down sequence

1.6. Control Interface

RTC6222 supports only I2C interface. Registers can be operated even RCLK is disappeared. VDD is required for register operation.

1.6.1 2-wire Control Interface

For 2-wire I2C operation, SDIO and SCLK are operated in the open-drain, so external pull-up resistors are required on PCB board. The transfer begins with START condition shown in Table 1. An 8-bits control word is defined in which is A6, A5, A4, A3, A2, A1, A0 and R/W_ where A6:A0=1100100b and R/W_ = 1/0 means read/write operation. This control word is internally latched on rising SCLK edge. To acknowledge control word, SDIO is driven low for one cycle before the next falling SCLK edge.

For write operation, (from HOST write to RTC6222), RTC6222 latches the incoming serial 8-bit data word on rising SCLK edge, as shown in Figure 3. To acknowledge (ACK) each data word, SDIO is driven low for one cycle before the next falling SCLK edge. For write operation, host must send BANK[3:0]/ADDR[3:0] first then continue write the following data words until the last register is reached. Host can even further write the following data words because the internal address counter automatically wraps around to the first register.

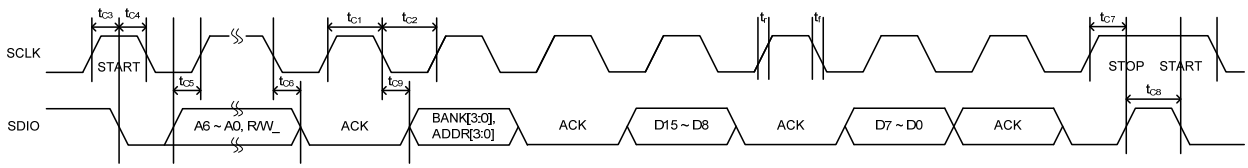

Figure 3. 2-Wire control interface write timing parameters

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Data transfer completes when STOP condition happens to make internal address counter rest to 0. Refer to table 1 for STOP condition.

For read operation (host read data from RTC6222), the serial 8-bit data word is shifted out at each falling SCLK edge and following with acknowledge as Figure 4. Before reading, host must send BANK[3:0]/ADDR[3:0] first without data. Host can continuously read the following data words until the last register is reached. Host can even further read the following data words because the internal address counter automatically wraps around to the first register. Host should acknowledge each data word but send a non-acknowledge specifically after the data word that occurs before the STOP condition. The internal address counter is reset to 0 when STOP condition is happen.

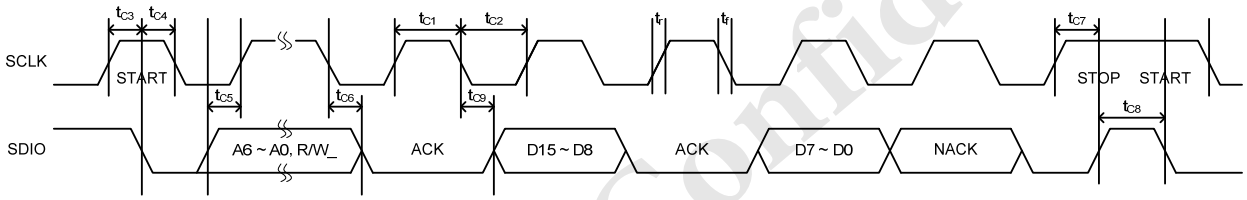

Figure 4. 2-Wire control interface read timing parameters

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Table 1. 2-Wire control interface characteristics

(VDD = 2 to 3.6 V T_A = –20 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
SCLK Frequency	f_{SCL}		0		400	kHz
SCLK High Time	t_{C1}		600			ns
SCLK Low Time	t_{C2}		1300			ns
Setup Time for START	t_{C3}		600			ns
Hold Time for START	t_{C4}		600			ns
SDIO Input to SCLK ↑ Setup	t_{C5}		100			ns
SDIO Input to SCLK ↓ Hold	t_{C6}		100		900	ns
Setup Time for STOP	t_{C7}		600			ns
STOP to START Time	t_{C8}		1300			ns
SDIO Output to SCLK ↓	t_{C9}		20 + 1*Cb		250	ns
SDIO, SCLK Rising Time	t_r		20 + 1*Cb		300	ns
SDIO, SCLK Falling Time	t_f		20 + 1*Cb		300	ns
SCLK, SDIO Capacitive Loading	C_b				50	pF

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2. Electrical Characteristic

Table 2. Recommended operating conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply Voltage	VDD	2		3.6	V
Ambient Temperature	T_A	-20	25	85	°C

Table 3. Absolute maximum ratings

PARAMETER	SYMBOL	VALUE	UNIT
Power Supply Voltage	VDD	–0.5 to 3.6	V
Input Current[1]	I_{IN}	±10	mA
Input Voltage[1]	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Operating Temperature	T_{OP}	–40 to 95	°C
Storage Temperature	T_{STG}	–40 to 125	°C
RF Input Level[2]		0.4	V_{pK}

Notes:
1. For input pins SCLK, SDIO, RCLK.
2. At RF input pins.

Table 4. DC electrical characteristics

(VDD = 2 to 3.6 V, TA = -20 to 85 °C)

PARAMETER	SYMBOL	TESTCONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Current[1]	IA	CSR0_ENABLE = 1		19		mA
Logic High Input Voltage[2]	VIH		0.7 x V_{DD}		V_{DD} + 0.3	V
Logic Low Input Voltage[2]	VIL				0.3 x V_{DD}	V
Logic High Input Current[2]	IIH	VIN = 3.6V VDD = 3.6 V	-10		+10	uA
Logic Low Input Current[2]	IIL	VIN = 0V VDD = 3.6 V	-10		+10	uA
Logic High Output Voltage[3]	VOH	IOUT = 500 µA	0.8 x V_{DD}			V
Logic Low Output Voltage[3]	VOL	IOUT = -500 µA			0.2 x V_{DD}	V

Notes:
1. Refer to register 06h, for the description of CSR0_ENABLE bit.
2. For input pins SCLK, SDIO, RCLK.
3. For output pins SDIO.

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Table 5. FM receiver characteristics

(VDD = 2 to 3.6V, T_A = –20 to 85 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Frequency			64	---	108	MHz
Usable Sensitivity		(S+N)/N=26dB	---	1.6	2.3	μV EMF
Adjacent Channel Selectivity		± 200kHz	35	50	---	dB
Alternate Channel Selectivity		± 400kHz	50	60	---	dB
IIP3		Δf1=200 kHz, Δf2=400 kHz	---	90	---	dBuV EMF
IIP3		Δf1=400 kHz, Δf2=800 kHz	---	99	---	dBuV EMF
Audio Output Voltage		Load 10KΩ ‖ 10pF	---	140	---	mVrms
Audio Frequency Response		0 to -3dB	30	---	15K	Hz
Audio (S+N)/N			50	53	---	dB
Audio Total Harmonic Distortion (THD)		Mono	---	0.1	0.5	%
Power-up Time		From Power-off to audio out	---	150	---	ms
Tuning/Seeking Time			---	30	---	ms

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3. Registers Summary

Table 6. Registers summary

Register Name	Description	Offset Address	Default
DEVICEID	Device ID code	00H	1688H
CHIPID	Chip ID code	01H	18C0H
VOLUME CONTROL	Volume configuration register	02H	8000H
TUNE	Tuning channel setting	03H	0000H
SYSCONFIG	System configuration register	04H	0100H
SEEK	Seek configuration register	05H	050FH
POWERCONFIG	Power configuration register	06H	5000H
Reserved	Reserved	07H	4000H
SEEK_FREQ_TOP	Seek top frequency	08H	0465H
SEEK_FREQ_BOT	Seek bottom frequency	09H	0265H
STATUS	Status register and work channel	0AH	0000H
RSSI	RSSI	0BH	0000H
STOP_CH	Stop channel	0CH	0000H
Reserved	Reserved	0DH	0000H
Reserved	Reserved	0EH	0000H
Reserved	Reserved	0FH	0000H

4. Register Descriptions

DEVICEID (Device ID code), 00H

Field	Bits	Type	Default	Description
PART_NUMBER	15:12	R		Part number
MFGID	11:0	R		Manufacture ID

CHIPID (Chip ID code), 01H

Field	Bits	Type	Default	Description
REVISION_NO	15:10	R		
Reserved	9:0	R		Reserved

VOLUME CONTROL (Volume configuration register), 02H

Field	Bits	Type	Default	Description
CSR0_DSMUTE	15	R/W	1	Disable Softmute

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				0 = Enable Softmute 1 = Disable Softmute(default)
CSR0_DMUTE	14	R/W	0	Disable Mute 0 = Enable Mute(default) 1 = Disable Mute
Reserved	13	R	0	Reserved
CSR0_DEEM	12	R/W	0	De-emphasis 0 = 75us(default) 1 = 50us
Reserved	11:8	R	0x0	Reserved
CSR0_SMUTERATE	7:6	R/W	0x0	Softmute Enter/Recover Rate 00 = fastest(default) 01 = fast 10 = slow 11 = slowest
CSR0_SMUTEATT	5:4	R/W	0x0	Softmute Attenuation value 00 = 16dB(default) 01 = 14dB 10 = 12dB 11 = 10dB
CSR0_VOLUME	3:0	R/W	0x0	Volume 0000 = mute(default). 0001 = -28dBFS …… 1110 = -2dBFS 1111 = 0dBFS

TUNE (Tuning channel setting), 03H

Field	Bits	Type	Default	Description
CSR0_TUNE	15	R/W	0	Enable Tune function 0 = Disable(default) 1 = Enable
CSR0_CH	14:0	R/W	0x0	Tuning Channel Channel for tune operation

SYSCONFIG (System configuration register), 04H

Field	Bits	Type	Default	Description
Reserved	15	R	0	Reserved
Reserved	14	R/W	0	Reserved
CSR0_DIS_AGC	13	R/W	0	Disable AGC 0 = Enable AGC (default)

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				1 = Disable AGC
Reserved	12	R/W	0	Reserved
ctl_fm_seek_step	11:10	R/W	0x0	Seeking step: 00: 50kHz 01: 10kHz 10: 100kHz;
Reserved	9:8	R/W	0x1	Reserved
Reserved	7:0	R	0x0	Reserved

SEEK (Seek configuration register), 05H

Field	Bits	Type	Default	Description
CSR0_SEEK	15	R/W	0	Enable Seek function 0 = Disable(default) 1 = Enable
CSR0_SEEKUP	14	R/W	0	Seek Direction 0 = Seek down(default) 1 = Seek up
CSR0_SKMODE	13	R/W	0	Seek Mode. 0 = Wrap at the upper or lower band limit and continue seeking (default). 1 = Stop seeking at the upper or lower band limit.
Reserved	12	R	0	Reserved
Reserved	11:10	R/W	0x1	Reserved
Reserved	9:8	R/W	0x1	Reserved
csr_rssi_low_th	7:4	R/W	0x0	RSSI low threshold = csr_rssi_low_th * 4
csr_rssi_mono_th	3:0	R/W	0xF	rssi mono threshold = csr_rssi_mono_th * 4

POWERCONFIG (Power configuration register), 06H

Field	Bits	Type	Default	Description
CSR0_ENABLE	15	R/W	0	Power-up Enable Default = 0
Reserved	14	R/W	1	Reserved
Reserved	13	R/W	0	Reserved
Reserved	12	R/W	1	Reserved
Reserved	11:9	R	0x0	reserved
Reserved	8	R/W	0	Reserved
Reserved	7	R/W	0	Reserved
Reserved	6:4	R/W	0	Reserved
CSR0_VOLEXT	3	R/W	0	0: Volume attenuate 0dB more (default) 1: Volume attenuate 15dB more

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CSR0_CLK_TYPE	2:0	R/W	0x0	000: 32.768KHz (default) 001: 12MHz 010: 13MHz 011: 19.2MHz 100: 32.768KHz 101: 24MHz 110: 26MHz 111: 38.4MHz

Reserved, 07H

Field	Bits	Type	Default	Description
Reserved	15	R/W	0	Reserved
Reserved	14	R/W	1	Reserved
Reserved	13:11	R	0x0	Reserved
Reserved	10	R/W	0	Reserved
Reserved	9:6	R	0x0	Reserved
Reserved	5:4	R/W	0x0	Reserved
Reserved	3:2	R/W	0x0	Reserved
Reserved	1:0	R/W	0x0	Reserved

SEEK_FREQ_TOP (Seek top frequency), 08H

Field	Bits	Type	Default	Description
Reserved	15:12	R	0x0	Reserved
CSR0_FM_SEEK_FREQ_TOP	11:0	R/W	0x465	The top frequency of seeking Unit: 100K Default = 112.5 decimal

SEEK_FREQ_BOT (Seek bottom frequency), 09H

Field	Bits	Type	Default	Description
Reserved	15:12	R	0x0	Reserved
CSR0_FM_SEEK_FREQ_BOT	11:0	R/W	0x265	The bottom frequency of seeking Unit: 100K Default = 61.3 decimal

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STATUS (Status register and work channel), 0AH

Field	Bits	Type	Default	Description
FBBMUTE	15	R	0	TuneSeekBusy
STD	14	R	0	Seek/Tune Done 0 = Not complete 1 = Done
SF	13	R	0	Seek Fail 0 = Seek successful 1 = Seek failure
Reserved	12:11	R	0x0	Reserved
SI	10	R	0	Stereo Indicator 0 = Mono 1 = Stereo
Reserved	9:5	R	0x0	Reserved
Reserved	4:0	R	0x0	Reserved

RSSI (RSSI), 0BH

Field	Bits	Type	Default	Description
Reserved	15:10	R	0x0	Reserved
Reserved	9	R	0x0	Reserved
Reserved	8	R	0x0	Reserved
RSSI	7:0	R	0x0	RSSI RSSI unit is dBuv

STOP_CH (Stop channel), 0CH

Field	Bits	Type	Default	Description
Reserved	15	R	0	Reserved
LVIOCHAN_NUM	14:0	R	0x0	Stop channel frequency

Reserved, 0DH

Field	Bits	Type	Default	Description
Reserved	15:11	R	0x0	Reserved.
Reserved	10:0	R	0x0	Reserved

Reserved, 0EH

Field	Bits	Type	Default	Description
Reserved	15:14	R	0x0	Reserved

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Reserved	13	R	0	Reserved
Reserved	12:7	R	0x0	Reserved.
Reserved	6:0	R	0x0	Reserved

Reserved, 0FH

Field	Bits	Type	Default	Description
Reserved	15:0	R	0x0	Reserved

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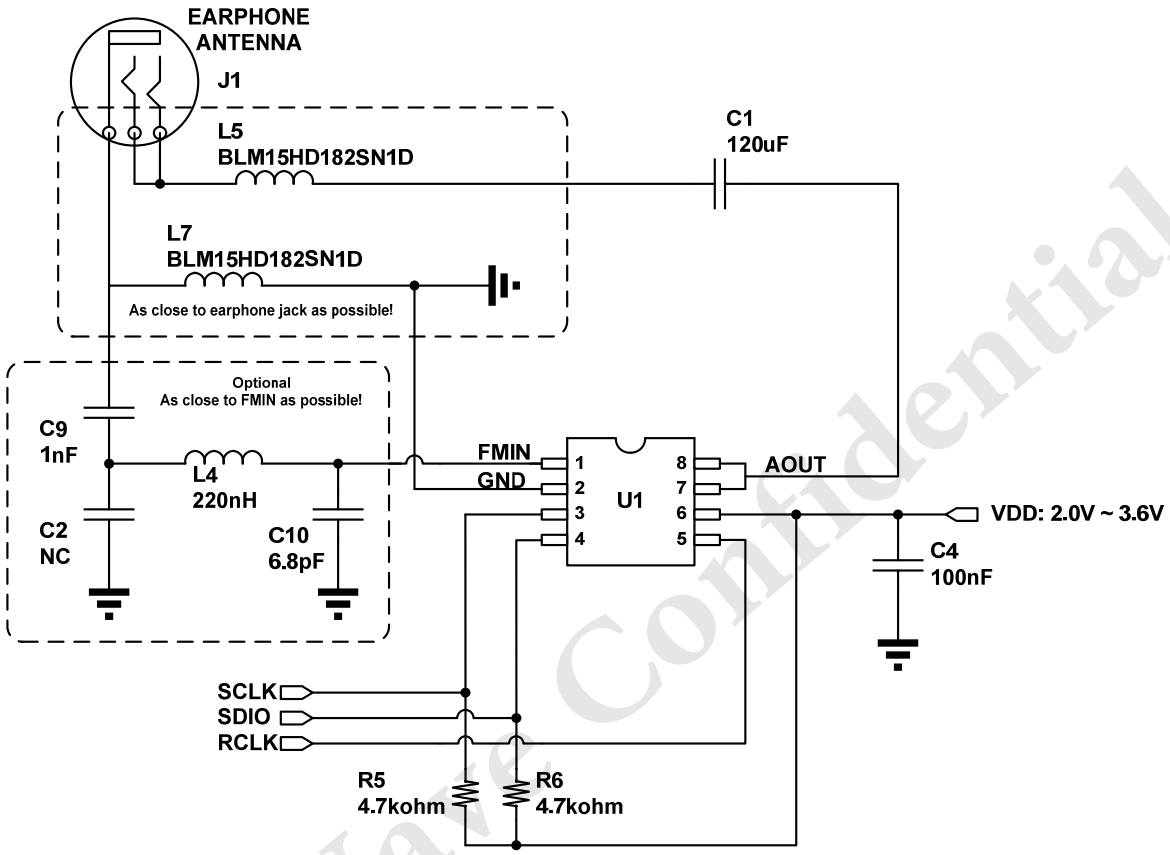
Application Circuit

Application Circuit for RCLK and headphone



Notes:

1. Place C4 close to VDD pin
2. Options: the antenna matching network is kept for high sensitivity mode.
3. Strongly recommended to keep L5, L7 and C9 when applying earphone antenna.

Part Type	Component	Value/Description	Supplier
6222	U1	6222 FM Radio Tuner	RichWave
120uF	C1	Audio AC couple capacitors	
BLM15HD182SN1D	L5, L7	Ferrite bead keep high-impedance for RF path	
100nF	C4	Supply bypass capacitor 100nF ,±20%,Z5U/X7R	
4.7kohm	R5, R6	I2C pull-up resistors	
6.8pF	C10	Antenna matching	
220nH	L4	Antenna matching	
1nF	C9	DC-blocking capacitor	

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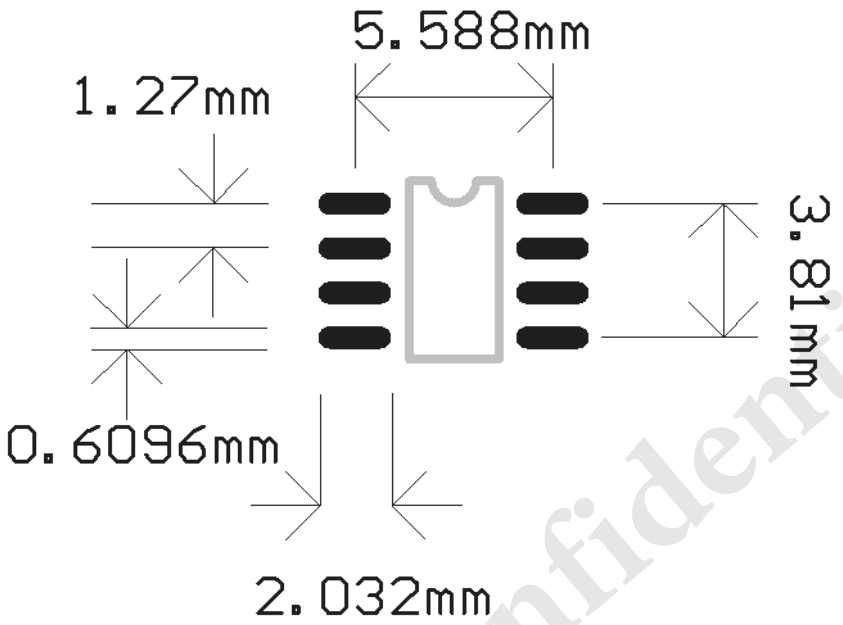
PCB Layout Footprint



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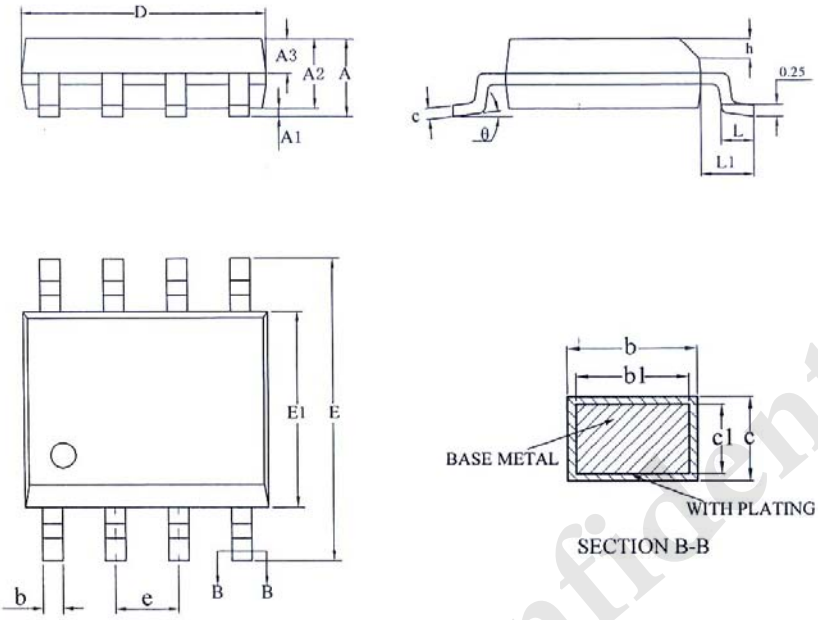
Package Outline Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	80*80	90*90	95*130

Specifications subject to change without notice
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