Yun Chia Yu

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Education

National Taiwan University(NTU)

Taipei, Taiwan

B.S. in Electrical Engineering, rank: 33/189 (17%)
GPA: Overall: 4.13/4.3, Major: 4.14/4.3, Last 60: 4.20/4.3

Sept. 2019 - Jun. 2023

- **IC-related courses**: Electronics(I&II)(A+), Integrated Circuit Design(A+), Computer Architecture(A+), Integrated Circuit Design Lab(A+), Digital Signal Processing in VLSI Design(A+), Advanced Integrated Circuit Design(A), Digital Circuit Lab(A-)
- **CS&Mathematics-related courses**: Machine Learning(A+), Computer Vision(A+), Calculus(A+), Probability and Statistics(A+), Linear Algebra(A+), Differential Equation(A+), Signals and Systems(A), Introduction to Digital Speech Processing(A)

Publication

Retraining-free Constraint-aware Token Pruning for Vision Transformer on Edge Devices

Co-1st Author

Yun-Chia Yu*, Mao-Chi Weng*, Ming-Guang Lin, An-Yeu Wu *Accepted*

(* denotes equal contribution), International Symposium on Circuits and Systems, 2024 (IEEE ISCAS 2024)

- Introduced Fisher information to evaluate token importance across different transformer blocks.
- Proposed a modified Viterbi algorithm to enable one-shot optimal pruning threshold set determinations under different FLOPs-constraints without retraining.
- Reduced FLOPs count of Vision Transformer-Base model by more than 27% with less than 0.4% accuracy loss, outperforming state-of-the-art retraining-free token reduction works.

Research Experience

Energy-aware pruning for NVM-based Computing-in-Memory (CIM) architecture for Vision Transformer (ViT)

Tools: Pytorch, NeuroSim

Undergraduate Research, Advisor: Prof. An-Yeu Wu, Dept. of EE, NTU *Sept. 2022 - Sept. 2023*

- Built a Python framework for autonomous conversion of transformer blocks from Pytorch to NeuroSim, facilitating the process of the energy estimation of ViT on hybrid CIM architecture with NeuroSim.
- Conducted experiments to incorporate trainable energy-aware pruning method into the crossbar-aware structure weight pruning for ViT, reducing 45% energy with less than 2% accuracy loss.

Energy-efficient keyword spotting (KWS) accelerator

Tools: Tensorflow, Verilog

Undergraduate Research, Advisor: Prof. Tsung-Te Liu, Dept. of EE, NTU *Sept. 2021 - Present*

- Evaluated the computation complexity and the memory access of various neural networks for the KWS system.
- Verified a lightweight 1-D DSCNN model for the KWS system and conducted power measurement of the KWS processor fabricated in 180nm CMOS process.

Work Experience

Energy-efficient spiking neural network (SNN) processor

Tools: Python, Verilog

Digital Circuit Design Intern, Industrial Technology Research Institute *Feb. 2023 - Present*

- Analyzed mathematically the energy efficiency in event-based SNN processors associated with different levels of parallelism and input spiking rates.
- Identified the limitations of deploying multi-layer SNN on model-agnostic SNN processors, including low PE utilization, low throughput for the packet decoder stalling problem, and redundant memory access of neuron states across spikes in the same timestamp.

Projects

Road marker 3D point cloud reconstruction

Tools: Python, OpenCV

Computer Vision Course taught by Prof. Shao-Yi Chien, Dept. of EE, NTU — *Mar. 2023 - Jun. 2023*

- Reconstructed road marker 3-D point cloud from 2-D road images.
- Implemented a 2-step process comprising Homography-based 2-D key points matching and 3-D point cloud reconstruction with Visual Odometry.

FPGA-based sparse convolution neural network processor

Tools: System Verilog, NC-Verilog, Quartus II

Digital Circuit Lab Course taught by Prof. Chia-Hsiang Yang, Dept. of EE, NTU — *Sept. 2022 - Jan. 2023*

- Deployed a sparse convolution neural network processor on Altera DE2-115 FPGA.
- Adopted channel-first dataflow, a specialized data compression format, and an input-weight pair matching module to enhance energy efficiency by mitigating memory writeback contention of output partial sums.

ASIC for Elliptic Curve Cryptography (ECC) encrypter

Tools: Verilog, NC-Verilog, Design Compiler, Innovus

Integrated Circuit Design Lab Course taught by Prof. Tzi-Dar Chiueh, Dept. of EE, NTU — *Mar. 2022 - Jun. 2022*

- Designed and taped out a 163-bit ECC encrypter ASIC fabricated in 180nm CMOS process.
- Reduced the area cost to below 2 mm ^ 2 by decomposing the ECC algorithm into three computation types and employing an area-efficient architecture, utilizing only 8 163-bit pipeline registers.

Honors & Awards

2023 **Dean's Award**, GPA: 4.3/4.3, top 5% in the department. — *Taipei, Taiwan*

2020 **ROHM enterprise award in MakeNTU Competition**, Designed a gesture-based control glove utilizing accelerometer and gyroscope sensors to detect hand gestures and wirelessly control LED lights in real-time. — *Taipei, Taiwan*

Leadership & Extra-Curricular Activities

NTU Azalea Festival

Taipei, Taiwan

Electrical Engineering Department Director — *Mar. 2022 - Mar.2022*

- Led a 15-member team in shooting 3D laboratory introduction videos and inviting professors to deliver live-stream lectures.
- Provided high school students with a better understanding of their upcoming college learning experience.

NTUEE Student Association

Taipei, Taiwan

Courses Improvement Department Leader — *Sept. 2021 - Jun. 2022*

- Assisted in the collection and organization of academic files related to Electrical Engineering courses.

Skills

Circuit Design NC-Verilog, Design Compiler, Innovus, Quartus II
Programming C++, Python, Verilog, Matlab, Shell