微算機系統

小組專案報告

實驗七：

八位元除法器

組別： 20

班級、姓名與學號：

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醫工三 湯青秀 B812110011

日期 :112年12月15日

一、實驗內容：

1. 請設計出一個可進行觸發的除法運算的電路系統
2. 必須透過移位暫存器配合實驗六運算方式，實現電路架構圖完成本次實驗
3. 測試時，以按鈕改變clock觸發事件進行運算並顯示結果
4. 除數與被除數輸入範圍為1-255，需顯示除法運算後的商與餘數結果
5. 可使用GENERIC以及PROCESS內之FOR LOOP
6. 需使用實驗五的多用途移位暫存器
7. 正確顯示“商”(Quotient)跟“餘”(Remainder)之結果於LED上。並在完成計算時(狀態機到達S4)，以16進制正確顯示“商”(Quotient) 跟“餘”(Remainder)之結果於七段顯示器上

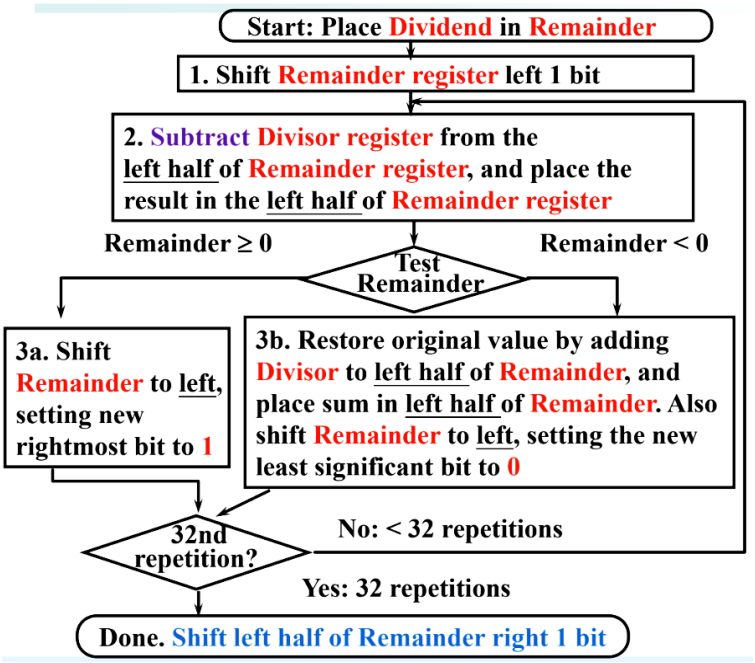
Variable	Pin Location	Signal Name
clk	PIN_M23	KEY[0]
output[0]	PIN_F19	LED[1]
output[1]	PIN_E19	LED[2]
output[2]	PIN_F21	LED[3]
Divisor(0)	PIN_AB28	SW[0]
Divisor(1)	PIN_AC28	SW[1]
Divisor(2)	PIN_AC27	SW[2]
Divisor(3)	PIN_AD27	SW[3]
Divisor(4)	PIN_AB27	SW[4]
Divisor(5)	PIN_AC26	SW[5]
Divisor(6)	PIN_AD26	SW[6]
Divisor(7)	PIN_AB26	SW[7]
Dividend(0)	PIN_AC25	SW[8]
Dividend(1)	PIN_AB25	SW[9]
Dividend(2)	PIN_AC24	SW[10]

Dividend(3)	PIN_AB24	SW[11]
Dividend(4)	PIN_AB23	SW[12]
Dividend(5)	PIN_AA24	SW[13]
Dividend(6)	PIN_AA23	SW[14]
Dividend(7)	PIN_AA22	SW[15]
clear	PIN_Y24	SW[16]
a0	PIN_G18	HEX0[0]
b0	PIN_F22	HEX0[1]
c0	PIN_E17	HEX0[2]
d0	PIN_L26	HEX0[3]
e0	PIN_L25	HEX0[4]
f0	PIN_J22	HEX0[5]
g0	PIN_H22	HEX0[6]
a1	PIN_M24	HEX1[0]
b1	PIN_Y22	HEX1[1]
c1	PIN_W21	HEX1[2]
d1	PIN_W22	HEX1[3]
e1	PIN_W25	HEX1[4]
f1	PIN_U23	HEX1[5]
g1	PIN_U24	HEX1[6]
a2	PIN_AA25	HEX2[0]
b2	PIN_AA26	HEX2[1]
c2	PIN_Y25	HEX2[2]
d2	PIN_W26	HEX2[3]
e2	PIN_Y26	HEX2[4]
f2	PIN_W27	HEX2[5]

g2	PIN_W28	HEX2[6]
a3	PIN_V21	HEX3[0]
b3	PIN_U21	HEX3[1]
c3	PIN_AB20	HEX3[2]
d3	PIN_AA21	HEX3[3]
e3	PIN_AD24	HEX3[4]
f3	PIN_AF23	HEX3[5]
g3	PIN_Y19	HEX3[6]
Quotient(0)	PIN_G19	LED[0]
Quotient(1)	PIN_F19	LED[1]
Quotient(2)	PIN_E19	LED[2]
Quotient(3)	PIN_F21	LED[3]
Quotient(4)	PIN_F18	LED[4]
Quotient(5)	PIN_E18	LED[5]
Quotient(6)	PIN_J19	LED[6]
Quotient(7)	PIN_H19	LED[7]
Remainder(0)	PIN_J17	LED[8]
Remainder(1)	PIN_G17	LED[9]
Remainder(2)	PIN_J15	LED[10]
Remainder(3)	PIN_H16	LED[11]
Remainder(4)	PIN_J16	LED[12]
Remainder(5)	PIN_H17	LED[13]
Remainder(6)	PIN_F15	LED[14]
Remainder(7)	PIN_G15	LED[15]

二、實驗過程及結果：

（一） 預期實驗結果的流程示意圖



（二） 設計電路示意圖

main →

process 1 : FSM.

case 1 : temp_s ∈ (左半邊 remainder - 除數) (右半 remainder)

case 2 : temp_p ∈ (左半邊 remainder + 除數) (右半 remainder)

process 2 : output select

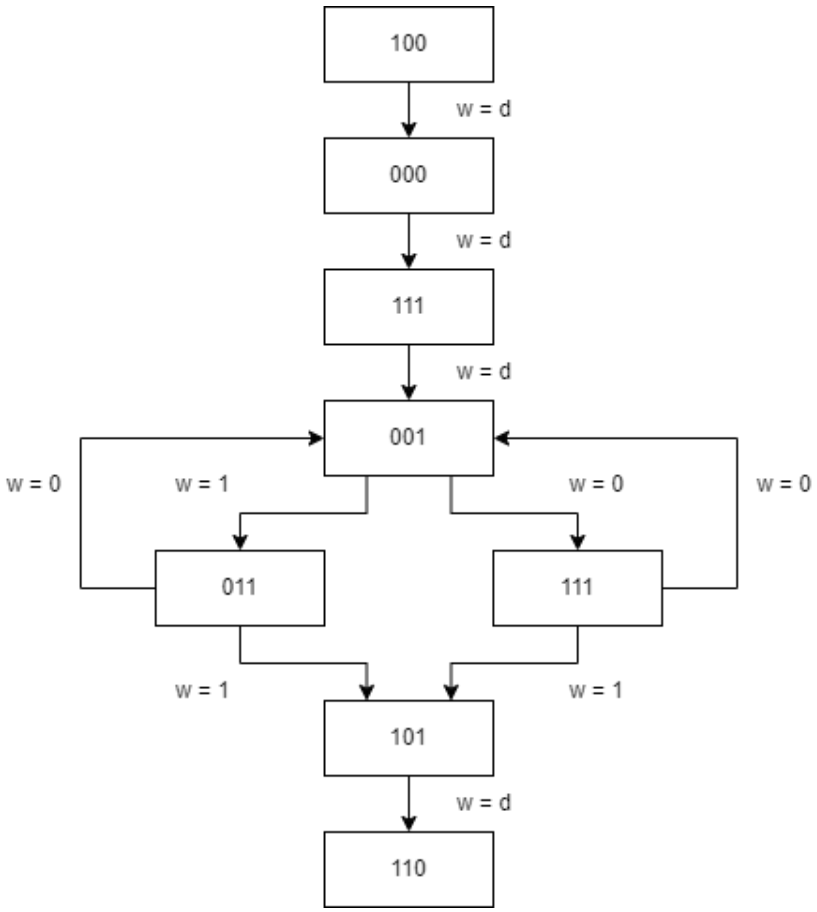
process 3 : count 次數 ⇒ 數到 8 次 時 run = 0

select w ⇒ "101" 時，如果 temp_s 最高位為 1 ⇒ w=0.

"011", "010" 時，如果還沒到 8 次 ⇒ w=0.

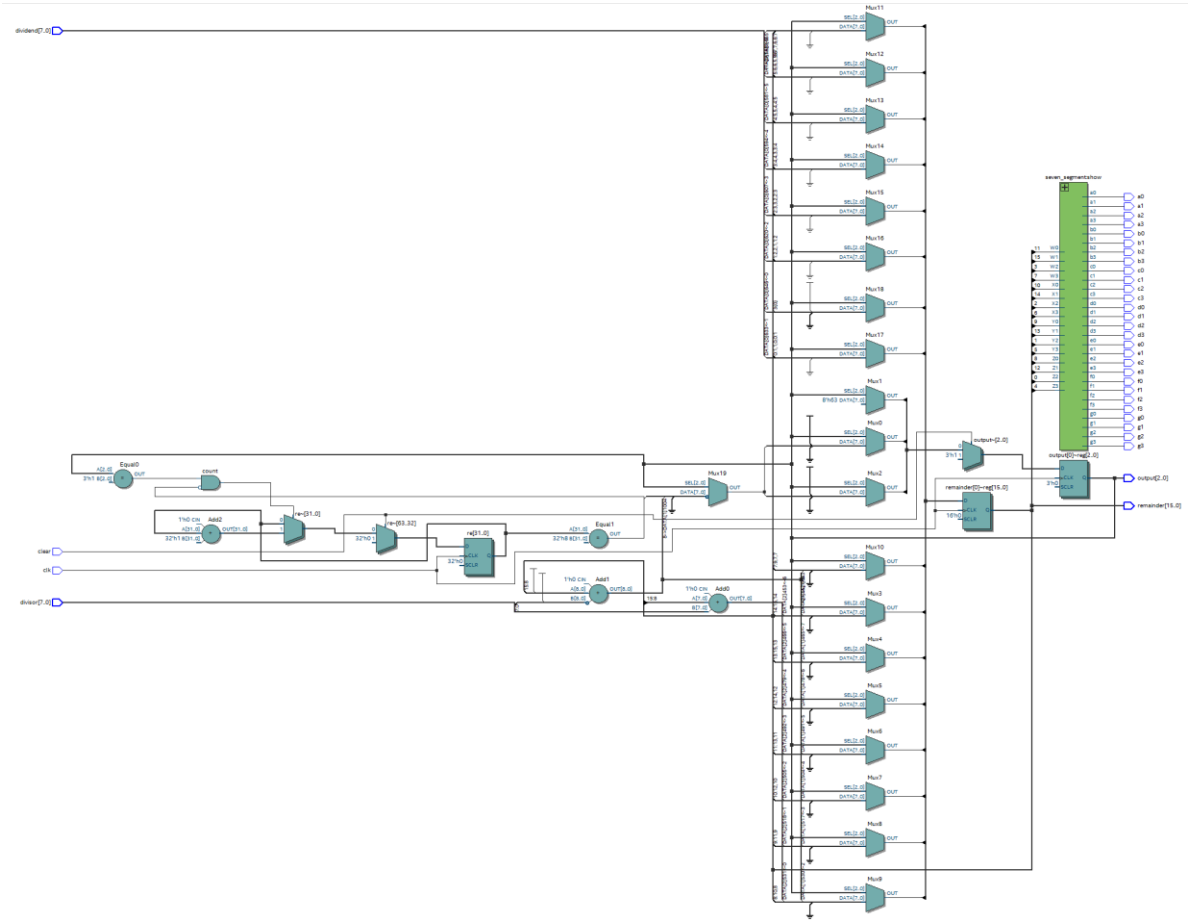
七段顯示器

process 1: FSM



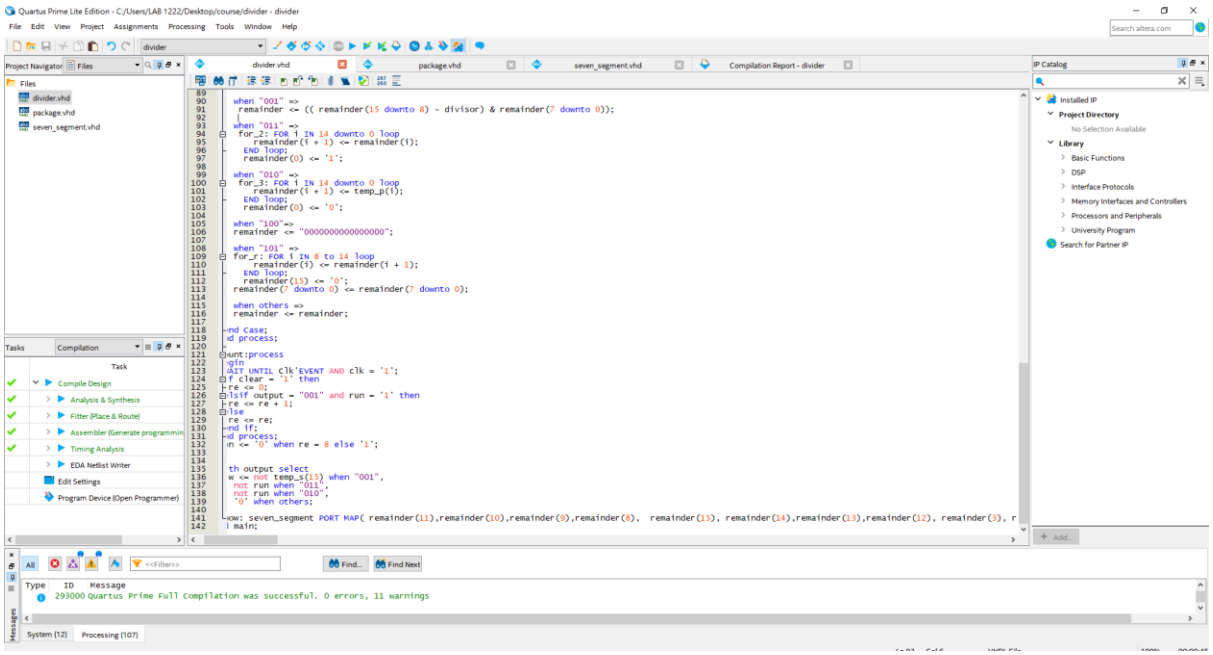
https://drive.google.com/file/d/1SFREBBdMMrIMH7U2qnHV2TXyJ2KqXx-2/view?usp=sharing

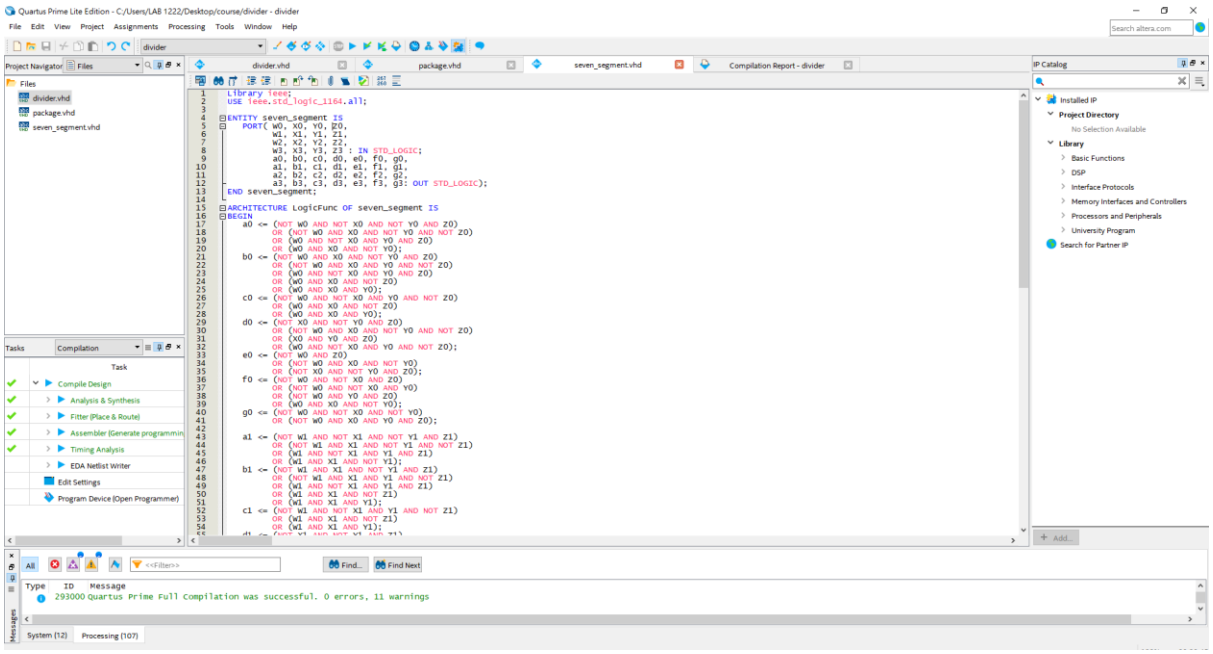
（三） 設計出的電路

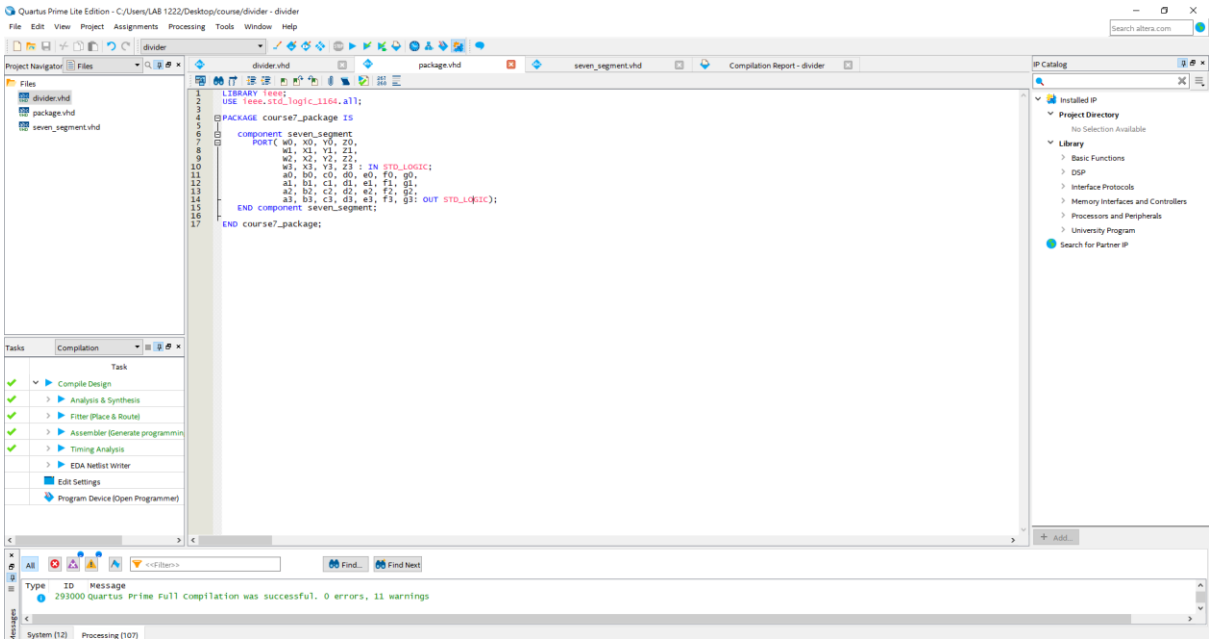


（四） 實驗過程

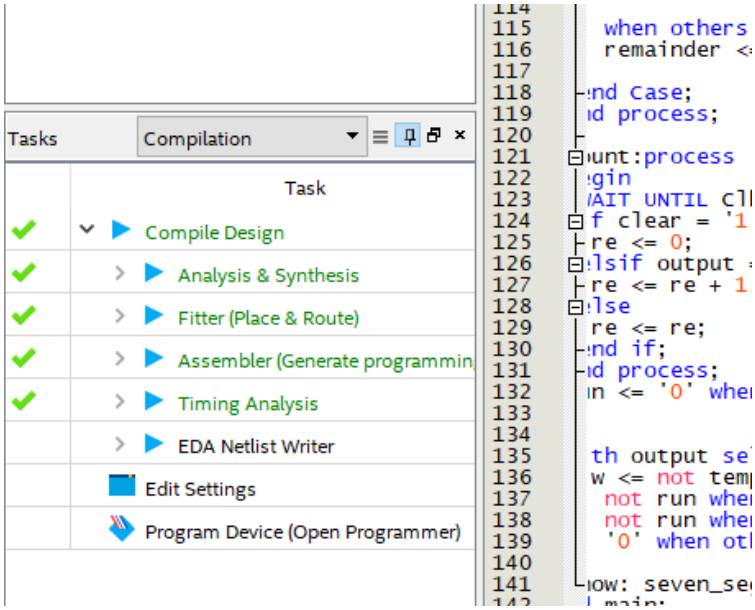
(1)　撰寫程式碼



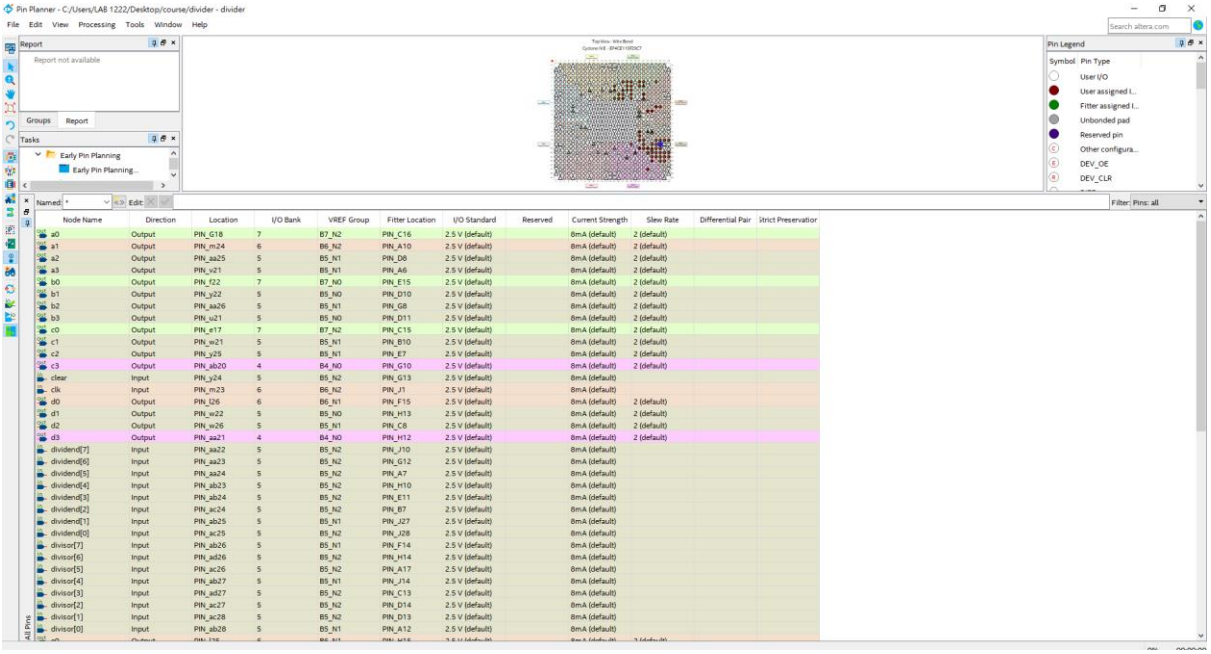


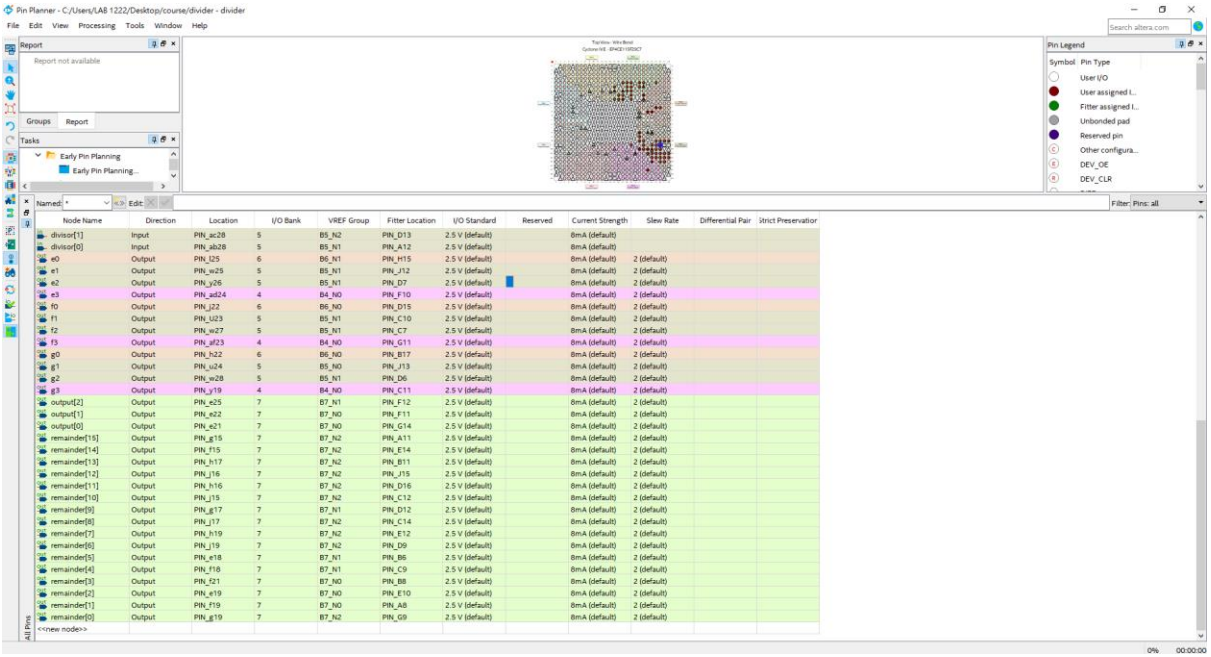

Quartus Prime Lite Edition - C:/Users/LAB 1222/Desktop/course/divider - divider
File Edit View Project Assignments Processing Tools Window Help
divider.vhd
package.vhd
seven_segment.vhd
Compilation Report - divider
Tasks
Compilation
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programmin
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)
IP Catalog
Installed IP
Project Directory
Library
Basic Functions
DSP
Interface Protocols
Memory Interfaces and Controllers
Processors and Peripherals
University Program
Search for Partner IP
Type ID Message
293000 Quartus Prime Full Compilation was successful. 0 errors, 11 warnings

(2)　編譯成功

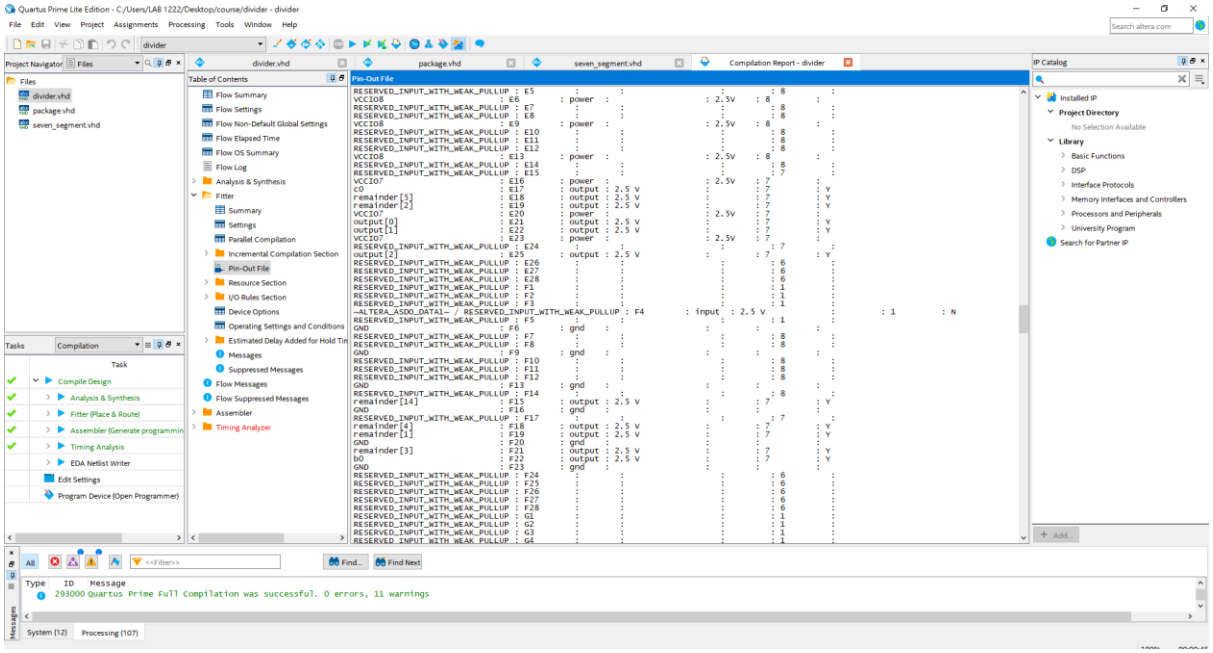

Tasks
Compilation
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programmin
Timing Analysis
EDA Netlist Writer
Edit Settings
Program Device (Open Programmer)

（3） 接脚位

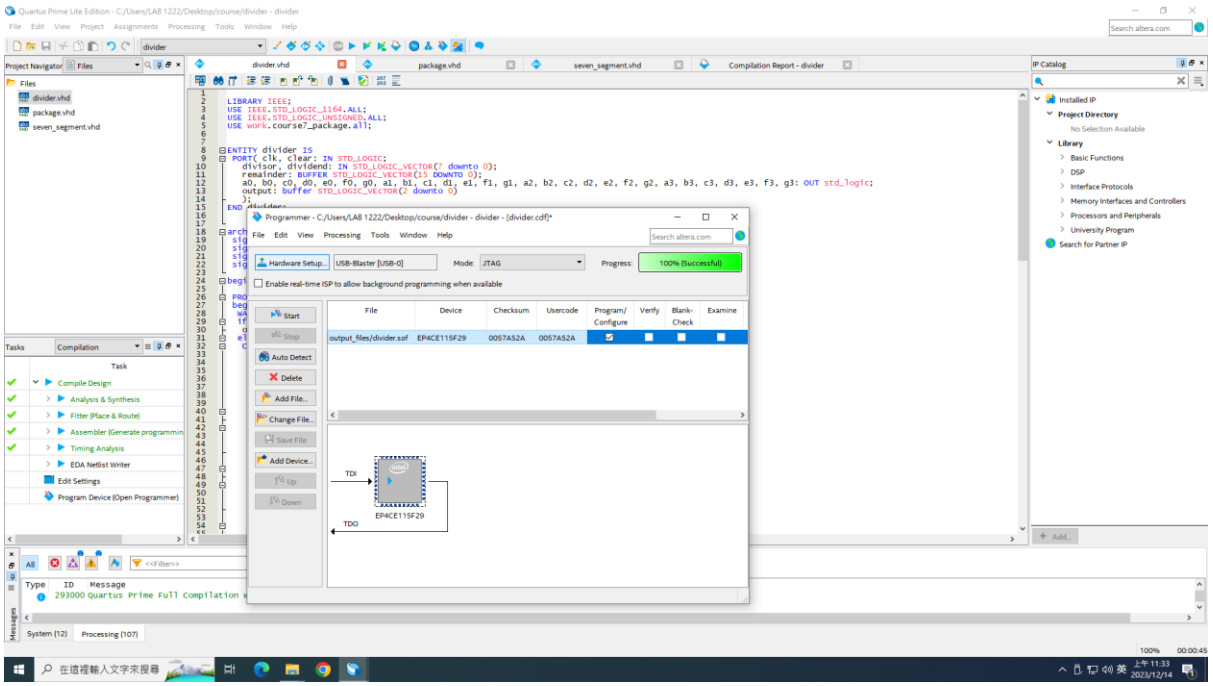

Pin Planner - C:/Users/LAB 1222/Desktop/course/divider - divider
File Edit View Processing Tools Window Help
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Pin Legend
Symbol Pin Type
User I/O
User assigned l...
Fitter assigned l...
Unbonded pad
Reserved pin
Other configura...
DEV_OE
DEV_CLR
Named: * Edit:
Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard Reserved Current Strength Slew Rate Differential Pair Strict Preservation
a0 Output PIN_G18 7 B7_N2 PIN_C16 2.5 V (default) 8mA (default) 2 (default)
a1 Output PIN_m24 6 B6_N2 PIN_A10 2.5 V (default) 8mA (default) 2 (default)
a2 Output PIN_aa25 5 B5_N1 PIN_D8 2.5 V (default) 8mA (default) 2 (default)
a3 Output PIN_v21 5 B5_N1 PIN_A6 2.5 V (default) 8mA (default) 2 (default)
b0 Output PIN_f22 7 B7_N0 PIN_E15 2.5 V (default) 8mA (default) 2 (default)
b1 Output PIN_y22 5 B5_N0 PIN_D10 2.5 V (default) 8mA (default) 2 (default)
b2 Output PIN_aa26 5 B5_N1 PIN_G8 2.5 V (default) 8mA (default) 2 (default)
b3 Output PIN_u21 5 B5_N0 PIN_D11 2.5 V (default) 8mA (default) 2 (default)
c0 Output PIN_e17 7 B7_N2 PIN_C15 2.5 V (default) 8mA (default) 2 (default)
c1 Output PIN_w21 5 B5_N1 PIN_B10 2.5 V (default) 8mA (default) 2 (default)
c2 Output PIN_y25 5 B5_N1 PIN_E7 2.5 V (default) 8mA (default) 2 (default)
c3 Output PIN_ab20 4 B4_N0 PIN_G10 2.5 V (default) 8mA (default) 2 (default)
clear Input PIN_y24 5 B5_N2 PIN_G13 2.5 V (default) 8mA (default)
clk Input PIN_m23 6 B6_N2 PIN_J1 2.5 V (default) 8mA (default)
d0 Output PIN_l26 6 B6_N1 PIN_F15 2.5 V (default) 8mA (default) 2 (default)
d1 Output PIN_w22 5 B5_N0 PIN_H13 2.5 V (default) 8mA (default) 2 (default)
d2 Output PIN_w26 5 B5_N1 PIN_C8 2.5 V (default) 8mA (default) 2 (default)
d3 Output PIN_aa21 4 B4_N0 PIN_H12 2.5 V (default) 8mA (default) 2 (default)
dividend[7] Input PIN_aa22 5 B5_N2 PIN_J10 2.5 V (default) 8mA (default)
dividend[6] Input PIN_aa23 5 B5_N2 PIN_G12 2.5 V (default) 8mA (default)
dividend[5] Input PIN_aa24 5 B5_N2 PIN_A7 2.5 V (default) 8mA (default)
dividend[4] Input PIN_ab23 5 B5_N2 PIN_H10 2.5 V (default) 8mA (default)
dividend[3] Input PIN_ab24 5 B5_N2 PIN_E11 2.5 V (default) 8mA (default)
dividend[2] Input PIN_ac24 5 B5_N2 PIN_B7 2.5 V (default) 8mA (default)
dividend[1] Input PIN_ab25 5 B5_N1 PIN_J27 2.5 V (default) 8mA (default)
dividend[0] Input PIN_ac25 5 B5_N2 PIN_J28 2.5 V (default) 8mA (default)
divisor[7] Input PIN_ab26 5 B5_N1 PIN_F14 2.5 V (default) 8mA (default)
divisor[6] Input PIN_ad26 5 B5_N2 PIN_H14 2.5 V (default) 8mA (default)
divisor[5] Input PIN_ac26 5 B5_N2 PIN_A17 2.5 V (default) 8mA (default)
divisor[4] Input PIN_ab27 5 B5_N1 PIN_J14 2.5 V (default) 8mA (default)
divisor[3] Input PIN_ad27 5 B5_N2 PIN_C13 2.5 V (default) 8mA (default)
divisor[2] Input PIN_ac27 5 B5_N2 PIN_D14 2.5 V (default) 8mA (default)
divisor[1] Input PIN_ac28 5 B5_N2 PIN_D13 2.5 V (default) 8mA (default)
divisor[0] Input PIN_ab28 5 B5_N1 PIN_A12 2.5 V (default) 8mA (default)
All Pins


Pin Planner - C:/Users/LAB 1222/Desktop/course/divider - divider
File Edit View Processing Tools Window Help
Report
Report not available
Groups Report
Tasks
Early Pin Planning
Early Pin Planning...
Pin Legend
Symbol Pin Type
User I/O
User assigned l...
Fitter assigned l...
Unbonded pad
Reserved pin
Other configura...
DEV_OE
DEV_CLR
Named: * Edit:
Filter: Pins: all
Node Name Direction Location I/O Bank VREF Group Fitter Location I/O Standard Reserved Current Strength Slew Rate Differential Pair Strict Preservation
divisor[1] Input PIN_ac28 5 B5_N2 PIN_D13 2.5 V (default) 8mA (default)
divisor[0] Input PIN_ab28 5 B5_N1 PIN_A12 2.5 V (default) 8mA (default)
e0 Output PIN_l25 6 B6_N1 PIN_H15 2.5 V (default) 8mA (default) 2 (default)
e1 Output PIN_w25 5 B5_N1 PIN_J12 2.5 V (default) 8mA (default) 2 (default)
e2 Output PIN_y26 5 B5_N1 PIN_D7 2.5 V (default) 8mA (default) 2 (default)
e3 Output PIN_ad24 4 B4_N0 PIN_F10 2.5 V (default) 8mA (default) 2 (default)
f0 Output PIN_j22 6 B6_N0 PIN_D15 2.5 V (default) 8mA (default) 2 (default)
f1 Output PIN_U23 5 B5_N1 PIN_C10 2.5 V (default) 8mA (default) 2 (default)
f2 Output PIN_w27 5 B5_N1 PIN_C7 2.5 V (default) 8mA (default) 2 (default)
f3 Output PIN_af23 4 B4_N0 PIN_G11 2.5 V (default) 8mA (default) 2 (default)
g0 Output PIN_h22 6 B6_N0 PIN_B17 2.5 V (default) 8mA (default) 2 (default)
g1 Output PIN_u24 5 B5_N0 PIN_J13 2.5 V (default) 8mA (default) 2 (default)
g2 Output PIN_w28 5 B5_N1 PIN_D6 2.5 V (default) 8mA (default) 2 (default)
g3 Output PIN_y19 4 B4_N0 PIN_C11 2.5 V (default) 8mA (default) 2 (default)
output[2] Output PIN_e25 7 B7_N1 PIN_F12 2.5 V (default) 8mA (default) 2 (default)
output[1] Output PIN_e22 7 B7_N0 PIN_F11 2.5 V (default) 8mA (default) 2 (default)
output[0] Output PIN_e21 7 B7_N0 PIN_G14 2.5 V (default) 8mA (default) 2 (default)
remainder[15] Output PIN_g15 7 B7_N2 PIN_A11 2.5 V (default) 8mA (default) 2 (default)
remainder[14] Output PIN_f15 7 B7_N2 PIN_E14 2.5 V (default) 8mA (default) 2 (default)
remainder[13] Output PIN_h17 7 B7_N2 PIN_B11 2.5 V (default) 8mA (default) 2 (default)
remainder[12] Output PIN_j16 7 B7_N2 PIN_J15 2.5 V (default) 8mA (default) 2 (default)
remainder[11] Output PIN_h16 7 B7_N2 PIN_D16 2.5 V (default) 8mA (default) 2 (default)
remainder[10] Output PIN_j15 7 B7_N2 PIN_C12 2.5 V (default) 8mA (default) 2 (default)
remainder[9] Output PIN_g17 7 B7_N1 PIN_D12 2.5 V (default) 8mA (default) 2 (default)
remainder[8] Output PIN_j17 7 B7_N2 PIN_C14 2.5 V (default) 8mA (default) 2 (default)
remainder[7] Output PIN_h19 7 B7_N2 PIN_E12 2.5 V (default) 8mA (default) 2 (default)
remainder[6] Output PIN_j19 7 B7_N2 PIN_D9 2.5 V (default) 8mA (default) 2 (default)
remainder[5] Output PIN_e18 7 B7_N1 PIN_B6 2.5 V (default) 8mA (default) 2 (default)
remainder[4] Output PIN_f18 7 B7_N1 PIN_C9 2.5 V (default) 8mA (default) 2 (default)
remainder[3] Output PIN_f21 7 B7_N0 PIN_B8 2.5 V (default) 8mA (default) 2 (default)
remainder[2] Output PIN_e19 7 B7_N0 PIN_E10 2.5 V (default) 8mA (default) 2 (default)
remainder[1] Output PIN_f19 7 B7_N0 PIN_A8 2.5 V (default) 8mA (default) 2 (default)
remainder[0] Output PIN_g19 7 B7_N2 PIN_G9 2.5 V (default) 8mA (default) 2 (default)
<<new node>>
All Pins

(4)　確認接線於正確腳位



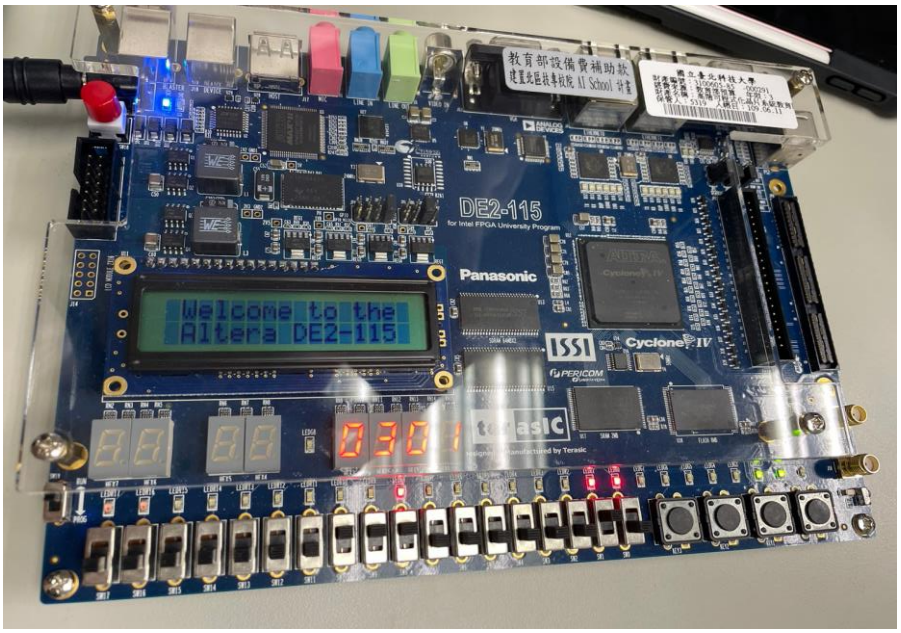
(5)　燒錄視窗設定及燒錄成功畫面



（五） 實驗結果

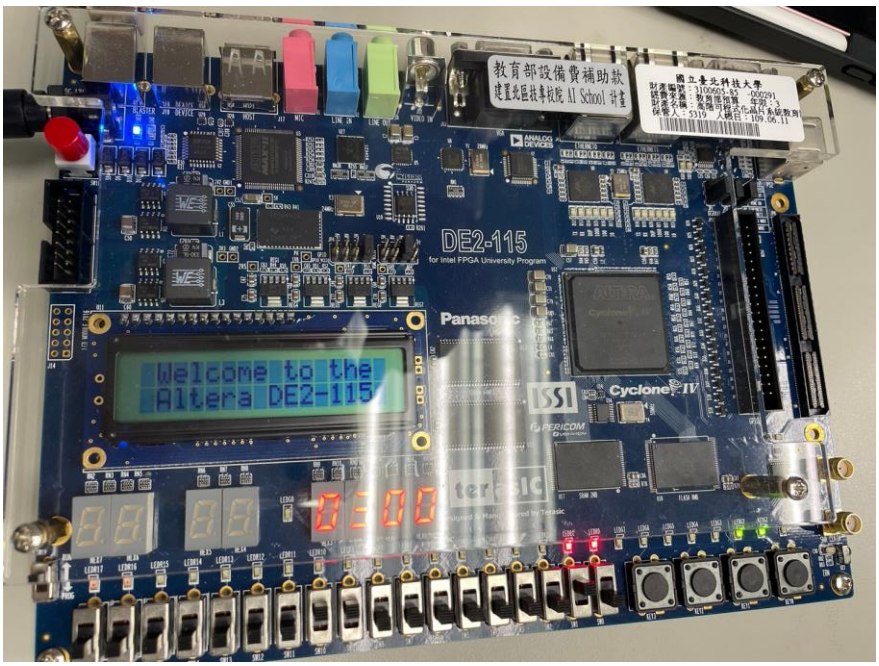
(1) 7 除以 2

輸出結果 Q: 3, R: 1



(2) 6 除以 2

Q: 3, R: 0



● 實際操作影片連結；

https://drive.google.com/file/d/1H41QsL72ab0y5Kg2CDLStdPW6-VORXHp/view?usp=drive_link

三、程式碼

divider.vhd

```
LIBRARY IEEE;

USE IEEE.STD_LOGIC_1164.ALL;

USE IEEE.STD_LOGIC_UNSIGNED.ALL;

USE work.course7_package.all;



ENTITY divider IS

 PORT( clk, clear: IN STD_LOGIC;

   divisor, dividend: IN STD_LOGIC_VECTOR(7 downto 0);

   remainder: BUFFER STD_LOGIC_VECTOR(15 DOWNTO 0);

   a0, b0, c0, d0, e0, f0, g0, a1, b1, c1, d1, e1, f1, g1, a2, b2, c2, d2, e2, f2, g2, a3, b3, c3, d3, e3, f
3, g3: OUT std_logic;

   output: buffer STD_LOGIC_VEcTOR(2 downto 0)

   );

END divider;
```

```
architecture main of divider is
 signal w : STD_LOGIC :='0';
 signal re : INTEGER:= 0;
 signal run : std_logic;
 signal temp_s, temp_p: STD_LOGIC_VECTOR(15 downto 0);

begin

 PROCESS
 begin
  WAIT UNTIL Clk'EVENT AND clk = '1';
  if clear = '1' then
   output <= "100";
  else
   Case output is
    when "000" =>
     output <= "111";
```

```
when "111" =>
 output <= "001";

when "001" =>
 if w = '1' then
output <= "011";
 else
output <= "010";
 end if;

when "011" =>
 if w = '1' then
output <= "101";
 else
output <= "001";
 end if;

when "010" =>
 if w = '1' then
```

```
   output <= "101";
    else
   output <= "001";
    end if;

   when "100"=>
   output <= "000";

   when others =>
   output <= "110";

   end Case;
 end if;
end PROCESS;

case3: temp_s <= (( remainder(15 downto 8) - divisor) & remainder(7 downto 0));
case4: temp_p <= (( remainder(15 downto 8) + divisor) & remainder(7 downto 0));

output_select: process
```

```
begin
 WAIT UNTIL Clk'EVENT AND clk = '1';
 case output is
  when "000" =>
  remainder <= ("00000000" & dividend);

  when "111" =>
   for_1: FOR i IN 14 downto 0 loop
       remainder(i + 1) <= remainder(i);
    END loop;
    remainder(0) <= '0';

   when "001" =>
    remainder <= (( remainder(15 downto 8) - divisor) & remainder(7 downto 0));

   when "011" =>
    for_2: FOR i IN 14 downto 0 loop
       remainder(i + 1) <= remainder(i);
    END loop;
```

```
  remainder(0) <= '1';


when "010" =>
 for_3: FOR i IN 14 downto 0 loop
    remainder(i + 1) <= temp_p(i);
  END loop;
  remainder(0) <= '0';


when "100"=>
remainder <= "0000000000000000";


when "101" =>
for_r: FOR i IN 8 to 14 loop
    remainder(i) <= remainder(i + 1);
  END loop;
  remainder(15) <= '0';
remainder(7 downto 0) <= remainder(7 downto 0);


when others =>
```

```
   remainder <= remainder;



 end Case;

end process;



count:process

begin

 WAIT UNTIL Clk'EVENT AND clk = '1';

 if clear = '1' then

  re <= 0;

 elsif output = "001" and run = '1' then

  re <= re + 1;

 else

  re <= re;

 end if;

end process;

run <= '0' when re = 8 else '1';



with output select
```

```
  w <= not temp_s(15) when "001",
   not run when "011",
   not run when "010",
   '0' when others;

 show: seven_segment PORT MAP( remainder(11),remainder(10),remainder(9),remainder(8),  re
mainder(15), remainder(14),remainder(13),remainder(12), remainder(3), remainder(2), remainder
(1),remainder(0), remainder(7), remainder(6),remainder(5),remainder(4),         a0, b0, c0, d0, e0, f
0, g0, a1, b1, c1, d1, e1, f1, g1, a2, b2, c2, d2, e2, f2, g2, a3, b3, c3, d3, e3, f3, g3);
end main;
```

package. vhd

```
LIBRARY ieee;

USE ieee.std_logic_1164.all;



PACKAGE course7_package IS

        component seven_segment

                PORT( W0, X0, Y0, Z0,

                                W1, X1, Y1, Z1,

                                W2, X2, Y2, Z2,

                                W3, X3, Y3, Z3          : IN STD_LOGIC;

                                a0, b0, c0, d0, e0, f0, g0,

                                a1, b1, c1, d1, e1, f1, g1,

                                a2, b2, c2, d2, e2, f2, g2,

                                a3, b3, c3, d3, e3, f3, g3: OUT STD_LOGIC);

        END component seven_segment;

END course7_package;
```

seven_segment.vhd

```
Library ieee;

USE ieee.std_logic_1164.all;



ENTITY seven_segment IS

        PORT( W0, X0, Y0, Z0,

                W1, X1, Y1, Z1,

                    W2, X2, Y2, Z2,

                W3, X3, Y3, Z3      : IN STD_LOGIC;

            a0, b0, c0, d0, e0, f0, g0,

                    a1, b1, c1, d1, e1, f1, g1,

                    a2, b2, c2, d2, e2, f2, g2,

                    a3, b3, c3, d3, e3, f3, g3: OUT STD_LOGIC);

END seven_segment;



ARCHITECTURE LogicFunc OF seven_segment IS

BEGIN

        a0 <= (NOT W0 AND NOT X0 AND NOT Y0 AND Z0)
```

```
                OR (NOT W0 AND X0 AND NOT Y0 AND NOT Z0)

                OR (W0 AND NOT X0 AND Y0 AND Z0)

                OR (W0 AND X0 AND NOT Y0);

b0 <= (NOT W0 AND X0 AND NOT Y0 AND Z0)

                OR (NOT W0 AND X0 AND Y0 AND NOT Z0)

                OR (W0 AND NOT X0 AND Y0 AND Z0)

                OR (W0 AND X0 AND NOT Z0)

                OR (W0 AND X0 AND Y0);

c0 <= (NOT W0 AND NOT X0 AND Y0 AND NOT Z0)

                OR (W0 AND X0 AND NOT Z0)

                OR (W0 AND X0 AND Y0);

d0 <= (NOT X0 AND NOT Y0 AND Z0)

                OR (NOT W0 AND X0 AND NOT Y0 AND NOT Z0)

                OR (X0 AND Y0 AND Z0)

                OR (W0 AND NOT X0 AND Y0 AND NOT Z0);

e0 <= (NOT W0 AND Z0)

                OR (NOT W0 AND X0 AND NOT Y0)

                OR (NOT X0 AND NOT Y0 AND Z0);

f0 <= (NOT W0 AND NOT X0 AND Z0)
```

```
                OR (NOT W0 AND NOT X0 AND Y0)

                OR (NOT W0 AND Y0 AND Z0)

                OR (W0 AND X0 AND NOT Y0);

g0 <= (NOT W0 AND NOT X0 AND NOT Y0)

                OR (NOT W0 AND X0 AND Y0 AND Z0);


a1 <= (NOT W1 AND NOT X1 AND NOT Y1 AND Z1)

                OR (NOT W1 AND X1 AND NOT Y1 AND NOT Z1)

                OR (W1 AND NOT X1 AND Y1 AND Z1)

                OR (W1 AND X1 AND NOT Y1);

b1 <= (NOT W1 AND X1 AND NOT Y1 AND Z1)

                OR (NOT W1 AND X1 AND Y1 AND NOT Z1)

                OR (W1 AND NOT X1 AND Y1 AND Z1)

                OR (W1 AND X1 AND NOT Z1)

                OR (W1 AND X1 AND Y1);

c1 <= (NOT W1 AND NOT X1 AND Y1 AND NOT Z1)

                OR (W1 AND X1 AND NOT Z1)

                OR (W1 AND X1 AND Y1);

d1 <= (NOT X1 AND NOT Y1 AND Z1)
```

```
                OR (NOT W1 AND X1 AND NOT Y1 AND NOT Z1)

                OR (X1 AND Y1 AND Z1)

                OR (W1 AND NOT X1 AND Y1 AND NOT Z1);

e1 <= (NOT W1 AND Z1)

                OR (NOT W1 AND X1 AND NOT Y1)

                OR (NOT X1 AND NOT Y1 AND Z1);

f1 <= (NOT W1 AND NOT X1 AND Z1)

                OR (NOT W1 AND NOT X1 AND Y1)

                OR (NOT W1 AND Y1 AND Z1)

                OR (W1 AND X1 AND NOT Y1);

g1 <= (NOT W1 AND NOT X1 AND NOT Y1)

                OR (NOT W1 AND X1 AND Y1 AND Z1);


a2 <= (NOT W2 AND NOT X2 AND NOT Y2 AND Z2)

                OR (NOT W2 AND X2 AND NOT Y2 AND NOT Z2)

                OR (W2 AND NOT X2 AND Y2 AND Z2)

                OR (W2 AND X2 AND NOT Y2);

b2 <= (NOT W2 AND X2 AND NOT Y2 AND Z2)

                OR (NOT W2 AND X2 AND Y2 AND NOT Z2)
```

```
                OR (W2 AND NOT X2 AND Y2 AND Z2)

                OR (W2 AND X2 AND NOT Z2)

                OR (W2 AND X2 AND Y2);

c2 <= (NOT W2 AND NOT X2 AND Y2 AND NOT Z2)

                OR (W2 AND X2 AND NOT Z2)

                OR (W2 AND X2 AND Y2);

d2 <= (NOT X2 AND NOT Y2 AND Z2)

                OR (NOT W2 AND X2 AND NOT Y2 AND NOT Z2)

                OR (X2 AND Y2 AND Z2)

                OR (W2 AND NOT X2 AND Y2 AND NOT Z2);

e2 <= (NOT W2 AND Z2)

                OR (NOT W2 AND X2 AND NOT Y2)

                OR (NOT X2 AND NOT Y2 AND Z2);

f2 <= (NOT W2 AND NOT X2 AND Z2)

                OR (NOT W2 AND NOT X2 AND Y2)

                OR (NOT W2 AND Y2 AND Z2)

                OR (W2 AND X2 AND NOT Y2);

g2 <= (NOT W2 AND NOT X2 AND NOT Y2)

                OR (NOT W2 AND X2 AND Y2 AND Z2);
```

```
a3 <= (NOT W3 AND NOT X3 AND NOT Y3 AND Z3)
        OR (NOT W3 AND X3 AND NOT Y3 AND NOT Z3)
        OR (W3 AND NOT X3 AND Y3 AND Z3)
        OR (W3 AND X3 AND NOT Y3);
b3 <= (NOT W2 AND X2 AND NOT Y3 AND Z3)
        OR (NOT W3 AND X3 AND Y3 AND NOT Z3)
        OR (W3 AND NOT X3 AND Y3 AND Z3)
        OR (W3 AND X3 AND NOT Z3)
        OR (W3 AND X3 AND Y3);
c3 <= (NOT W3 AND NOT X3 AND Y3 AND NOT Z3)
        OR (W3 AND X3 AND NOT Z3)
        OR (W3 AND X3 AND Y3);
d3 <= (NOT X3 AND NOT Y3 AND Z3)
        OR (NOT W3 AND X3 AND NOT Y3 AND NOT Z3)
        OR (X3 AND Y3 AND Z3)
        OR (W3 AND NOT X3 AND Y3 AND NOT Z3);
e3 <= (NOT W3 AND Z3)
        OR (NOT W3 AND X3 AND NOT Y3)
```

```
                    OR (NOT X3 AND NOT Y3 AND Z3);

    f3 <= (NOT W3 AND NOT X3 AND Z3)

                    OR (NOT W3 AND NOT X3 AND Y3)

                    OR (NOT W3 AND Y3 AND Z3)

                    OR (W3 AND X3 AND NOT Y3);

    g3 <= (NOT W3 AND NOT X3 AND NOT Y3)

                    OR (NOT W3 AND X3 AND Y3 AND Z3);


END LogicFunc;
```