微算機系統

小組專案報告

實驗一：七段顯示器解碼電路

組別： 20

班級、姓名與學號：

醫工三 葉芸茜 B812110004

醫工三 湯青秀 B812110011

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一、實驗內容：

（一）基本題

透過Modelsim進行模擬輸入輸出W、X、Y、Z、a、b、c、d、e、 f和g，在燒入開發板用指撥開關（4個Switch）控制七段顯示器顯 示0 ~ F之間任意數字。

Variable	Pin Location	Signal Name
Z	PIN_AB28	SW[0]
Y	PIN_AC28	SW[1]
X	PIN_AC27	SW[2]
W	PIN_AD27	SW[3]
a	PIN_G18	HEX0[0]
b	PIN_F22	HEX0[1]
c	PIN_E17	HEX0[2]
d	PIN_L26	HEX0[3]
e	PIN_L25	HEX0[4]
f	PIN_J22	HEX0[5]
g	PIN_H22	HEX0[6]

（二）加分題

透過指撥開關控制七段顯示器顯示0 ~ FFF之間任意數字 （百位數、十位數、個位數分開輸入，共12個Switch）。

Variable	Pin Location	Signal Name	Variable	Pin Location	Signal Name
Z0	PIN_AB28	SW[0]	a0	PIN_G18	HEX0[0]
Y0	PIN_AC28	SW[1]	b0	PIN_F22	HEX0[1]
X0	PIN_AC27	SW[2]	c0	PIN_E17	HEX0[2]
W0	PIN_AD27	SW[3]	d0	PIN_L26	HEX0[3]
			e0	PIN_L25	HEX0[4]
			f0	PIN_J22	HEX0[5]
			g0	PIN_H22	HEX0[6]
Z1	PIN_AB27	SW[4]	a1	PIN_M24	HEX1[0]
Y1	PIN_AC26	SW[5]	b1	PIN_Y22	HEX1[1]
X1	PIN_AD26	SW[6]	c1	PIN_W21	HEX1[2]
W1	PIN_AB26	SW[7]	d1	PIN_W22	HEX1[3]
			e1	PIN_W25	HEX1[4]
			f1	PIN_U23	HEX1[5]
			g1	PIN_U24	HEX1[6]
Z2	PIN_AC25	SW[8]	a2	PIN_AA25	HEX2[0]
Y2	PIN_AB25	SW[9]	b2	PIN_AA26	HEX2[1]
X2	PIN_AC24	SW[10]	c2	PIN_Y25	HEX2[2]
W2	PIN_AB24	SW[11]	d2	PIN_W26	HEX2[3]
			e2	PIN_Y26	HEX2[4]
			f2	PIN_W27	HEX2[5]
			g2	PIN_W28	HEX2[6]

二、實驗過程及結果：

（一）預期實驗結果的真值表

數字	W	X	Y	Z	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	1	0	0	1	1	1	1
2	0	0	1	0	0	0	1	0	0	1	0
3	0	0	1	1	0	0	0	0	1	1	0
4	0	1	0	0	1	0	0	1	1	0	0
5	0	1	0	1	0	1	0	0	1	0	0
6	0	1	1	0	0	1	0	0	0	0	0
7	0	1	1	1	0	0	0	1	1	1	1
8	1	0	0	0	0	0	0	0	0	0	0
9	1	0	0	1	0	0	0	1	1	0	0
A	1	0	1	0	0	0	0	1	0	0	0
B	1	0	1	1	1	1	0	0	0	0	0
C	1	1	0	0	1	1	1	0	0	1	0
D	1	1	0	1	1	0	0	0	0	1	0
E	1	1	1	0	0	1	1	0	0	0	0
F	1	1	1	1	0	1	1	1	0	0	0

（二）根據上方真值表輸出布林代數並化簡

a = $\overline{W}\,\overline{X}\,\overline{Y}\,Z + \overline{W}\,X\,\overline{Y}\,\overline{Z} + W\,\overline{X}\,Y\,Z + W\,X\,\overline{Y}$

b = $\overline{W}\,X\,\overline{Y}\,Z + \overline{W}\,X\,Y\,\overline{Z} + W\,\overline{X}\,Y\,Z + W\,X\,\overline{Z} + W\,X\,Y$

c = $\overline{W}\,\overline{X}\,Y\,\overline{Z} + W\,X\,\overline{Z} + W\,X\,Y$

d = $\overline{X}\,\overline{Y}\,Z + \overline{W}\,X\,\overline{Y}\,\overline{Z} + X\,Y\,Z + W\,\overline{X}\,Y\,\overline{Z}$

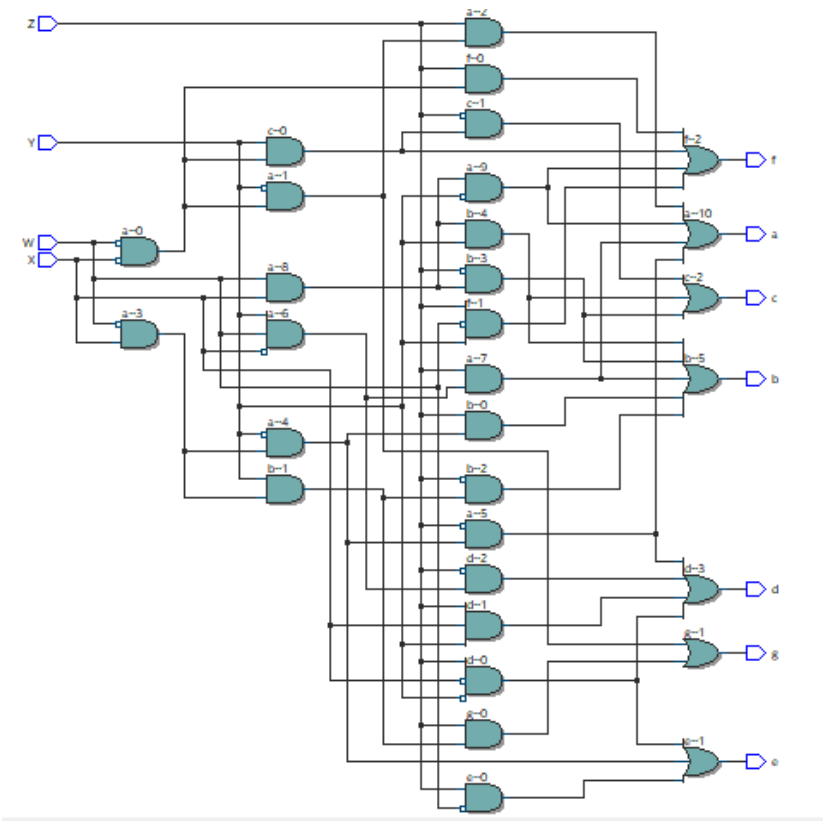
e = $\overline{W}\,Z + \overline{W}\,X\,\overline{Y} + \overline{X}\,\overline{Y}\,Z$

f = $\overline{W}\,\overline{X}\,Z + \overline{W}\,\overline{X}\,Y + \overline{W}\,Y\,Z + W\,X\,\overline{Y}$

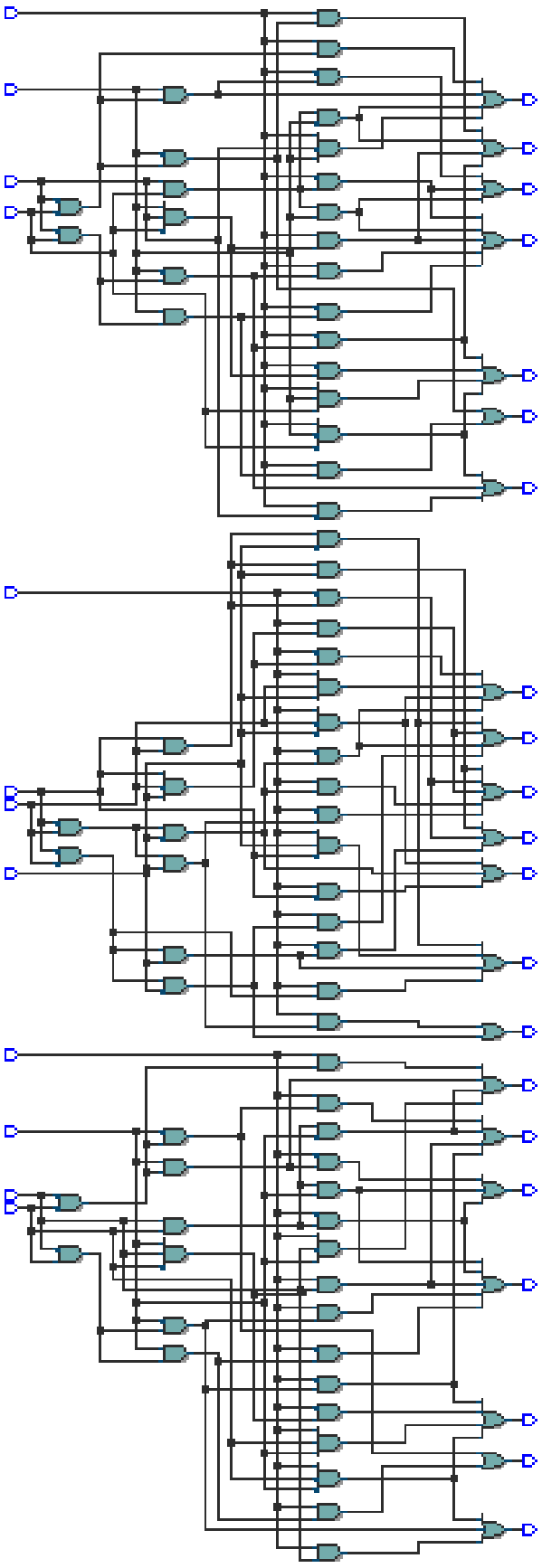
g = $\overline{W}\,\overline{X}\,\overline{Y} + \overline{W}\,X\,Y\,Z$

（三）布林代數化簡後設計出的電路

1. 基本題

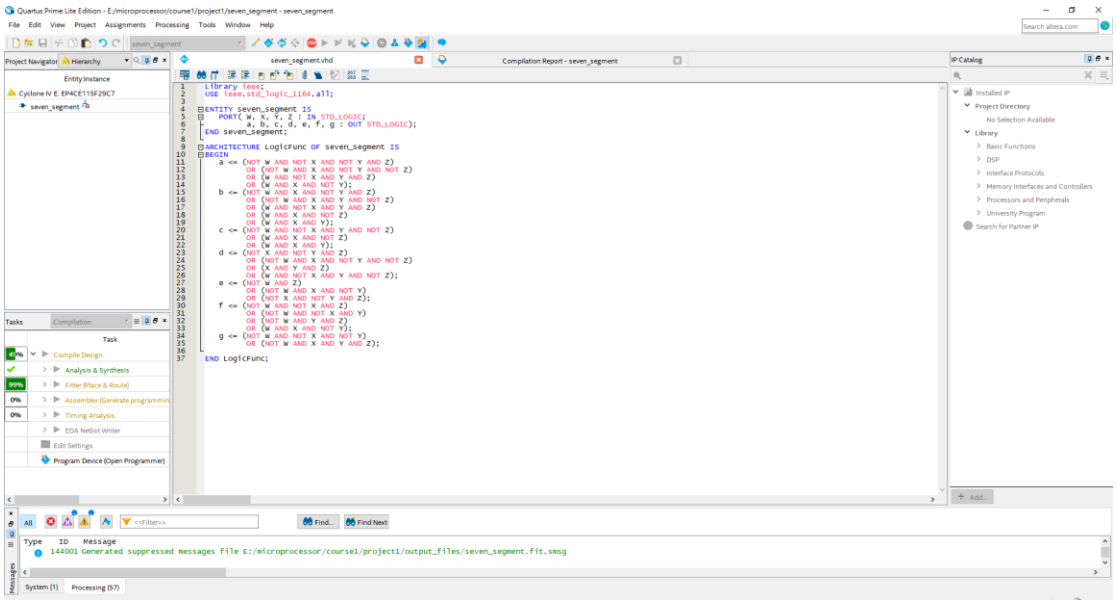


2. 加分題

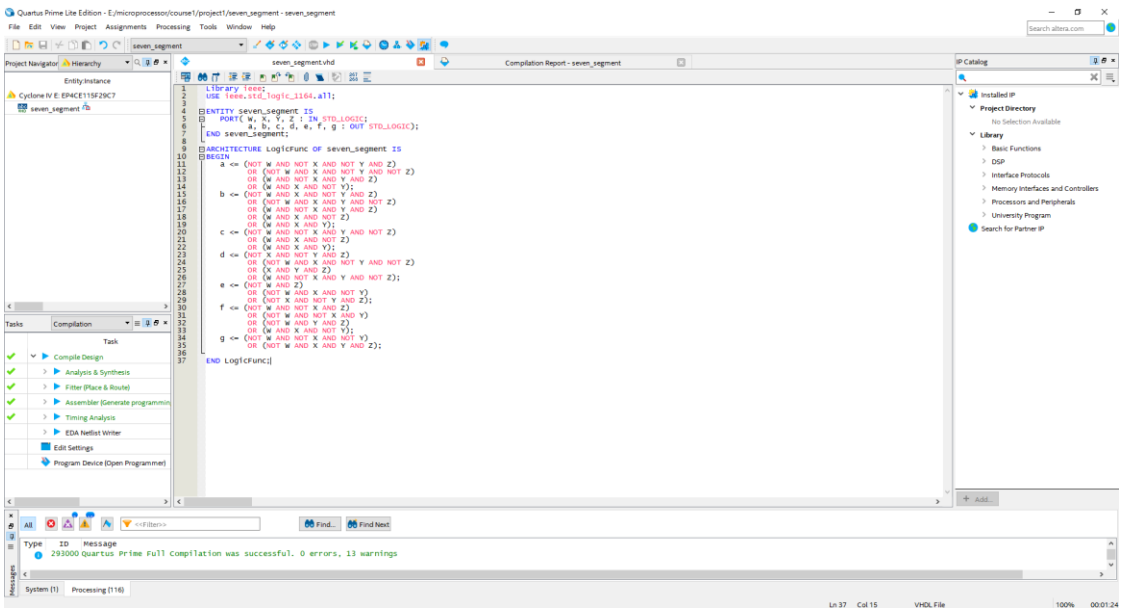


（四）實驗過程

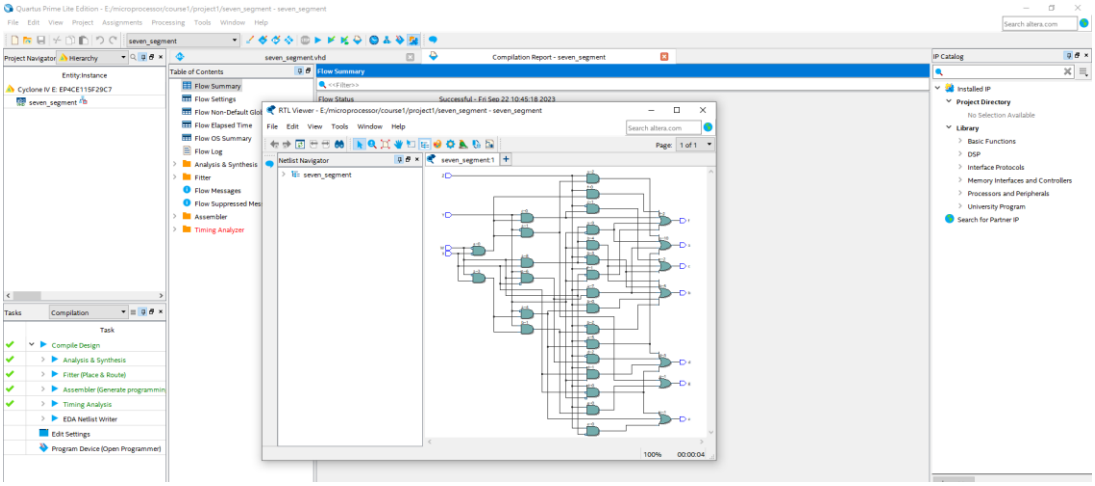
1. 撰寫程式碼



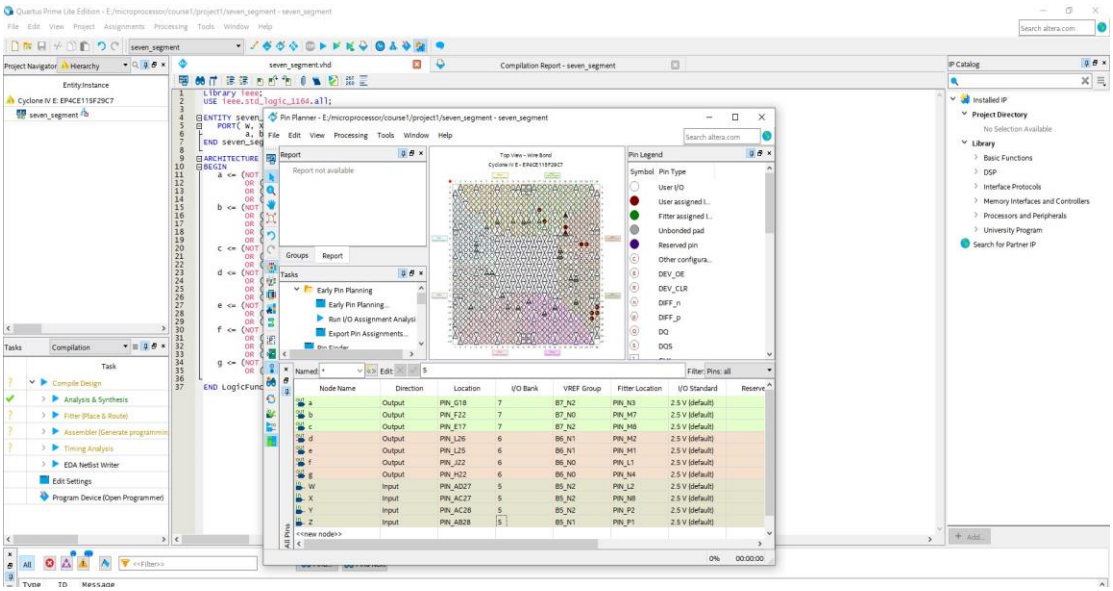
2. 編譯成功



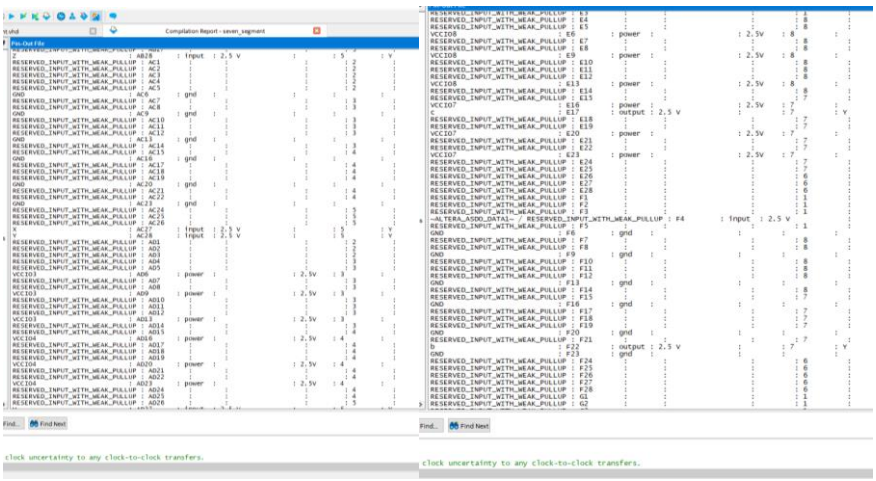
3. 電路圖



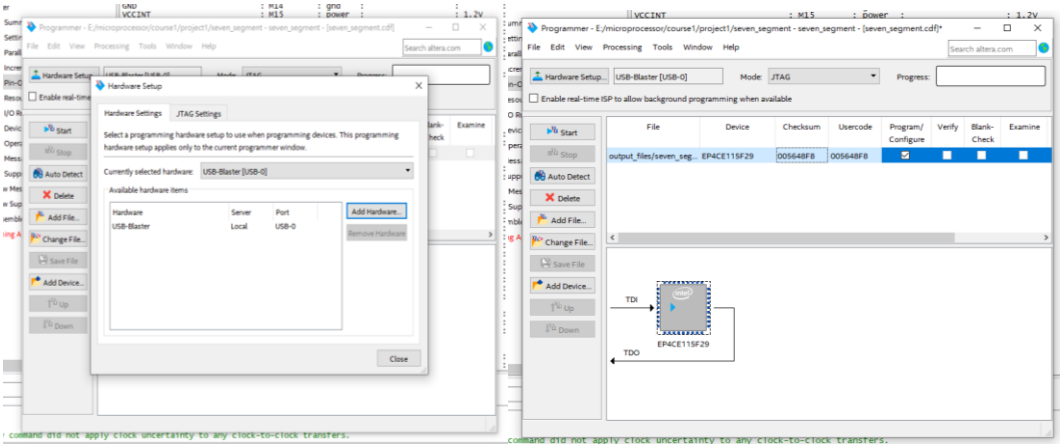
4. 接腳位

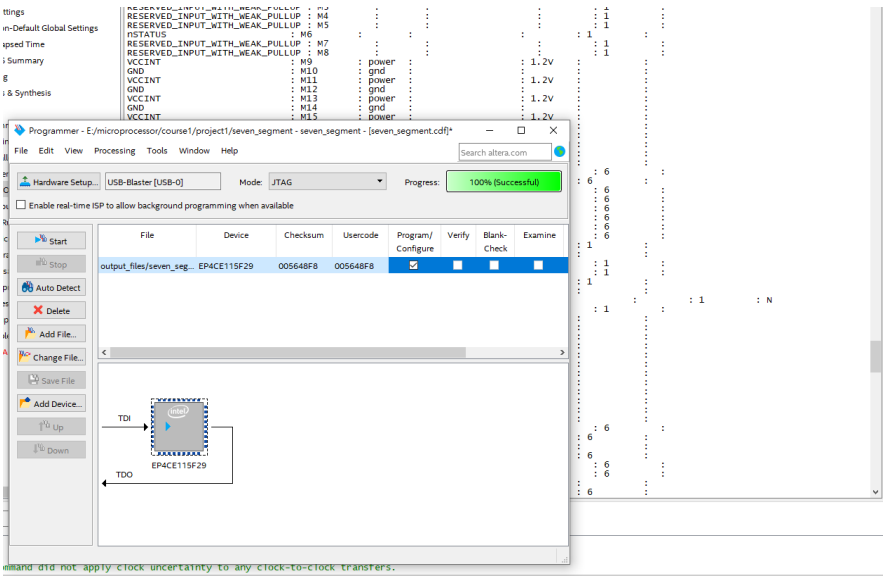


5. 確認接線於設定腳位

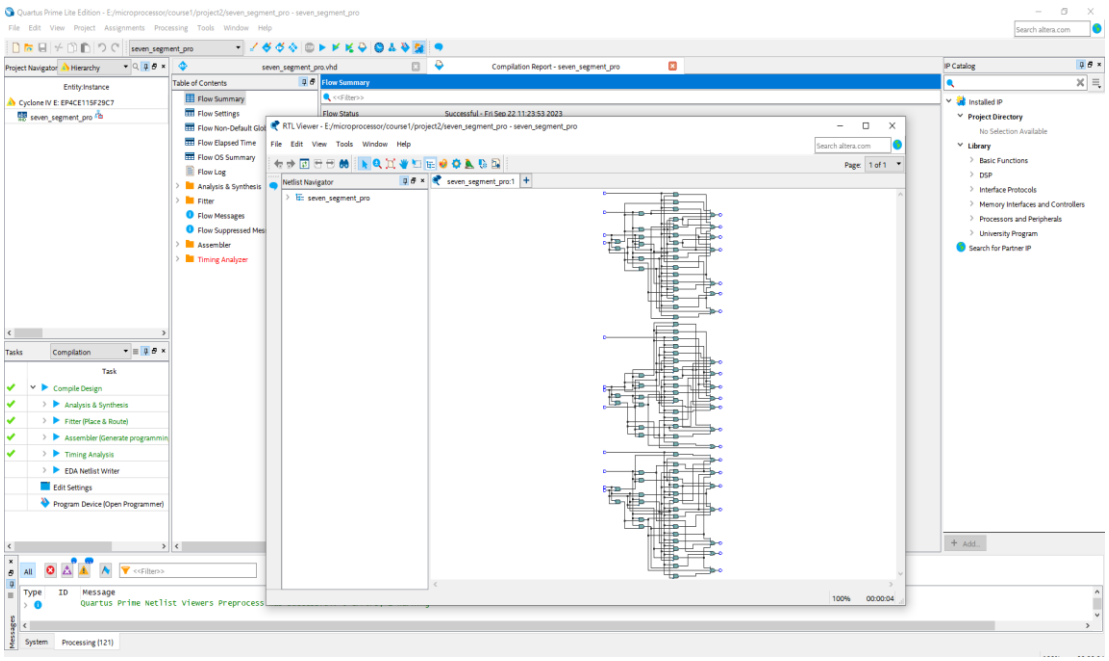


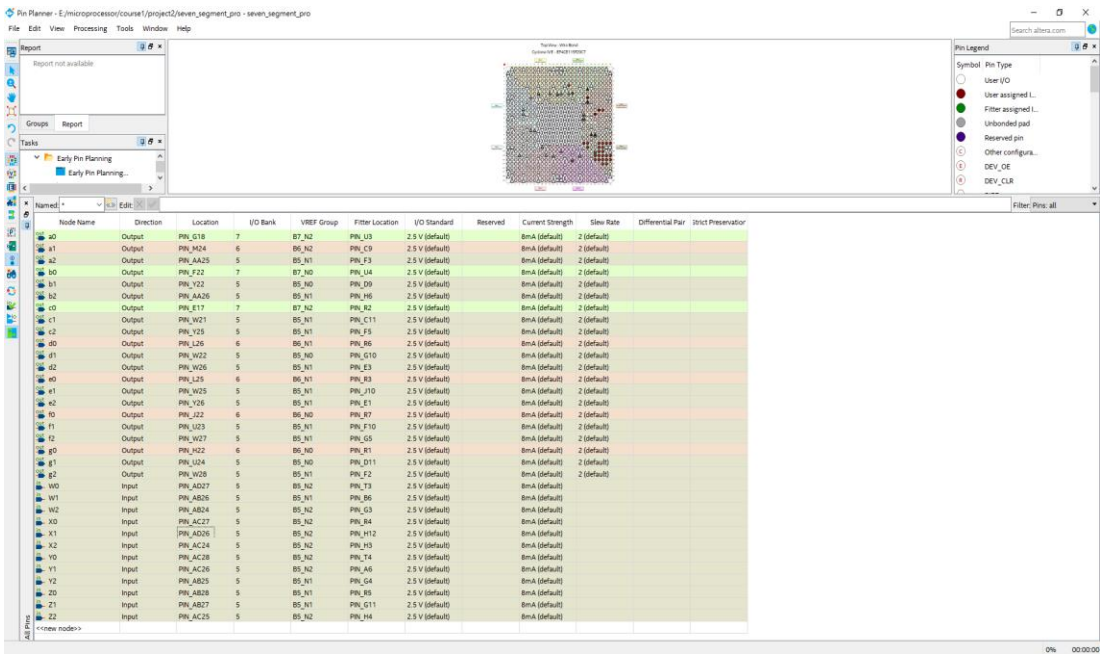
6. 燒錄視窗設定及燒錄成功畫面

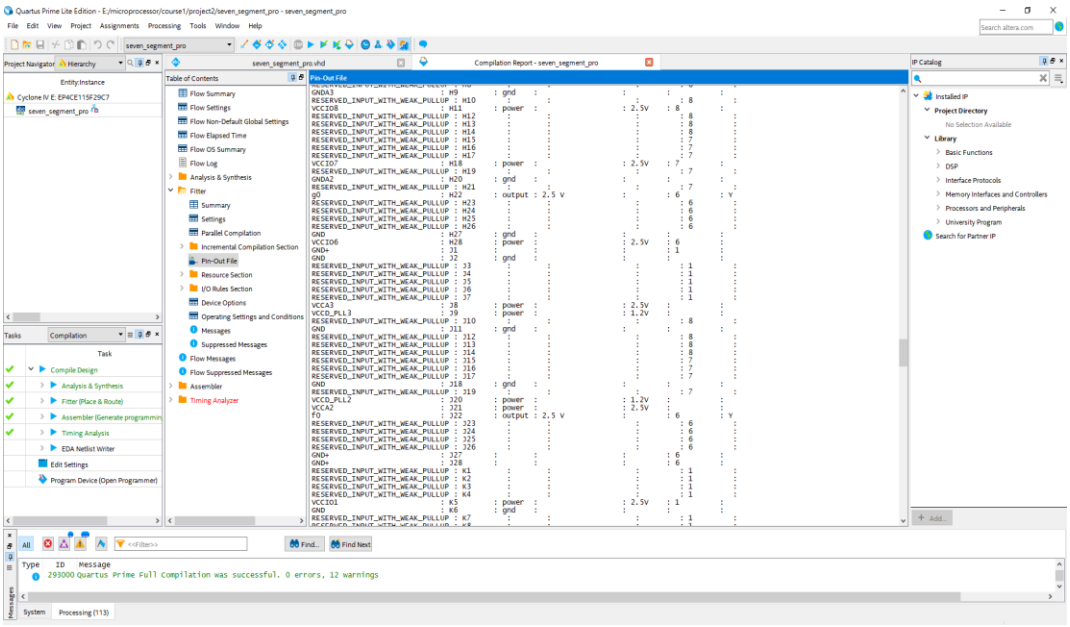


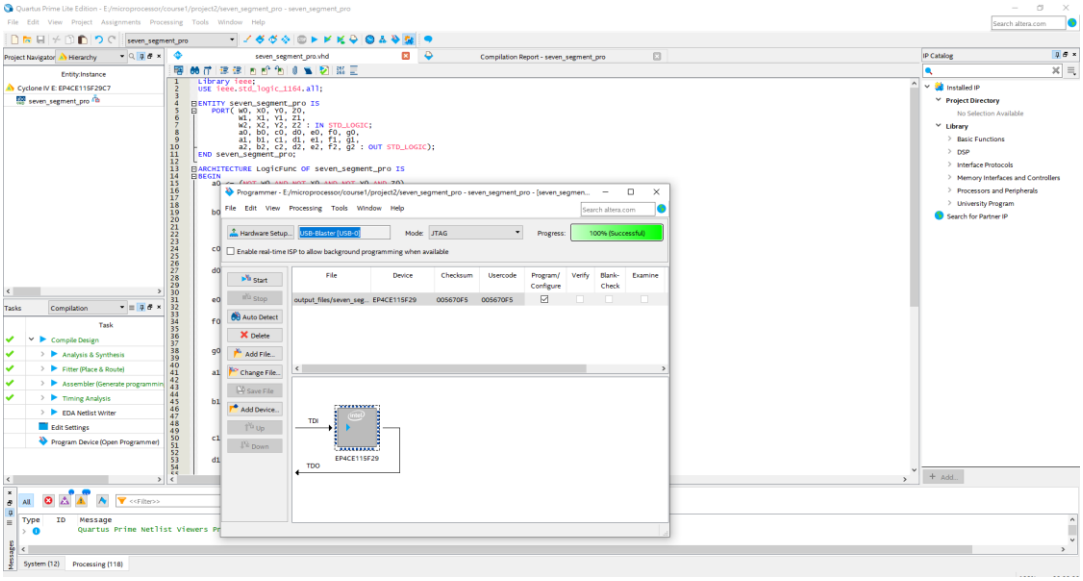


7. 加分題操作過程







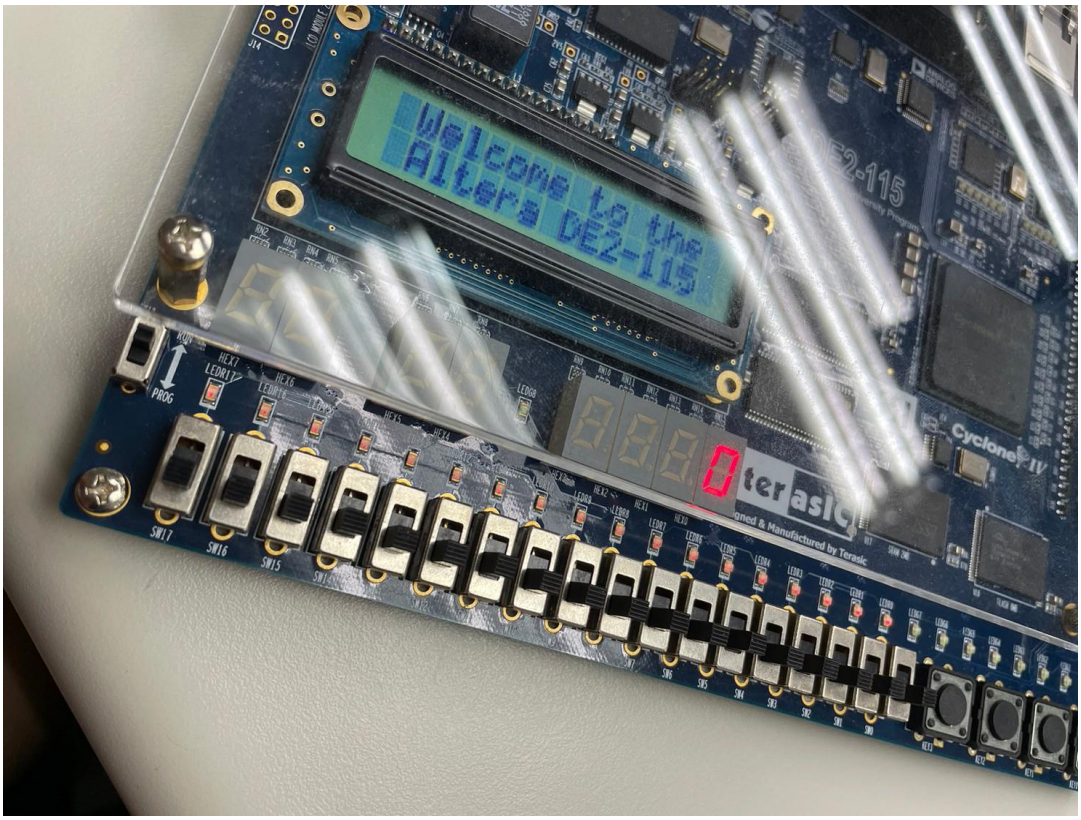


（五）實驗結果

1. 基本題

W, X, Y, Z = 0 0 0 0

輸出為 0



2. 加分題

（1） W0, X0, Y0, Z0 = 1 1 1 1

W1, X1, Y1, Z1 = 1 0 1 0

W2, X2, Y2, Z2 = 1 1 1 1

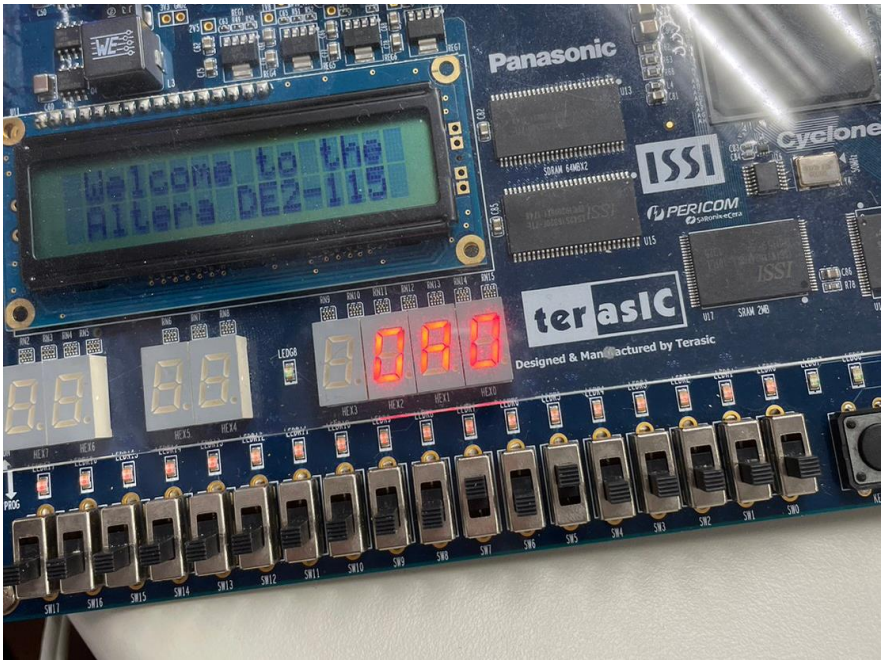
輸出為 FAF

(2) W0, X0, Y0, Z0 = 0 0 0 0

W1, X1, Y1, Z1 = 1 0 1 0

W2, X2, Y2, Z2 = 0 0 0 0

輸出為 0A0



實際操作影片連結；https://drive.google.com/drive/folders/1-TE977VAXFRKDgSP9XgpqGfFPB2IZR2i?usp=drive_link

三、程式碼

基本題

```
Library ieee;
USE ieee.std_logic_1164.all;


ENTITY seven_segment IS
  PORT( W, X, Y, Z : IN STD_LOGIC;
        a, b, c, d, e, f, g : OUT STD_LOGIC);
END seven_segment;


ARCHITECTURE LogicFunc OF seven_segment IS
BEGIN
  a <= (NOT W AND NOT X AND NOT Y AND Z)
                OR (NOT W AND X AND NOT Y AND NOT Z)
                OR (W AND NOT X AND Y AND Z)
                OR (W AND X AND NOT Y);
  b <= (NOT W AND X AND NOT Y AND Z)
                OR (NOT W AND X AND Y AND NOT Z)
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```
                OR (W AND NOT X AND Y AND Z)

                OR (W AND X AND NOT Z)

                OR (W AND X AND Y);

c <= (NOT W AND NOT X AND Y AND NOT Z)

                OR (W AND X AND NOT Z)

                OR (W AND X AND Y);

d <= (NOT X AND NOT Y AND Z)

                OR (NOT W AND X AND NOT Y AND NOT Z)

                OR (X AND Y AND Z)

                OR (W AND NOT X AND Y AND NOT Z);

e <= (NOT W AND Z)

                OR (NOT W AND X AND NOT Y)

                OR (NOT X AND NOT Y AND Z);

f <= (NOT W AND NOT X AND Z)

                OR (NOT W AND NOT X AND Y)

                OR (NOT W AND Y AND Z)

                OR (W AND X AND NOT Y);

g <= (NOT W AND NOT X AND NOT Y)

                OR (NOT W AND X AND Y AND Z);
```

```
END LogicFunc;
```

加分題

```
Library ieee;
USE ieee.std_logic_1164.all;


ENTITY seven_segment_pro IS
  PORT( W0, X0, Y0, Z0,
              W1, X1, Y1, Z1,
                    W2, X2, Y2, Z2 : IN STD_LOGIC;
      a0, b0, c0, d0, e0, f0, g0,
                    a1, b1, c1, d1, e1, f1, g1,
                    a2, b2, c2, d2, e2, f2, g2 : OUT STD_LOGIC);
END seven_segment_pro;


ARCHITECTURE LogicFunc OF seven_segment_pro IS
```

```
BEGIN

  a0 <= (NOT W0 AND NOT X0 AND NOT Y0 AND Z0)

                OR (NOT W0 AND X0 AND NOT Y0 AND NOT Z0)

                OR (W0 AND NOT X0 AND Y0 AND Z0)

                OR (W0 AND X0 AND NOT Y0);

  b0 <= (NOT W0 AND X0 AND NOT Y0 AND Z0)

                OR (NOT W0 AND X0 AND Y0 AND NOT Z0)

                OR (W0 AND NOT X0 AND Y0 AND Z0)

                OR (W0 AND X0 AND NOT Z0)

                OR (W0 AND X0 AND Y0);

  c0 <= (NOT W0 AND NOT X0 AND Y0 AND NOT Z0)

                OR (W0 AND X0 AND NOT Z0)

                OR (W0 AND X0 AND Y0);

  d0 <= (NOT X0 AND NOT Y0 AND Z0)

                OR (NOT W0 AND X0 AND NOT Y0 AND NOT Z0)

                OR (X0 AND Y0 AND Z0)

                OR (W0 AND NOT X0 AND Y0 AND NOT Z0);

  e0 <= (NOT W0 AND Z0)

                OR (NOT W0 AND X0 AND NOT Y0)
```

```
                OR (NOT X0 AND NOT Y0 AND Z0);
f0 <= (NOT W0 AND NOT X0 AND Z0)
                OR (NOT W0 AND NOT X0 AND Y0)
                OR (NOT W0 AND Y0 AND Z0)
                OR (W0 AND X0 AND NOT Y0);
g0 <= (NOT W0 AND NOT X0 AND NOT Y0)
                OR (NOT W0 AND X0 AND Y0 AND Z0);

a1 <= (NOT W1 AND NOT X1 AND NOT Y1 AND Z1)
                OR (NOT W1 AND X1 AND NOT Y1 AND NOT Z1)
                OR (W1 AND NOT X1 AND Y1 AND Z1)
                OR (W1 AND X1 AND NOT Y1);
b1 <= (NOT W1 AND X1 AND NOT Y1 AND Z1)
                OR (NOT W1 AND X1 AND Y1 AND NOT Z1)
                OR (W1 AND NOT X1 AND Y1 AND Z1)
                OR (W1 AND X1 AND NOT Z1)
                OR (W1 AND X1 AND Y1);
c1 <= (NOT W1 AND NOT X1 AND Y1 AND NOT Z1)
                OR (W1 AND X1 AND NOT Z1)
```

```
                OR (W1 AND X1 AND Y1);

d1 <= (NOT X1 AND NOT Y1 AND Z1)

                OR (NOT W1 AND X1 AND NOT Y1 AND NOT Z1)

                OR (X1 AND Y1 AND Z1)

                OR (W1 AND NOT X1 AND Y1 AND NOT Z1);

e1 <= (NOT W1 AND Z1)

                OR (NOT W1 AND X1 AND NOT Y1)

                OR (NOT X1 AND NOT Y1 AND Z1);

f1 <= (NOT W1 AND NOT X1 AND Z1)

                OR (NOT W1 AND NOT X1 AND Y1)

                OR (NOT W1 AND Y1 AND Z1)

                OR (W1 AND X1 AND NOT Y1);

g1 <= (NOT W1 AND NOT X1 AND NOT Y1)

                OR (NOT W1 AND X1 AND Y1 AND Z1);


a2 <= (NOT W2 AND NOT X2 AND NOT Y2 AND Z2)

                OR (NOT W2 AND X2 AND NOT Y2 AND NOT Z2)

                OR (W2 AND NOT X2 AND Y2 AND Z2)

                OR (W2 AND X2 AND NOT Y2);
```

```
b2 <= (NOT W2 AND X2 AND NOT Y2 AND Z2)
                OR (NOT W2 AND X2 AND Y2 AND NOT Z2)
                OR (W2 AND NOT X2 AND Y2 AND Z2)
                OR (W2 AND X2 AND NOT Z2)
                OR (W2 AND X2 AND Y2);
c2 <= (NOT W2 AND NOT X2 AND Y2 AND NOT Z2)
                OR (W2 AND X2 AND NOT Z2)
                OR (W2 AND X2 AND Y2);
d2 <= (NOT X2 AND NOT Y2 AND Z2)
                OR (NOT W2 AND X2 AND NOT Y2 AND NOT Z2)
                OR (X2 AND Y2 AND Z2)
                OR (W2 AND NOT X2 AND Y2 AND NOT Z2);
e2 <= (NOT W2 AND Z2)
                OR (NOT W2 AND X2 AND NOT Y2)
                OR (NOT X2 AND NOT Y2 AND Z2);
f2 <= (NOT W2 AND NOT X2 AND Z2)
                OR (NOT W2 AND NOT X2 AND Y2)
                OR (NOT W2 AND Y2 AND Z2)
                OR (W2 AND X2 AND NOT Y2);
```

```
    g2 <= (NOT W2 AND NOT X2 AND NOT Y2)
                    OR (NOT W2 AND X2 AND Y2 AND Z2);


END LogicFunc;
```