CS6135 VLSI Physical Design Automation
Homework 1: P&R Tool
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1. Goal

使用 Synopsys IC Compiler 練習 APR 步驟，並比較調整各個參數後的影響。

2. Procedure

APR Flow:

A. Design Setup:

創建一個 Library，並讀入 gate level netlists 檔。

B. Floorplan:

設定晶片 core utilization，IO Pad, Power Pad 的擺放位置，Power Ring 和 Power Starp 的設定。

C. Placement

congestion-driven 和 timing-driven 的優化程度取捨。

D. Clock Tree Synthesis (CTS)

對 clock tree 做分析，優化 clock 擺放位置。

E. Routing

繞線步驟。IC Compiler 的 DRC (Design Rule Check)也是在這步修正。

F. Design for Manufacturing (DFM)

增加晶片量產的良率，本次作業是 Insert Filler Cells

Reference:

https://timsnote.wordpress.com/digital-ic-design/ic-compiler/

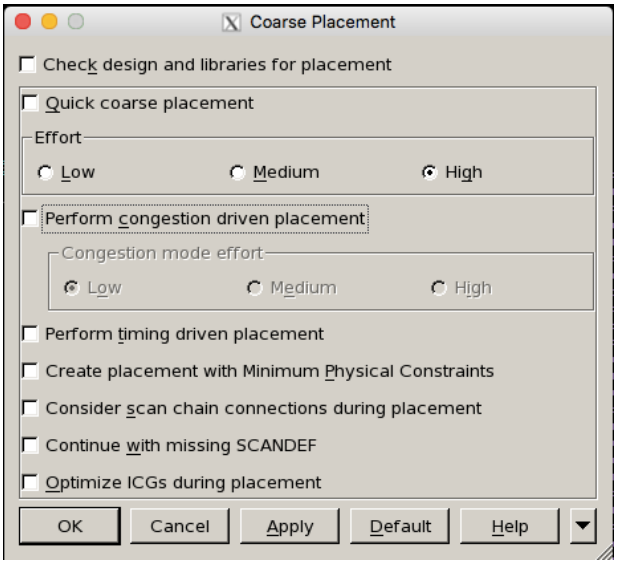
3. Results

Core utilization: determines the core and module sizes by total standard cells and macros density.

In the step B, Design Planning, I set the core utilization = 0.7.

For the Coarse Placement Option, I set Effort = high.

The clock period = 30ns (in .sdc file).



The settings of congestion driven placement and timing driven placement is as the following table.

	(congestion-driven, timing-driven)			
	(off, off)	(on, off)	(off, on)	(on, on)
Slack	19.53	18.89	18.88	20.32
Total cell area	68447.653505	68576.655881	68617.393487	68522.339107
Total wirelength	239988	236440	232413	237432

Slack: (off, on) < (on, off) < (off, off) < (on, on)

Total cell area: (off, off) < (on, on) < (on, off) < (off, off)

Total wirelength: (off, on) < (on, off) < (on, on) < (off, off)

Chip Layout

Clock period = 30

Core utilization = 0.7

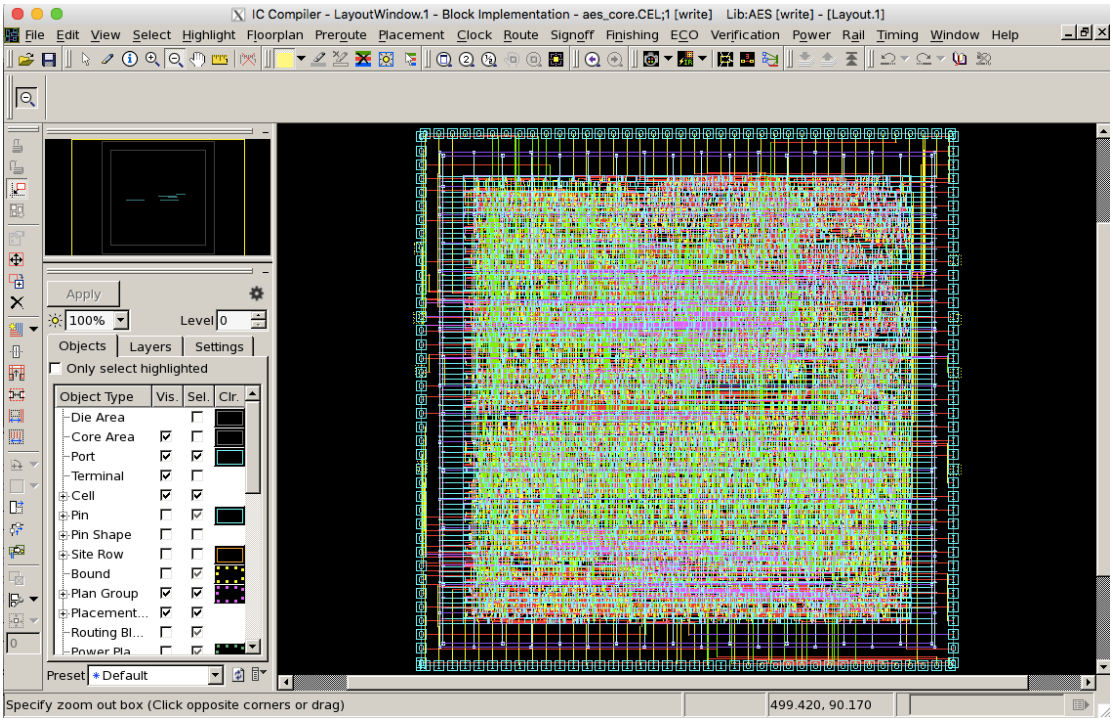
Congestion-driven = on

Timing-driven = off

Slack = 18.89

Area = 68576.655881

Wirelength = 236440



4. Discussion

What is the difference(s) between the congestion-driven placement and timing-driven placement?

Timing 和 Congestion (繞線壅擠程度)的優化是需要做取捨的。

Timing-driven placement 會盡量讓 cell 之間的距離靠近，使 timing 下降。

Congestion-driven placement 則是讓 cell 之間更分散，但會造成 timing 上升。

Why do we insert filler cells?

Standard cells APR flow 中，cells 是擺放成 row 排列，之間相鄰擺放確保 power 和 ground 連接。但無法保證每個 cells 都能相連接，為了要避免 Layout 製成晶片時因為 standard cell 密度分配不均勻，導致量率下降，所以會在沒有擺放 cell 的地方加入 filler cells，使 chip 密度均勻。

Reference:

https://timsnote.wordpress.com/digital-ic-design/ic-compiler/placement/

https://www.quora.com/Why-do-we-use-filler-cells-for-N-well-continuity

5. Summary

這次作業比較麻煩的部分是 Placement 後要檢查 timing report 是否有 no path

發生，如果有，就要重新做一次 placement，改參數再試一次。而因為 EDA problems 多半是使用 heuristic algorithm，所以在不改變任何參數的狀況下，扔可能會成功。

上學期修 VLSI Design 時已經有使用過 EDA tool 的經驗，雖然那時候也是照 guideline 點步驟一知半解。這次算是比較了解 ARP flow 後再使用 tool。寫作業的過程中，也有找到以前清大學長使用 IC compiler 的筆記並整理成網誌分享，真的非常感謝。期待這學期學好 physical design 的概念以及作業都能順利完成。