

# ZHANG YUNFAN

BLK604B, #12-758

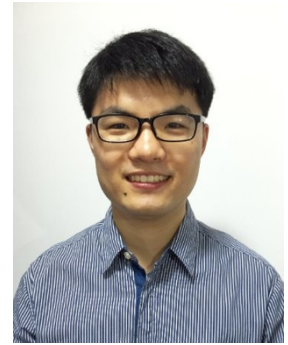
Punggol Road

Singapore 822604

**Citizenship:** Singaporean

**Mobile:** +65 98295382

**E-mail:** [yunfan.zhang23@gmail.com](mailto:yunfan.zhang23@gmail.com)



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## WORKING EXPERIENCE

### **Senior Analog IC Design Engineer in Marvell Asia Pte. Ltd.**

**Jul 2018 – Present**

- In charge of the key blocks of write driver features ultra-high speed, ultra-low power, high performance, including the biasing DAC, PECL, ECL to CMOS converter, Push-Pull driver, Voltage Controlled Oscillator and peripheral control logics
- In Charge of the Digital Design and Software Design part in the Pre-Amp team dedicated to hard-drive storage
- Investigated and improved the DC regulator to sustain sudden loading variation
- Designed a high-speed Digital Interface over 100MHz for the register data written into and read back programming from Front-end RTL to Back-end Synthesis, Place and Route, and Timing Constrain check using Synopsys Design Kit
- Proposed a completely new User Interface embedded with the hardware driver for the bench testing using C# and introduced a lot of useful feature
- Developed the new automatic test program across different conditions for enhanced bench evaluation which reduces the full set of tests from 2 days to 3 hours
- Proposed a data compilation tool using VBA for fast and standard data processing and presentation

### **Electrical Senior Engineer in Skyworks Global Pte. Ltd.**

**Apr 2017 – Jul 2018**

- In charge of Silicon controller design for 2G, 3G and 4G Power Amplifiers dedicated for different customers through all development procedures: specification definition, circuit realization, verification, lab validation, ATE; first silicon all functionality-pass success on all Si/SOI die design
- On track to volume production with process migration based on the silicon proven product and comprehensive lab characterization of the taped-out chip; co-work with System engineer to conduct the comprehensive system level validation process
- In collaboration with RF designer to design of the SOI Band Select Switch Module including PowerOnReset circuitry, customized digital design, level shifter, charge-pump and ESD network

### **Analog IC Design Engineer in Marvell Asia Pte. Ltd.**

**Jun 2012 – Apr 2017**

- In charge of the key blocks of write driver features ultra-high speed, ultra-low power, high performance, including the biasing DAC, PECL, ECL to CMOS converter, Push-Pull driver, Voltage Controlled Oscillator and peripheral control logics
- In Charge of the Digital Design and Software Design part in the Pre-Amp team dedicated to hard-drive storage
- Investigated and improved the DC regulator to sustain sudden loading variation
- Designed a high-speed Digital Interface over 100MHz for the register data written into and read back programming from Front-end RTL to Back-end Synthesis, Place and Route, and Timing Constrain check using Synopsys Design Kit
- Proposed a completely new User Interface embedded with the hardware driver for the bench testing using C# and introduced a lot of useful feature

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- Proposed a data compilation tool using VBA for fast and standard data processing and presentation

#### **Industrial Attachment in Siemens**

**Jul 2010 – Dec 2010**

- Scheduled systematic maintenance plans to ensure the service quality and liaised with vendor representatives, consultants and subcontractors to monitor the progress of upgrading project
- Appreciated highly by Corporate Manager for excellent customer service provided as well as the school supervisor due to solid knowledge obtained during servicing

## **EDUCATION**

### **National University of Singapore**

**Aug 2014 – May 2016**

#### **Master of Science (Electrical & Computing Engineering)**

CGPA 4.60 out of 5

### **Nanyang Technological University**

**Jul 2008 – Jun 2012**

#### **Bachelor of Engineering (Electrical & Electronic Engineering)**

First Class Honors (CGPA 4.80 out of 5)

Awarded the Micron Gold Medal with excellent academic result

- **Dean's List 2011-12 School of Electrical and Electronic Engineering**
- **Dean's List 2009-10 School of Electrical and Electronic Engineering**
- **Dean's List 2008-09 School of Electrical and Electronic Engineering**
- Top 5% students in the School of EEE, NTU
- **Singapore Ministry of Education Scholarship (Full Scholarship)**

## **RESEARCH EXPERIENCE**

### **Final Year Project**

**Sep 2010 – May 2012**

- Proposed a novel fully differential Class-D Amplifier – Digital buffer which features high efficiency and high Power Supply Rejection Ratio for audio application
- Introduced a novel timing control block to immune the output stage power supply noise without sacrificing much performance independently
- Appreciated highly appreciated by the supervisor and examiner and awarded with grade A for the excellent work achieved

### **Undergraduate Research Experience on Campus**

**Sep 2009 – Jun 2010**

- Engaged passionately in a research team of 2 PhDs to design Readout Integrated Circuit for a Novel Image Sensor in collaboration with DSO and MIT
- Obtained a firm knowledge of research progress in IC Design, PCB Design
- Awarded certification letter from URECA Office as an NTU President Research Scholar and outstanding research results published in the URECA Program 2009/2010

### **Design & Innovation Project**

**Dec 2009 – Jun 2010**

- Took charge of a team of 12 in DIP project to design Low-Power Optical Transceiver which is used for high speed data communication
- Came up conceptualized algorithm for frequency improvement of integrator in transceiver
- Outstanding research result exhibited in IET Green Energy Forum and highly appreciated by supervisors and honor guests

## **Circuit Design Skill**

- Analog: Regulator, Charge Pump, Op-Amp, SAR-ADC, Biasing DAC
- Digital – Verilog Front-end Design, Synopsys Design Compiler, IC Compiler, PrimeTime
- Mix-Mode Design – Cadence INCASIVE cosim design, Verilog-A, Verilog-AMS

## **COMPUTING SKILLS**

- Proficient in Microsoft Office Word, PowerPoint, and Excel
- Proficient in C, VBA, Perl, and C-Shell, SKILL Script
- Proficient in C#

## **LANGUAGES**

- English – proficient for both spoken and written
- Chinese – native speaker