Power Budget

	Component	Min (mA)	Nom (mA)	Max (mA)	
+5V	**Loads**				
	+5V power good LED (debug)	2	2	3	
	Teensy 4.1 consumption	100	100	100	
	Derived Voltage Rails				
	+/- 15V boost quiescent current	216.15	216.75	332.5125	
	+3V3 (LDO on Teensy)	2.85286	9.022	11.067	
	Totals	321.0029	327.772	446.5795	**Must stay below 500mA to respect USB 2.0 spec!**
+3V3	**Loads**				
	MCP33151-10 ADC x 3 (DVio)	0.00036	1.2	1.5	
	MCP23008 IO Expansion x 3	0.006	3	3	
	Relay driver HIGH pull-down in driver	0.792	0.792	0.792	
	+3V3 power good LED (debug)	2	2	3	
	+1V8_A LDO quiescent draw	0.05	0.05	0.075	
	Derived Voltage Rails				
	+1V8_A (LDO from +3V3)	0.0045	1.98	2.7	
	Totals	2.85286	9.022	11.067	
+12V	**Loads**				
	INA821 In-amp	0.6	0.6	0.87	
	RC4580 Op-amp x 7	42	42	63	
	DG408 8:1 mux x 4	0.04	0.2	0.3	
	DG409 dual 4:1 mux x 5	5	5	10	
	+12V power good LED (debug)	2	2	3	
	+12V LDO quiescent draw	2	2	5	
	Derived Voltage Rails				
	+5V_A (precision shunt reference)				
	Totals	51.64	51.8	82.17	
-12V	**Loads**				
	DG408 8:1 mux x 4	0.004	0.3	0.3	
	DG409 dual 4:1 mux x 5	2.5	2.5	2.5	
	-12V power good LED (debug)	2	2	3	
	Other				
	-12V inverting converter quiescent draw	6	6	6.5	
	Totals	10.504	10.8	12.3	
+5V_A	**Loads**				
	MCP33151-10 ADC x 3 (VREF)	0.00012	0.66	0.87	
	+5V_A power good LED (debug)	1.10	1.20	1.50	
	Totals	1.10012	1.86	2.37	
+1V8_A	**Loads**				
	MCP33151-10 ADC x 3 (AVDD)	0.0045	1.98	2.7	
	Totals	0.0045	1.98	2.7	

Summary

Rail	Min (mA)	Nom (mA)	Max (mA)
+5V	321.003	327.772	446.580
+3V3	2.853	9.022	11.067
+12V	51.640	51.800	82.170
-12V	10.504	10.800	12.300
+5V_A	1.100	1.860	2.370
+1V8_A	0.005	1.980	2.700

Digital Input Protection

Parameter	Value	Units	Comments
Maximum design input voltage	27	V	
Minimum design input voltage	-27	V	
Maximum design microcontroller pin source current	15	mA	
Maximum design microcontroller pin sink current	15	mA	
Microcontroller pin source/sink max current	25	mA	
Microcontroller pin max voltage	4	V	FT pins can take up to 3.3+4 = 7.4
Microcontroller pin min voltage	-0.3	V	All pins
External protection diode max current	125	mA	BAT54S rated for 200mA abs max
External protection diode forward voltage	0.25	V	
Nominal rated input/output voltage high	3.3	V	
Nominal rated input/output voltage low	0	V	
Source: required R1 + R2	220	Ohm	Assuming pin outputs 3.3V, short to GND
Sink: required R1 + R2	220	Ohm	
Chosen R1	470	Ohm	
Chosen R2	10	Ohm	
Resultant max input voltage	62.3	V	
Resultant min input voltage	-59	V	
Resultant max source/sink current	6.875	mA	
R1 max power dissipation	7.34375	W	
Current at which Pdiss of R1 is 0.5W	32.616	mA	
Input voltage at which Pdiss of R1 is 0.5W	18.880	V	
Input voltage at which Pdiss of R1 is 0.5W	-15.5797	V	

Note: not accounting for variation of diode forward voltage as function of diode current

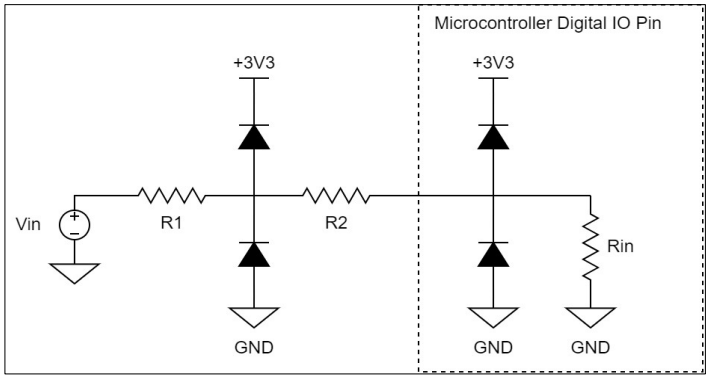
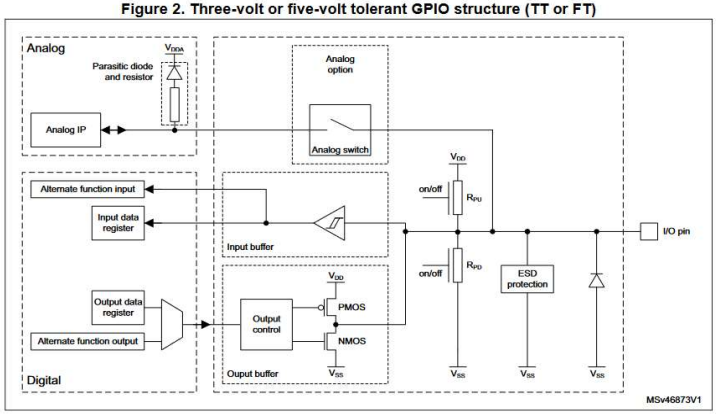


Figure 2. Three-volt or five-volt tolerant GPIO structure (TT or FT)



Note: *The parasitic diode in the analog domain is connected to V_{DDA} and cannot be used as a protection diode.*

The voltage level called V_{DD_FT} in some datasheets and reference manuals is inside the ESD protection block.

When the analog option is selected (by enabling analog peripheral on the given pin), the FT I/O is not five-volt tolerant anymore since the pin is supplied with V_{DDA}.

Caution: A TT or FT GPIO pin has no internal protection diode connected to supply (V_{DD}). There is no physical limitation against over-voltage. Therefore, for applications requiring a limited voltage threshold, it is recommended to connect an external diode to V_{DD}.

According to AN4899 from STMicro, cannot rely on internal protection diodes which may/may not exist.

Will proceed with design as if they do not exist.

Teensy 4.0/4.1 pins are all 3.3v only without overvoltage protection.

ADC Resolution

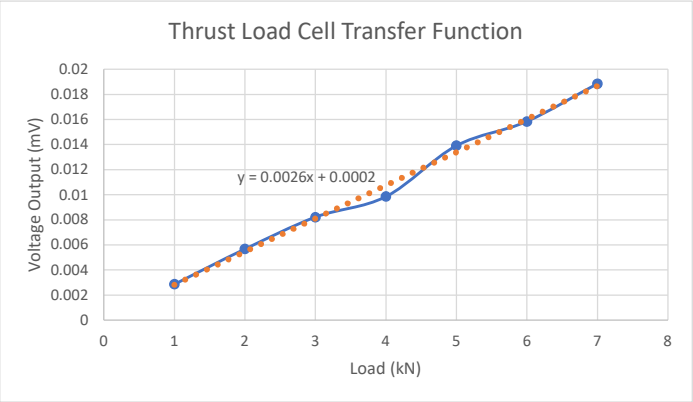
Parameter	Value	Units	Comments
Minimum sensor output voltage	0	mV	Differential output
Maximum sensor output voltage	100	mV	Differential output
Sensor resolution	0.05	mV/PSI	Voltage-output pressure transducer is 0.05mV/PSI
Signal conditioning gain	50	V/V	max gain to keep output voltage within ADC Vref
Minimum ADC sampling voltage	0	mV	
Maximum ADC sampling voltage	5000	mV	
ADC resolution required	2.5	mV/LSB	to resolve single PSI
ADC reference voltage	5	V	
ADC effective number of bits	12.8	bits	
ADC resolution	0.7011	mV/LSB	
PSIs resolvable	0.2804	PSI	
N resolvable	2.6966	N	
Calculate ENOB			
ADC reference voltage	5	V	
ADC SINAD	80.4	dB	MCP33151 14-bit
ADC effective number of bits (ENOB)	13.063	bits	
ADC resolution	0.5842	mV/LSB	
Calculate ENOB			
ADC reference voltage	5	V	
ADC SINAD	86.9	dB	MCP33131 16-bit
ADC effective number of bits (ENOB)	14.143	bits	
ADC resolution	0.2764	mV/LSB	

Options

- MCP33151-10-E/MS	14-bit SAR 1Msps SPI single-ended
- MCP33131-10-E/MS	16-bit SRAR 1Msps SPI single-ended

Thrust Load Cell Requirements			
Minimum sensor output voltage	0	mV	Differential output
Maximum sensor output voltage	23.1308	mV	Differential output
Sensor resolution	0.0026	mV/N	
Sensor resolution	0.0255	mV/kgf	kilogram-force
Signal conditioning gain	100	V/V	
Minimum ADC sampling voltage	0	mV	
Maximum ADC sampling voltage	2313.075	mV	
ADC resolution required	0.26	mV/LSB	to resolve single N
ADC resolution required	2.550	mV/LSB	to resolve single kg
Max gain to work with 5V ADC	216.16	V/V	

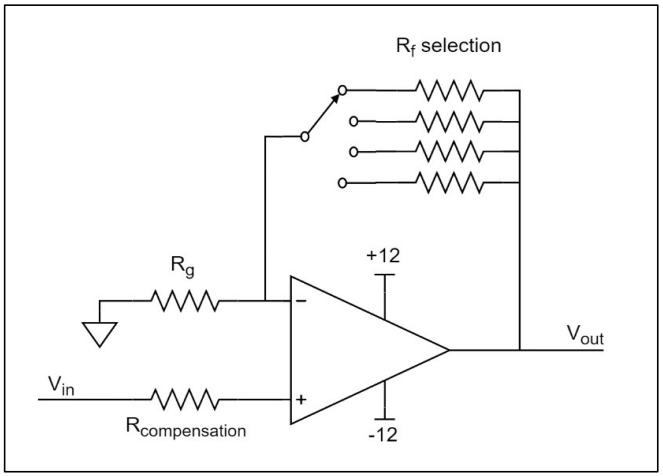
kN	V
1	0.002881
2	0.005678
3	0.008215
4	0.009862
5	0.013907
6	0.01584
7	0.018864
slope	0.0026 mV/N
max load	8896.443 N



ADC Tolerance Calculations

Resolution	VREF / 2^ENOB		Analog mux: Vishay DG409
Vref	5		
ENOB	12		
V/LSB	0.001220703	V/LSB	

		Tolerance	Min	Nom	Max	Units	Compensation Resistor
G = 1 V/V	Non-inverting amplifier Rf	0.10%	0	0	0	Ohm	000.000E+0 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	1.008	1.020	1.025	V/V	
G = 10 V/V	Non-inverting amplifier Rf	0.10%	45.255E+3	45.300E+3	45.345E+3	Ohm	4.495E+3 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	10.068	10.098	10.121	V/V	
G = 50 V/V	Non-inverting amplifier Rf	0.10%	242.757E+3	243.000E+3	243.243E+3	Ohm	4.890E+3 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	49.705	49.717	49.820	V/V	
G = 100 V/V	Non-inverting amplifier Rf	0.10%	498.501E+3	499.000E+3	499.499E+3	Ohm	4.941E+3 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	100.808	101.020	101.225	V/V	



TPS65131 Dual-Rail Boost Calculations

Parameter	Value	Units	Comments
Positive Boost Converter			
R2 max value	200	kOhm	
Vpos	15	V	Positive boost output voltage value
Vref	1.213	V	Positive boost output reference voltage
R2 chosen value	47.5	kOhm	
Ideal R1	539.886645	kOhm	
Chosen R1	536	kOhm	
Actual Vpos	14.9007474	V	
Inductor Selection (Vpos)			
Vin	5	V	
Vpos rail current requirement	0.08	A	power budget shows 70mA, I added safety margin
Peak inductor current I_L-P	0.375	A	
Inductor current ripple	0.075	A	
Converter switching frequency	1.25	MHz	
L1 value	35.5555556	uH	datasheet recommends between 3.3uH to 6.8uH
			Go with 4.7uH for now, check performance once sample is received. May tune inductor value after receiving the boards.
Output Capacitors			
Max allowed ripple (Delta Vpos)	0.005	V	
Minimum output capacitance (C4)	8.5333	uF	
ESR of C4	0.01	Ohm	
Ripple due to ESR	0.0008	V	
Feedforward Capacitor			
C9 value	12.69E-12	F	
Chosen C9 value	13	pF	

Parameter	Value	Units	Comments
Inverting Boost Converter			
R4 max value	200	kOhm	
Vneg	-15	V	
Vref	1.213	V	
R4 chosen value	47.5	kOhm	
Ideal R3	587.38664	kOhm	
Chosen R3	576	kOhm	
Actual Vpos	-14.709221	V	
Inductor Selection (Vneg)			
Vin	5	V	
Vneg rail current requirement	0.01	A	power budget shows 5mA, I added safety margin
Peak inductor current I_L-P	0.0625	A	
Inductor current ripple	0.0125	A	
Converter switching frequency	1.25	MHz	
L2 value	240	uH	datasheet recommends between 3.3uH to 6.8uH
Output Capacitors			
Max allowed ripple (Delta Vneg)	0.005	V	
Minimum output capacitance (C5)	1.2	uF	
ESR of C5	0.01	Ohm	
Ripple due to ESR	0.0001	V	
Feedforward Capacitor			
C10 value	13.02E-12	F	
Chosen C10 value	13	pF	

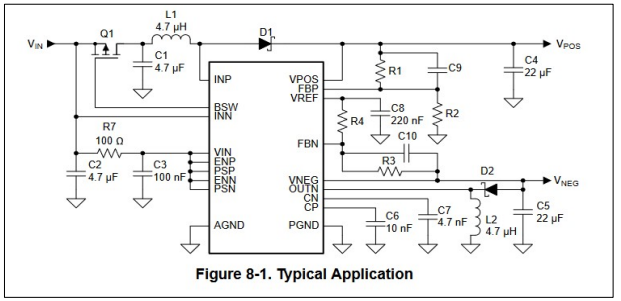


Figure 8-1. Typical Application

Power Rail Tolerance Calculations

Parameter	Tolerance (%)	Min	Nom	Max	Units	Comments
+15V boost						
R1	1%	530.64	536	541.36	kOhm	
R2	1%	47.025	47.5	47.975	kOhm	
Vref	-	1.2	1.213	1.225	V	
Output voltage	-	14.47291	14.90075	15.32741	V	
-15V inverting boost						
R3	1%	570.24	576	581.76	kOhm	
R4	1%	47.025	47.5	47.975	kOhm	
Vref	-	1.2	1.213	1.225	V	
Output voltage	-	-15.1548	-14.7092	-14.2634	V	
+12V LDO						
Dropout	-	0.7	1	1.2	V	
Minimum input voltage required		12.7	13	13.2	V	satisfied
Output voltage accuracy		-5%	0%	5%		
Output voltage		11.4	12	12.6	V	
-12V LDO						
Dropout	-	1.7	1.7	1.7	V	
Minimum input voltage required		-13.7	-13.7	-13.7	V	satisfied
Output voltage		-11.4	-12	-12.6	V	provided in datasheet
+1V8_A LDO						
Dropout		0.35	0.35	0.695	V	
Minimum input voltage required		2.15	2.15	2.495	V	satisfied
Output voltage accuracy	-	-1.50%	0%	1.50%		
Output voltage		1.773	1.8	1.827	V	

5V_A Precision Reference Biasing

Parameter	Tolerance	Min	Nom	Max	Units	Comments
ADC VREF current (load)	-	0.00012	0.66	0.87	mA	
Shunt reference bias current	-	1	1	1	mA	Min. 60uA. Cannot exceed 15mA.
Total current through Rbias	-	1.00012	1.66	1.87	mA	
Supply voltage (input to shunt)	-	11.9	12	12.1	V	100mV of ripple is a lot
Shunt reference output voltage	-	4.995	5	5.005	V	
Vin - Vshunt_out		6.895	7	7.105	V	
Rbias		3.69	4.22	7.10	kOhm	
Rbias calculated from Eqn 3	-		4.22		kOhm	verifies my nominal calculation above
Chosen resistor value	**1%**	**4.18**	**4.22**	**4.26**	**kOhm**	
Resultant bias current		0.748	0.999	1.701	mA	Meets requirements!

APPLICATIONS INFORMATION

The ADR5040/ADR5041/ADR5043/ADR5044/ADR5045 are a series of precision shunt voltage references. They are designed to operate without an external capacitor between the positive and negative terminals. If a bypass capacitor is used to filter the supply, the references remain stable.

For a stable voltage, all shunt voltage references require an external bias resistor (R_{BIAS}) between the supply voltage and the reference (see Figure 19). The R_{BIAS} sets the current that flows through the load (I_L) and the reference (I_{IN}). Because the load and the supply voltage can vary, the R_{BIAS} needs to be chosen based on the following considerations:

- R_{BIAS} must be small enough to supply the minimum I_{IN} current to the ADR5040/ADR5041/ADR5043/ADR5044/ADR5045, even when the supply voltage is at its minimum value and the load current is at its maximum value.
- R_{BIAS} must be large enough so that I_{IN} does not exceed 15 mA when the supply voltage is at its maximum value and the load current is at its minimum value.

Given these conditions, R_{BIAS} is determined by the supply voltage (V_S), the ADR5040/ADR5041/ADR5043/ADR5044/ADR5045 load and operating current (I_L and I_{IN}), and the ADR5040/ADR5041/ADR5043/ADR5044/ADR5045 output voltage (V_{OUT}).

$$R_{BIAS} = \frac{V_S - V_{OUT}}{I_L + I_{IN}} \quad (3)$$

ADC SPI Bandwidth

Parameter	Value	Units	Comments	Calculations are estimation for the MCP33151-10
ADC data bits	16	bits	Sent in groups of 8 bits	
Dead time between 8-bit bursts	5	bits	number of equivalent clock cycles	
Dead time from CS low to start	5	bits		
Dead time from end to CS high	5	bits		
SPI clock frequency	100	MHz		
SPI clock period	10.0E-9	s		
Time needed to read one sample	310.0E-9	s		
Max samples read per second	3.2E+6		So theoretically we can hit 1Msps if Teensy is fast enough	
Data throughput				
High-speed sample rate	56000	sps		
Number of high-speed channels	10	-		
Low-speed sample rate	100	sps		
Number of low-speed channels	20	-		
data bits per sample	16	bits		
overhead per sample	0	bits		
data throughput	8.992	Mbit/s		
LabJack data throughput (max)				
Data bits per sample	24	bits		
overhead per sample	0	bits		
samples per second	100000	sps		
data throughput	2.4	Mbit/s		

Mid-Project Report Progress

Section	Done?	Comments
Abstract	Yes	
List of Abbreviations	Yes	
Introduction	In Progress	
Background	No	
Requirements	Yes	
Design	Yes	
Results	Yes	
Plan for next semseter	Yes	
Impact on Society and Environment	No	
Conclusion	Yes	
~~A1-Perfboard~~	~~Yes~~	~~removed :)~~
A2-Eval board	In Progress	
A3-Design calculations	No	
References	In Progress	

High-Speed Analog Input Filtering

dB	V
0	1.000
-3	0.708
-6	0.501
-10	0.316
-20	0.100
-30	0.032
-40	0.010
-50	0.003
-60	0.001