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Design of an Open-Source and Flexible Low-Cost Data Acquisition Device

Final Report

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Abstract

The McGill Rocket Team's rocket engine test site data acquisition (DAQ) system currently uses a LabJack T7 as the DAQ device to interface with sensors and control components. For a student design team, the T7 is expensive. The cost of the T7 and its closed-source software have put the team in challenging situations in the past. Thus, there is increasing interest in developing a lower-cost, in-house alternative with similar or better hardware capabilities to improve the performance and usability of the system. The goal of the thesis is to develop a low-cost DAQ and control device to replace the T7. Specifically, the thesis aims to: determine hardware and software requirements for the replacement device; design the schematics and printed circuit board (PCB) layout; order a prototype PCB for the replacement device; and characterize its performance with bench testing, sensors, and controlled components from the test site. During the Winter 2023 semester, the schematics for the replacement device were completed using knowledge gained from reading industry application notes and extensive circuit simulation in LTspice, the PCB layout was finished using Altium Designer, and the board was manufactured and assembled. Firmware was written to test the features of the device on the bench and demonstrated that the design meets the requirements. Future work includes writing the application firmware and thoroughly testing the device with sensors and components from the team's test site.

ACKNOWLEDGMENTS

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LIST OF ABBREVIATIONS

ADC	Analog-to-digital converter
BGA	Ball grid array
BOM	Bill of materials
CAN	Controller area network
DAQ	Data acquisition
DMA	Direct memory access
D-sub	D-subminiature
ENOB	Effective number of bits
GND	Ground
I2C	Inter-integrated circuit
In-amp	Instrumentation amplifier
IO	Input/output
ksp	Kilo samples per second
LED	Light-emitting diode
LDO	Low-dropout
MRT	McGill Rocket Team
Mbps	Megabits per seconds
Msps	Million samples per second
Op-amp	Operational amplifier
PCB	Printed circuit board
PSRAM	Pseudo-static RAM
QFP	Quad flat pack
SAC	Spaceport America Cup
SPI	Serial peripheral interface
SRAD	Student-researched and designed
UART	Universal asynchronous receiver-transmitter
USB	Universal serial bus

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I. INTRODUCTION

Space and rocketry are becoming increasingly popular. Many student design teams around the world design, test, and launch high power rockets, as evident by the strong competition each year at the annual Spaceport America Cup (SAC), an intercollegiate rocket engineering competition. As teams develop experience with commercially available rocket motors, they naturally gravitate toward designing their own propulsion systems.

The McGill Rocket Team (MRT) decided to pursue development of a student-researched and designed (SRAD) hybrid rocket engine in 2017. Since then, a permanent rocket engine testing facility was built from the ground up at McGill's Macdonald campus. The team's efforts culminated in 2021 with its first successful hot-fire test of an SRAD hybrid rocket engine. The team has since conducted multiple tests at the test site, striving to improve engine performance and design.

An essential part of the test site is the data acquisition (DAQ) and control system. To minimize the time required to get the test site to a functional state, many commercially available components were used because minimizing development time was prioritized over cost optimization. Most notably, a LabJack T7 DAQ device was chosen as the heart of the DAQ and control system at the test site.

The T7 is a powerful, flexible, and easy-to-use tool that has served well at the test site. The T7 offers high-resolution, high-speed analog sampling across multiple channels, various flexible digital inputs/outputs (IO), and data streaming over universal serial bus (USB) or Ethernet [1]. Additionally, LabJack offers expansion boards to increase the capabilities of the T7. To complement its hardware, LabJack developed an application programming interface for multiple programming languages, including LabVIEW, Python, MATLAB, and more. However, these useful features come with great monetary cost.

MRT is a student team with limited budget. The relatively expensive price of the T7 was justified when the test site was first being constructed because the team prioritized rapid development. Now, with an operational test site, the team seeks to expand the scope of its instrumentation and control system by adding additional sensors and actuated components. Further, as the team builds its expertise in SRAD engines, there is future potential to use the test site to characterize bi-propellant liquid rocket engines which would require almost doubling the current number of sensors and actuated components. Although the T7 is a powerful device, its performance will be insufficient to handle the expansion. A possible solution to this problem would be to purchase a second T7, but under the team's current budget, this option is not financially feasible.

The goal of this thesis project is to design, manufacture, and test a lower cost, in-house replacement for the T7, hereon referred to as the DAQ device. To do so, hardware and software requirements for the replacement device will be determined; the schematics and printed circuit board (PCB) layout will be designed; a prototype PCB for the replacement device will be ordered; and its performance will be characterized with bench testing, sensors, and controlled components from the test site. An SRAD replacement for the T7 allows members of the team to gain greater understanding of DAQ theory and builds expertise within MRT for analog signal conditioning and sampling hardware. Further, with more affordable DAQ devices, the team can continually improve the DAQ and control system at the test site in a financially sustainable manner.

This report is organized as follows: background information about DAQ theory will be provided in Section II, the requirements for the DAQ device will be described in Section III, design considerations and details in Section IV, and results in Section V. The impact of the DAQ device on society and the environment will be analyzed in Section VI, with concluding remarks in Section VII. The appendices contain the design calculations, schematics, and testing results.

II. BACKGROUND

The test site has an extensive instrumentation suite to collect different streams of data necessary for characterizing the performance of the team's SRAD rocket engines. All of the sensors are analog and

measure different types of signals. For example, thermocouples are used to measure the temperatures of the plumbing for the liquid oxidizer and the combustion chamber, and pressure transducers measure the fluid pressures at points in the system. For different physical phenomena, the DAQ system must sample the analog signals at different minimum sampling rates to accurately digitize the signal.

A. Analog Signal Sampling

Analog signals are continuous. For computer systems to interpret analog signals, they must be converted to discrete forms through sampling, which records the signal at periodic intervals. However, depending on how the conversion from continuous to discrete signals is performed, error may be introduced into the discrete version.

The Nyquist-Shannon sampling theorem [2] provides a fundamental rule for the minimum sampling rate required to accurately digitize analog signals. Specifically, the theorem states that for a bandwidth-limited signal, a sufficient sampling rate is greater than two times the frequency of the highest frequency signal contained in the bandwidth-limited signal. If this condition is not met, either by sampling a bandwidth-limited signal too slowly or by sampling a signal that is not bandwidth-limited, then the (discrete) sampled signal will be inaccurate due to aliasing, where higher frequency signals appear as lower frequency signals. Moreover, aliasing is not distinguishable from the true signals.

Since analog signals are continuous and their bandwidths may be unpredictable, an accurate DAQ system will require some form of guarantee that the signal becomes bandwidth-limited prior to sampling by an analog-to-digital converter (ADC) with a sufficiently high sampling frequency. To ensure that the signal is bandwidth-limited, anti-aliasing filters can be used.

B. Anti-Aliasing Filters

To satisfy the Nyquist-Shannon sampling theorem, the signal sampled by the ADC must be bandwidth-limited to prevent higher frequency contents from aliasing into the sampled, digitized signals. Therefore, an anti-aliasing filter, which can be implemented using a low-pass filter, is placed before the ADC in the analog signal chain.

Filters can be described by the frequency response, which is composed of the magnitude and phase responses. The magnitude response indicates how the amplitude of the output compares to the input over different frequencies. Similarly, the frequency response shows the phase shift between the input and output over frequency.

An ideal anti-aliasing filter has a perfectly flat magnitude response and group delay (linear phase delay) in the passband, and a “brick wall” stopband. A flat magnitude response and group delay ensures that the signal is not distorted by applying varying gain and phase shift, respectively, to different signal frequencies. However, these filters cannot be realized in practice, so there is a region between the passband and stopband where the magnitude response rolls off. Different filter topologies are optimized for different magnitude and phase responses. Fig. 1 shows the magnitude response of several commonly-used analog filters [3].

For anti-aliasing filters in DAQ systems, it is important to minimize the distortion applied to the signal by the magnitude and phase responses of the filter. As an example, the Chebyshev filter (shown in red in Fig. 1) would not be suitable for anti-aliasing due to the relatively large ripple in the passband of the magnitude response. Maxim Integrated [3] and National Instruments [4] provide excellent application notes describing anti-aliasing filters.

III. REQUIREMENTS

The requirements in this section form the specifications for the DAQ device. These specifications will be used to guide design decisions. Requirements and general statements of intent are distinguished by the following:

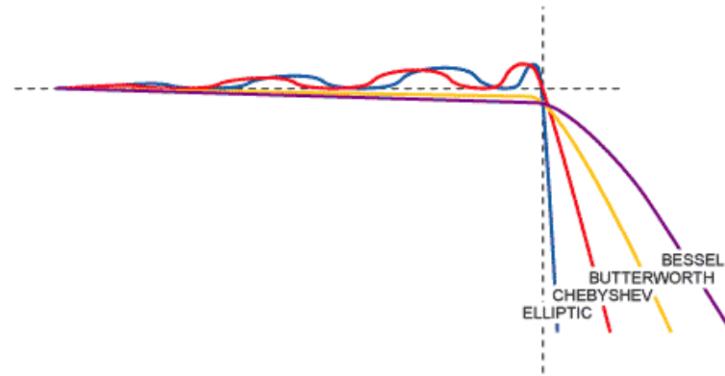


Fig. 1. Comparison of the magnitude response of popular analog filters [3].

- Mandatory requirements are denoted with “**shall**”
- Strongly recommended requirements are denoted with “**should**”
- Optional requirements or statements of intent are denoted with “**may**” or “**will**”

These conventions are chosen to align with those used by the Design, Test, & Evaluation Guide from the SAC competition documents. Members of MRT should be familiar with these conventions.

A. Digital and Analog Channels

The DAQ device **shall** provide:

- At least 24 digital IO channels
- At least 4 high speed differential analog inputs
- At least 20 low speed single-ended analog inputs
- At least 4 high speed single-ended analog inputs

The test site currently uses 10 digital IO channels for relay control for the hybrid engine. In the future, for a bi-propellant liquid engine, the test site will require at least 16 channels. To add margin for expandability and contingency, the requirement was set to be 24 digital IO channels.

Although most analog sensors used for instrumentation at the test site have differential voltage outputs, the team currently uses a dedicated sensor board to condition the signals before digitization by the LabJack T7. Instead of performing all signal conditioning on the DAQ device, using a dedicated sensor board provides greater flexibility because there are both current-output (4-20 mA output) and voltage-output sensors that may be used interchangeably, depending on the test being conducted. Therefore, to keep the DAQ device flexible, a total of 4 differential analog inputs and 24 single-ended analog inputs was chosen. Depending on the microcontroller chosen and board space requirements, more channels may be implemented to increase the capability of the DAQ device.

B. Input Protections

The device **shall** protect all inputs to the following ratings:

- Digital IO **shall** be protected against input voltages up to $\pm 27\text{ V}$
- Analog inputs **shall** be protected against input voltages up to $\pm 15\text{ V}$

As this device is intended to be flexible, it is not unlikely that signals which exceed the typical 3.3 V or 5 V input ratings of microcontrollers will be accidentally connected to the IO channels of the device. These protections will ensure that the device is not damaged by these accidental connections.

C. Analog Inputs

1) *Analog Input Sample Rates*: At the test site, most signals are adequately sampled at 50 Hz, therefore, low speed analog inputs **shall** have a minimum of 50 Hz sampling rate. For the few select sensors that can give insight into combustion stability and performance, a signal bandwidth of 20 kHz is required. Thus, high speed analog inputs **shall** be able to accurately sample 20 kHz bandwidth signals.

2) *Common-Mode Input Voltage Range*: The common-mode input voltage range of all analog inputs **shall** be at least ± 10 V. This value was chosen because the sensors at the test site are supplied by 12 V (single supply) or ± 12 V (split supply).

3) *ADC Resolution*: All analog inputs **shall** be measured by ADCs that have at least 12 effective number of bits (ENOB). Note that this requirement was specified after performing design calculations for ADC resolution, which will be described in Section IV.

4) *Adjustable Gain*: The device **shall** be able to apply adjustable voltage gain to the analog inputs. The adjustable gain settings **shall** be 1 V/V, 10 V/V, 50 V/V, and 100 V/V.

D. Board Temperature Sensor

The device **shall** be able to measure the temperature of the PCB of the device. The measurement accuracy **shall** be within ± 3 °C. Please note that the internal temperature sensor on some microcontrollers does not satisfy this requirement because microcontrollers may generate significant heat during operation, thus the temperature of the microcontroller may differ from the board temperature.

E. Operating Temperature Range

The device **shall** have a rated operational temperature range of -40 °C to 85 °C.

F. Standalone Operation

1) *Battery Power Input*: To enable standalone operation without computer control, the device **shall** have a connector to accept battery power. The battery power input voltage ratings will be determined later in the design phase.

2) *SD Card*: The device **shall** have a microSD card slot to save data to a microSD card. This is intended to enable the device to be programmed to run without interfacing to a computer.

G. Computer Interface

The DAQ device **will** be used with a computer to display live values of inputs and outputs at the test site. As such, the device **shall** interface with a computer via USB or Ethernet. For the scope of the thesis project, Ethernet capability **shall** be present but does not necessarily need to be usable.

H. Add-Ons and Expansion

1) *Power*: The device **shall** provide access to 5 V power and ground (GND) for add-ons.

2) *Digital IO*: The device **shall** provide access to at least 8 digital IO pins that are unique to the add-ons. Please note that this requirement does not mean that each add-on must have 8 unique digital IO ports assigned to it; rather, all add-ons may share the 8 digital IO pins.

3) *Analog Inputs*: The device **shall** provide access to at least 8 analog inputs that are unique to the add-ons, similar to the above requirement for digital IO.

4) Peripheral Expansion Ports: To enable easy integration of additional features, the device **shall** provide access to the following hardware peripheral ports:

- Serial peripheral interface (SPI)
- Controller area network (CAN)
- Inter-integrated circuit (I2C)
- Universal asynchronous receiver-transmitter (UART)

Please note the emphasis on “hardware peripheral ports”. While bit banging could likely provide SPI, I2C, and UART interfaces, bit banging will reduce the logging speed significantly.

IV. DESIGN

In this section, the decisions made during the design of each section of the DAQ device will be explained. The block diagram of the DAQ device, shown in Fig. 2, is presented first to provide an overall idea of the design of the board before discussion of detailed design choices. First, the analog signal chain, which is depicted at the top of Fig. 2, will be discussed, followed by some of the digital sections.

A. Analog Input Selection

According to the requirements, the DAQ device must be able to interface with at least 4 high-speed differential analog inputs, 20 low-speed single-ended analog inputs, and 5 high-speed single-ended analog inputs. These requirements are derived from the number of sensors required for a liquid bi-propellant rocket engine test site instrumentation suite.

A naive implementation would be to use one ADC per analog input, resulting in 29 ADCs. However, this approach is both costly and inefficient. Using a microcontroller, each ADC would be polled sequentially. The advantage of this approach is that the maximum sampling rate of all the ADCs is limited by the maximum polling rate of the microcontroller. That is, the microcontroller does not need to wait for each ADC to finish its conversion because the ADC can perform its conversions while the microcontroller is sampling other ADCs. However, the major disadvantages of this design are the high number of components, anticipated difficulties in PCB layout, and large number of IO pins required to interface with the ADCs. For instance, supposing that the ADCs communicate using SPI, then 29 IO pins would be used simply for the chip select pins.

The design can be improved by using analog multiplexers to connect one ADC to multiple analog inputs. The requirements have categorized the analog inputs as low-speed single-ended, high-speed single-ended, and high-speed differential inputs. Thus, it is logical to use multiplexers to connect one ADC to each group of inputs. Using this scheme, only three ADCs are required with six analog multiplexers. Although digital IO pins will be needed to select between multiplexed inputs, there is an overall reduction in the number of IO pins required. Therefore, the design has proceeded with this approach, as shown in the block diagram in Fig. 2.

B. Anti-Aliasing Filter Design

To satisfy the Nyquist-Shannon sampling theorem, the signal being sampled must be bandwidth-limited which can be guaranteed by using a low-pass filter. The cut-off frequency of the low-pass filter depends on the bandwidth of the analog signals being sampled. For rocket engine tests, the signals with the highest frequency content are pressure transducers measuring the combustion chamber pressures of liquid rocket engines [5]. Although the bandwidths of combustion chamber pressure signals in hybrid rocket engines, which the team is currently designing, are lower than those in liquid engines, the team wants to be able to expand the test site DAQ and control system in the future to test liquid engines. Hence, the DAQ device is being designed to accurately measure the signals for a liquid engine instrumentation system. Explicitly, the maximum bandwidth of liquid engine combustion chamber pressure signals is 20 kHz [5].

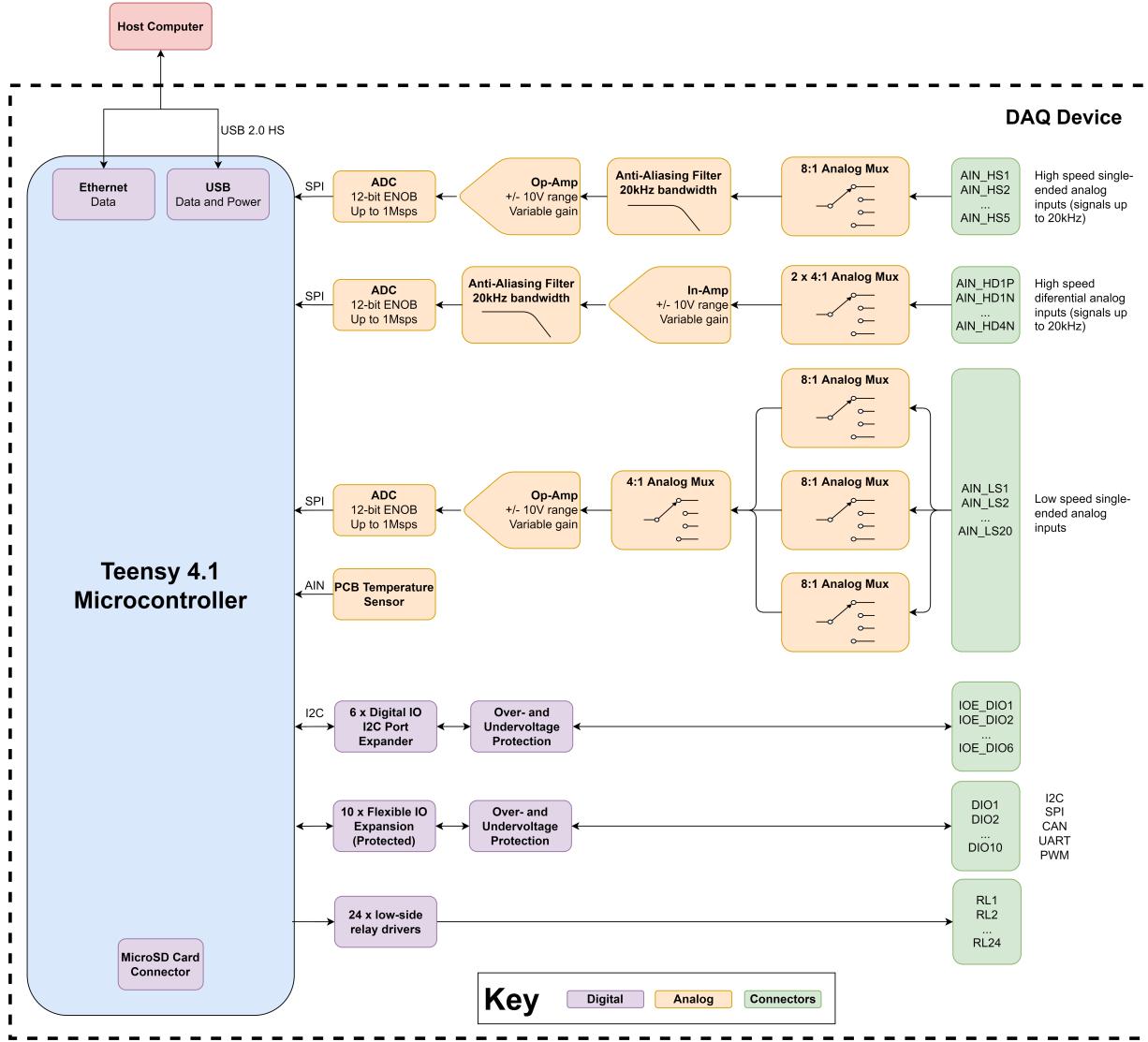


Fig. 2. Main block diagram for the DAQ device.

However, the cut-off frequency of the low-pass filter is not necessarily 20 kHz, as the filter will attenuate the signal by -3 dB at the cut-off frequency, which is undesirable.

To design the filter, the Filter Design Tool by Analog Devices [6] was used. The tool visualizes important filter parameters and characteristics, such as frequency response, phase delay, group delay, step response, etc., and also provides filter implementations in Sallen-Key and multiple feedback architectures. After settling on a filter using the tool, the generated filter circuits were simulated in LTspice.

For this project, the Sallen-Key architecture was chosen because, compared to the multiple feedback topology, Sallen-Key filters minimize the gain bandwidth requirements for the operational amplifiers (op-amps) used in the filter [7], hence lowering cost and making part selection. These are important design considerations due to the current widespread chip shortage which has persisted for the last few years and will likely continue. The Sallen-Key topology also uses one fewer passive component compared to the multiple feedback architecture. However, the Sallen-Key filter is not easily tuned and is sensitive to the values of the passive components used [7], but high-precision passives, such as 1%-tolerance capacitors

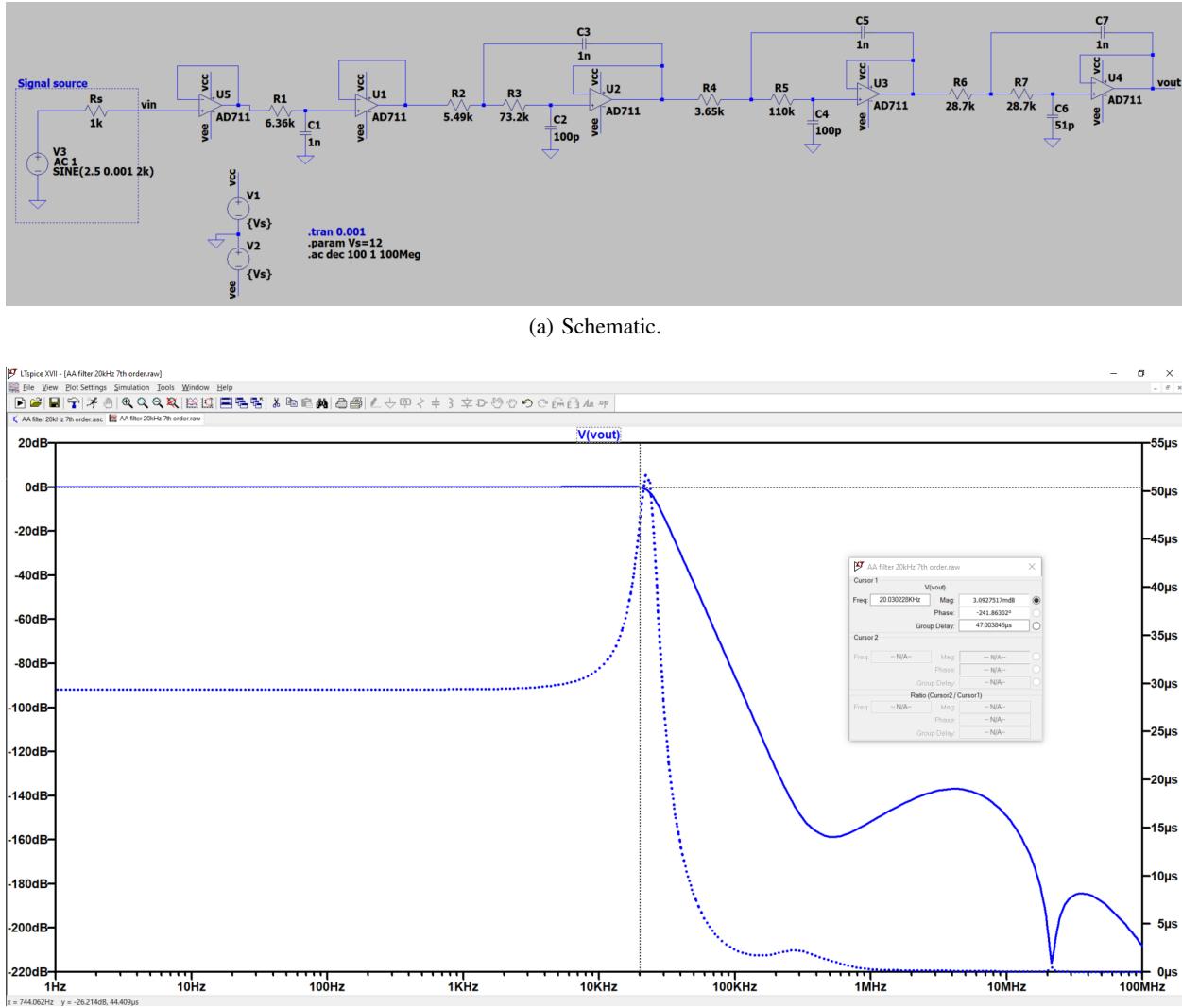
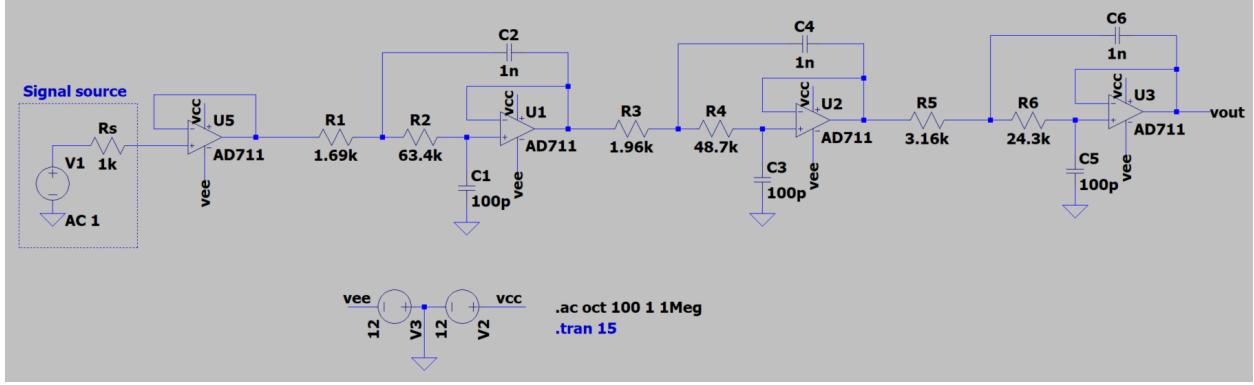


Fig. 3. Schematic and simulation results of the 7th-order Butterworth filter with a cut-off frequency of 25 kHz in LTspice. The cursors read a magnitude response and group delay of 0.003 09 dB and 47.004 μ s at a frequency of 20.030 kHz. Note that the initial group delay is 29.382 μ s. The group delay begins to increase starting at approximately 6 kHz.

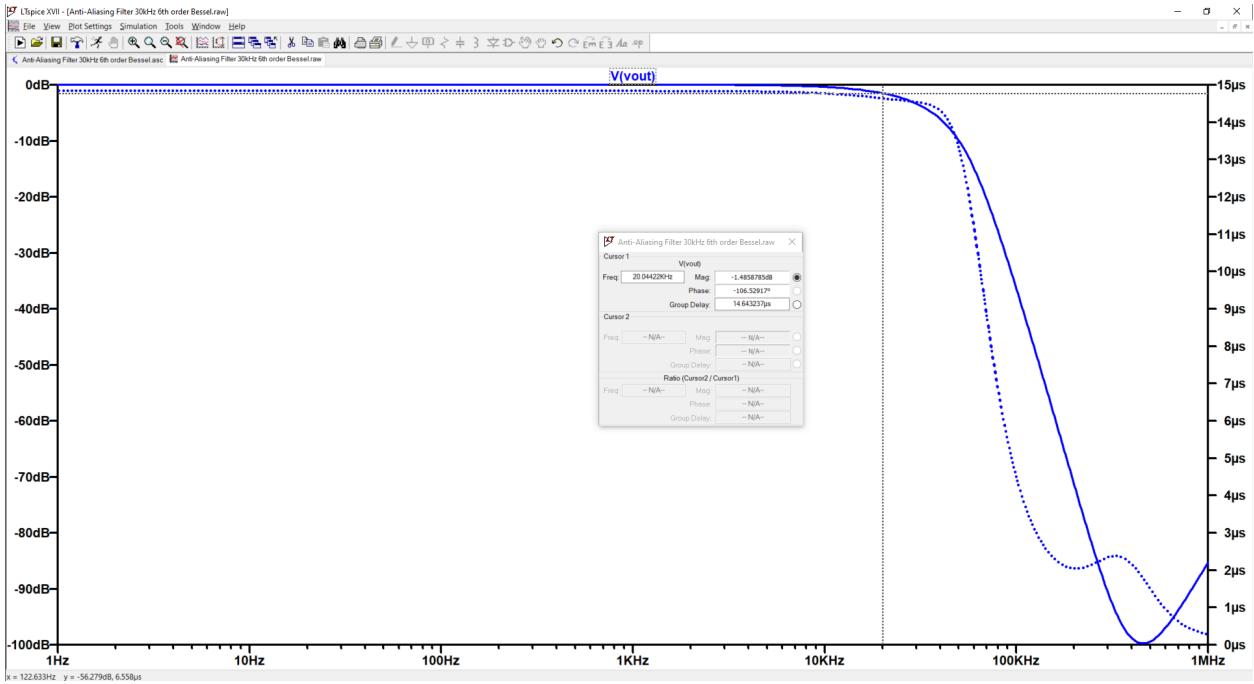
and 0.1%-tolerance resistors, can be used. Significant effort will be dedicated to verifying the performance of the filter after it is manufactured.

Initially, an 7th-order Butterworth low-pass filter was chosen for its maximally flat magnitude response in the pass-band and sharp roll-off [8]. The cut-off frequency was chosen to be 25 kHz. The filter was implemented using four op-amps, as shown by the schematic in Fig. 3a. The frequency response was simulated in LTspice and is shown in Fig. 3b. However, the Butterworth filter was found to be unsuitable for anti-aliasing filtering because it does not have a flat group delay in the pass-band. As shown in Fig. 3b, the simulation results show that the filter would add significant distortion due to non-constant group delay for frequency content above approximately 6 kHz.

Instead, a 6th-order Bessel low-pass filter will be used. Bessel filters have a maximally flat pass-band and linear phase response [9], meaning that they preserve the shape of the waveform. The trade-off is slower roll-off into the stop-band which can result increased noise in the sampled signal. Additionally, the filter roll-off begins earlier, so the cut-off frequency needs to be set higher to ensure that signals at



(a) Schematic.



(b) Magnitude response (left axis, solid curve) and group delay (right axis, dotted curve).

Fig. 4. Schematic and simulation results of the 6th-order Bessel filter with a cut-off frequency of 28 kHz in LTspice. The cursors read a magnitude response and group delay of -1.486 dB and $14.643 \mu\text{s}$ at a frequency of 20.044 kHz . The initial group delay is $14.838 \mu\text{s}$.

the edge of the pass-band are not significantly attenuated.

The 6th-order Bessel filter will be implemented using three op-amps in the Sallen-Key architecture as shown in Fig. 4a. The frequency response is shown in Fig. 4b. The cut-off frequency of the filter was set to 28 kHz to reduce the attenuation at 20 kHz. With the current filter implementation, the attenuation at 20 kHz is -1.486 dB , and the group delay remains flat until approximately 30 kHz.

Higher-order filters were chosen for the faster roll-off between the pass-band and stop-band, resulting in lower noise in the sampled signal compared to first-order anti-aliasing filters. The tradeoff is cost, circuit complexity, and board space. With higher-order filters, more components are required for the circuit implementation. However, since this design will not be manufactured in high volume, these small cost inefficiencies were considered acceptable.

According to the block diagram shown in Fig. 2, only the high-speed analog inputs have anti-aliasing

filters on the DAQ device. This design was chosen because the test site DAQ system employs a separate sensor PCB to perform signal conditioning before the LabJack T7 digitizes the signals. Thus, the DAQ device will assume that the signal conditioning for the low-speed analog inputs is performed externally, emulating the current system and keeping the DAQ device compatible with the hardware already developed for the test site.

C. ADC Sample Rates

Having decided on the anti-aliasing filter cut-off frequency for the high-speed analog inputs, the calculation to determine the sampling rate necessary on a single analog input is based on the Nyquist-Shannon sampling theorem [2]. Since the filter cut-off frequency is 28 kHz, the sampling rate must be greater than 56 kHz. However, this sampling rate is for a single analog input channel. As established in the previous section, the DAQ device will use three ADCs to sample 29 multiplexed inputs. Therefore, the required sampling rate of each ADC must be determined.

The minimum sampling speed required for the ADC can be calculated from the requirements. The 20 low-speed single-ended inputs must be sampled by a minimum of 50 Hz per channel which translates to an ADC sampling rate of 1 kHz. For the high-speed inputs, it was established that each channel must be sampled faster than 56 kHz. With five inputs in the high-speed single-ended group and four inputs in the high-speed differential group, the minimum ADC sampling speed is 280 kHz.

D. ADC Resolution and Input Voltage Range

One of the most important questions to answer in the design process is the resolution and input voltage range required for the ADC. These requirements are driven by the signals that must be sampled by the DAQ device. At the test site, the sensor with the highest sensitivity is a load cell with a differential output voltage whose sensitivity is $2.6 \mu\text{V}/\text{N}$ over a measurement range of 0 to 9000 N.

Knowing the sensitivity and measurement range of the sensor, a basic implementation could be to use the ADC to directly sample the output of the sensor. This approach imposes additional constraints on the ADC selection. Since the pressure transducer uses a differential voltage output, the ADC would need to have differential inputs. To resolve 1 N accurately, the ADC resolution would need to be at least 21 bits (ENOB, assuming an ADC reference voltage of 5 V). Moreover, most of the ADC input range is unused; at a maximum load of 9000 N, the load cell differential output is 23.4 mV. In comparison, the sensor with the second-highest sensitivity of $50 \mu\text{V}/\text{PSI}$ is a pressure transducer with a differential voltage output. This pressure transducer can measure pressures between 0 and 2000 PSI, so the maximum differential output is 100 mV.

A simple solution to solving the relatively high resolution requirements and inefficient use of the input measurement range of the ADC would be to reduce the ADC reference voltage from 5 V to, for example, 0.5 V. In doing so, the ADC resolution required to resolve 1 N on the load cell becomes approximately 17.5 bits. However, this approach is not feasible because some other sensors at the test site can output voltages greater than 0.5 V. Further, designing and testing a product that can accurately resolve voltages on the scale of $2.6 \mu\text{V}$ imposes significant challenges. MRT does not have equipment accurate enough to measure at that scale.

Instead, a different design was chosen. Based on the requirements, the DAQ device must be able to apply hardware voltage gain factors of 1 V/V, 10 V/V, 50 V/V, and 100 V/V. The hardware gain can be applied prior to ADC sampling, which relaxes the ADC resolution requirement. Assuming a gain of 100 V/V, the load cell output sensitivity, from the perspective of the DAQ device, becomes $260 \mu\text{V}/\text{N}$ and the maximum load cell output at a load of 9000 N would be 2.34 V. Correspondingly, the ADC resolution requirement drops from 21 bits to approximately 14.3 bits, assuming an ADC reference voltage of 5 V. Further, if the DAQ device only needs to resolve, for example, 5 N, then the ADC resolution requirement further relaxes to 12 bits.

After performing similar analyses and discussing with MRT, it was decided that the required ADC resolution is 12 bits (ENOB), and the ADC input measurement range is 5 V. With these specifications, the DAQ device will be able to resolve 5 N on the load cell, using a gain of 100 V/V, and 0.5 PSI on the pressure transducer, using a gain of 50 V/V. As shown in the block diagram in Fig. 2, differential inputs are converted to single-ended signals using an instrumentation amplifier (in-amp), which allows the same ADC component and anti-aliasing filter design to be used for both differential and single-ended high speed analog inputs.

E. ADC Selection

At this point, the minimum ADC sampling rates, the ADC resolution requirements, and the ADC input voltage measurement range have been established. With these specifications, an appropriate ADC can be selected.

The first ADCs that were investigated were the on-board ADCs in the microcontrollers being considered, which were the STM32F4, STM32F7, STM32H7, and i.MX RT1060X series of microcontrollers (the reasons for choosing these particular families of microcontrollers will be discussed in the next section). There are multiple advantages of using on-board ADCs. Namely, direct memory access (DMA) can be leveraged to reduce the computational load on the microcontroller; the component count in the DAQ device is reduced; and the need to write firmware drivers to interface with an external ADC using a digital communication protocol is eliminated. The disadvantages of on-board ADCs include limited input voltage range and limited resolution. Further, in the current era of widespread chip shortages, it is more difficult to find microcontrollers available for low volume purchases compared to discrete ADCs.

The STM32F4, STM32F7, and i.MX RT1060X series have internal 12-bit ADCs which are approximately 10.8 bits ENOB and can sample up to 2 million samples per second (Msps) [10]–[12]. Immediately, these series were disqualified from consideration because they fail to meet the ADC resolution requirement. Further, their input measurement ranges are from 0 to 3.6 V [10]–[12], which fail to meet the input measurement range requirement.

The STM32H7 series of microcontrollers have both 16-bit and 12-bit ADCs, which are 12.2-bit and 11.2-bit ENOB, respectively [13]. However, these parts also fail to meet the input measurement range requirement, and were also disqualified. Moreover, it was difficult to find a supplier with STM32H7 chips in stock for reasonable prices.

Having removed the internal ADCs from consideration, the search turned to external ADCs. To simplify firmware development later on, it was decided that the digital interface for the ADC would be either I2C or SPI because almost all microcontrollers have hardware peripherals for these interfaces. Given that the ADC sampling rate requirement is quite slow at a minimum of 280 kHz, the decision to use I2C or SPI did not impose undue additional constraints on the ADC selection process.

After searching on the Digi-Key website for ADCs that were in stock and fulfilled the requirements, the 14-bit (13.1 bits ENOB), 1 Msps Microchip MCP33151-10 [14] was chosen. This ADC interfaces over SPI using a simple interface. Although 1 Msps sampling rate is much higher than necessary, it provides room for expansion to higher sampling rates on the high-speed channels if desired.

F. Microcontroller Selection

Since this thesis project has a short timeline of one year, important considerations during the microcontroller selection processes included familiarity with the hardware and the software development process. The design of the DAQ device can be accelerated by using a microcontroller that the team has experience with. Over the last two years, the avionics team has used STM32 chips in the team's flight computers, becoming familiar with the vendor-provided hardware abstraction layer libraries and the software toolchain. At the same time, the Teensy 4.0, which uses an i.MX RT1062 microcontroller,

has been used for the team's ground station hardware. Therefore, the microcontrollers under review for the DAQ device are the STM32 series and the i.MX RT1060X series.

The STM32F4, STM32F7, and STM32H7 families are high-performance microcontrollers from STMicroelectronics. With hardware floating point units, USB capabilities, SDIO connectivity, and extensive SRAM and flash memory, they are powerful chips. Available in various quad flat pack (QFP) packages, they are easier to solder and inspect compared to the i.MX 1060X microcontrollers which are packaged in ball grid arrays (BGA), requiring X-ray machines to inspect the solder joints.

While the STM32 microcontrollers are easier to solder, the Teensy 4.0 and 4.1 boards break out many IO pins from the i.MX RT1062 chip into breadboard-compatible header pins. The i.MX RT1062 has a faster internal clock speed, rich set of peripherals, and can be programmed with the Arduino framework. Many developers in the Arduino community have dedicated considerable effort into optimizing libraries for the Teensy platform. Thus, it was expected that despite using the Arduino framework, the Teensy 4.0 and 4.1 could likely achieve similar performance to lower level code written for STM32 microcontrollers.

To compare the performance of the options listed above, experiments were conducted with a STM32F446ZE Nucleo evaluation board and a Teensy 4.0, interfacing with an MCP33151-10 ADC. The results, which will be presented in Section V, led to the decision to use the Teensy 4.1 for the DAQ device. The Teensy 4.1 uses the same microcontroller as the Teensy 4.0 but exposes more pins for use.

In addition to the results of the experimentation with the ADC, there are a few other compelling reasons that the Teensy 4.1 was chosen as the microcontroller. The Teensy boards are breakout boards with supporting circuitry already implemented. Thus, the amount of schematic and PCB layout design required on the DAQ device is reduced. Specifically, the Teensy 4.1 implements the following (not an exhaustive list): USB 2.0 high speed communication (instead of full speed), voltage regulation for the chip; Ethernet physical layer; microSD card interface over 4-bit SDIO; and footprints available for pseudo-static RAM (PSRAM) expansion. The Ethernet, SDIO, and PSRAM features are important for the DAQ device because the test site currently uses Ethernet to connect to the LabJack, SDIO provides a faster interface to microSD cards than SPI, and PSRAM can increase the RAM available to the microcontroller if needed. Further, the Teensy boards have similar cost to bare STM32 chips when purchasing in low volume, so selecting the Teensy boards also reduces cost.

G. Power Architecture

The power architecture design began with considerations for usability of the DAQ device. Adding a connector for an external power supply, such as a 5 V wall plug, would make the power system design easier than using the 5 V from the USB connector but make the device more difficult to use, since an additional power source would be required. Since the Teensy 4.1 was chosen as the microcontroller, 5 V USB power was chosen as the root of the power architecture design.

Based on the analog common-mode input voltage range requirements, the power rails for analog multiplexers and for the op-amps used in the anti-aliasing filters can be determined. ± 12 V rails were chosen because they satisfy the requirements and because the test site DAQ system currently uses these rails. However, these voltage rails need to be generated from the 5 V USB power. As such, switched-mode boost converters are used to generate ± 15 V power supplies that are post-regulated with linear low-dropout (LDO) voltage regulators to ± 12 V. Although the boost converters can directly generate ± 12 V supplies, the linear regulators help filter the noise and voltage ripple on the outputs of the boost converters.

The ADCs require a precision voltage reference to ensure that the conversions are accurate. The required ADC input measurement range is 0 to 5 V, so a 5 V reference is required. Although the voltage supply provided with USB 2.0 power is 5 V, it is not suitable for use as the ADC reference voltage for various reasons. According to the USB 2.0 specification [15], under the worst-case conditions, the supposed 5 V power supply that the Teensy 4.1 receives at its input can drop to 4.15 V, with respect to the ground

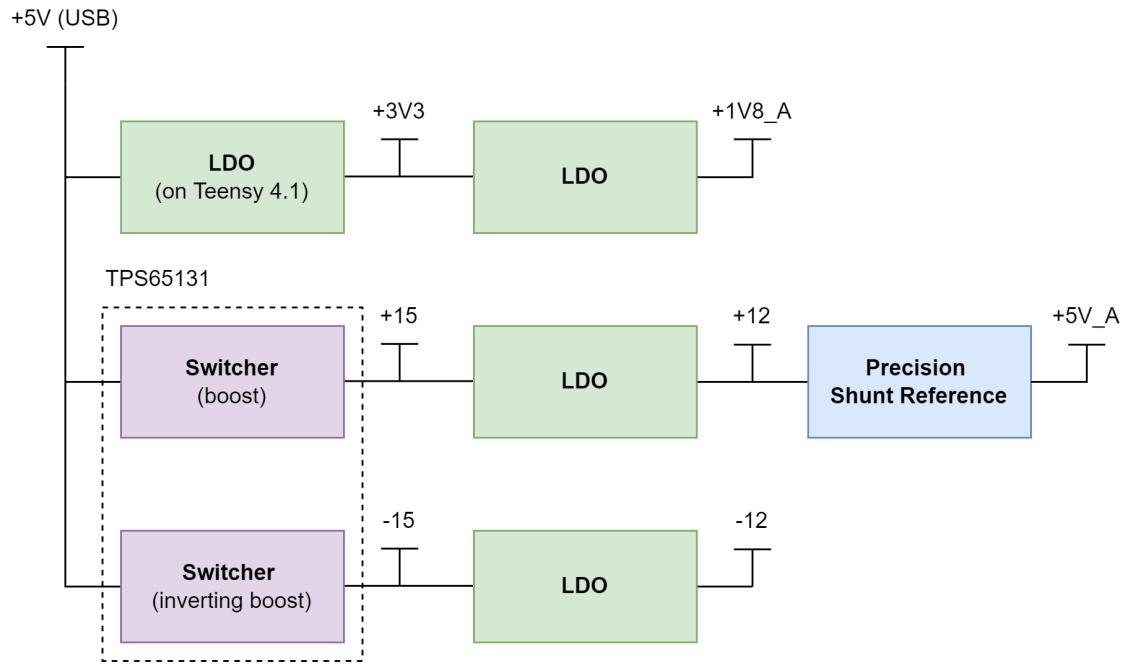


Fig. 5. Power architecture diagram for the DAQ device.

reference on the laptop. Further, the USB power supply contains noise from all of the digital switching circuits on the DAQ device and the host computer. Thus, a separate precision 5 V reference supply is used.

The ADCs also require a 1.8 V analog voltage supply and a 3.3 V digital IO voltage supply. The 3.3 V supply is provided by the 3.3 V output available from the Teensy 4.1 board, and an linear LDO regulator is used to generate the 1.8 V rail.

The decision to use USB power as the source for all the power on the DAQ device required careful consideration. USB power is limited to 500 mA by the USB 2.0 specification [15] which adds some constraints to the power architecture design. Early in the design process, the use of an external power supply, such as a battery, was considered. By using a suitably high external voltage supply, the current available for the DAQ device increases, and the noise and ripple on derived power rails can be potentially reduced by removing the boost converters from the power architecture and using linear LDO regulators only. However, power is already available from the USB connection; adding a requirement for a battery to make the device functional reduces its usability. With good design and sufficient filtering, the noise and ripple from the boost converters can be kept low enough to meet board performance requirements.

To ensure that the USB power specifications are met, a power budget, which can be found in Appendix A in the design calculations, was created to analyze the current draw on each power rail. It was found that the 500 mA is sufficient for the DAQ board in the current design. If the 500 mA USB power limit was exceeded during design, an additional power connector would have been used.

The chosen power architecture for the board is shown in Fig. 5, which summarizes the information presented above.

H. Relay Drivers

From the requirements, the DAQ device must control 24 relays. The current DAQ and control system at the test site has a PCB dedicated to the relays that is separate from the LabJack T7. This design enables separation of low-power, low-voltage control signals connected to the LabJack from high-power, high-voltage supplies that are switched by the relays, such as the 120 VAC mains voltage required for the heating blankets.

An alternative design would be to integrate the relays onto the DAQ device. In doing so, the external relay PCB can be eliminated and the entire DAQ and control system can be made more compact. However, this approach adds significant complexity to the DAQ device. To ensure that the DAQ device is flexible and safe, all relays on the DAQ device PCB would need to be routed to satisfy high voltage creepage and clearance constraints which increases board size and cost. Moreover, if different relays with higher current ratings are needed in the future, they would need to be pin-compatible with the relays on the DAQ device; otherwise, the DAQ device would need to be re-designed and re-ordered, adding significant expenses.

The chosen design follows the current implementation at the test site. Specifically, the DAQ device will have relay drivers on the board that interface with external relays through connectors on the board. Integrated low-side relay drivers were chosen as they are inexpensive and contain flyback protection, which reduces the component count on the DAQ device. This design also reduces the power consumed by the DAQ device because it does not have to source the power to drive relay coils. An additional advantage of this approach is that the relay board currently used at the test site will be compatible with the DAQ device.

I. IO Expansion

The requirements specify that various hardware peripheral ports for I2C, CAN, SPI, etc. must be available to expand the functionality of the DAQ device. Many of these peripherals are multiplexed onto the same pins on the Teensy 4.1. Thus, by careful pin assignment during schematic design, the IO expansion requirements can be easily met.

Initially, the requirements were interpreted as providing different pins for each of the hardware peripherals exposed for IO expansion. That is, two pins would be available for I2C data and clock, two pins for CAN, three pins for SPI data and clock, etc. However, this is difficult to achieve because the peripherals available on the pins on the Teensy 4.1 are multiplexed. Meeting the requirements under this interpretation would require significantly more pins for IO expansion, which would reduce the number of IO available for the rest of the DAQ device, such as for selecting between multiplexed analog inputs. Instead, IO pins that had the most peripherals available were selected to be exposed through connector pins.

The requirements also call for at least 8 analog inputs that are unique to the IO expansion for add-ons. This requirement was met by using 24 low-speed single-ended and 8 high-speed single-ended analog inputs. 4 of the low-speed inputs and 4 of the high-speed inputs are used to meet the analog inputs requirement for add-ons, and the remaining inputs meet the requirements for the number of channels in Section III-A.

J. MCP33151 Eval Board PCB Design

During the Fall 2022 semester, a PCB was designed to test the design of the circuits described above. The eval board serves as a smaller-scale test platform for the DAQ device. It implements the circuits designed above and meets many (but not all) of the requirements for the DAQ device. The eval board has fewer analog and relay channels than the DAQ device, which results in fewer components and smaller board size. Hence, it is a prototype of the DAQ device but at lower cost. Unless problems are found

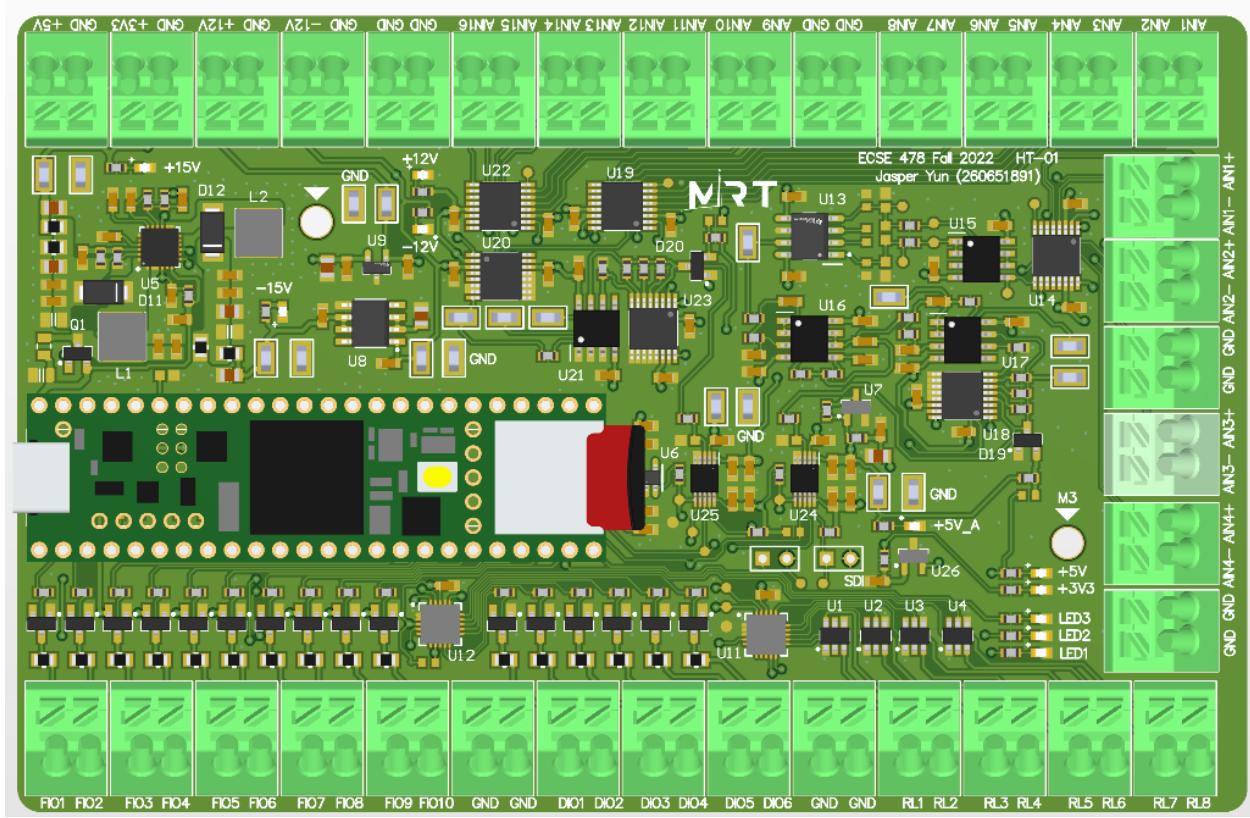


Fig. 6. Top view screenshot of the eval board, rendered in Altium Designer. The bottom side of the board does not have any components.

during with the eval board, the intention is to directly copy circuits from the eval board to the DAQ device after validation through testing. The board schematics are provided in Appendix B-A.

Fig. 6 shows a top view of the PCB as rendered in Altium Designer, which was the software used to design the PCB. Detailed descriptions of the design process for this board are outside the scope of this document.

A 4-layer board stackup was chosen and is presented in Table I. Using the two inner layers as ground planes allows the outer layers, which route the signals and power, to have their reference planes close by. This design improves the performance of the board compared to using 2 layers because power rails have lower inductance and high-speed digital signals have unbroken return paths.

TABLE I
MCP33151 EVAL BOARD STACKUP.

Layer	Usage
Top (L1)	Signal / Routed Power / Ground Pour
Inner 1 (L2)	Ground Pour
Inner 2 (L3)	Ground Pour
Bottom (L4)	Signal / Routed Power / Ground Pour

Since this board has both analog and digital signals, it was important to separate the two domains to prevent digital switching noise from coupling into sensitive analog signals. This separation is achieved through careful component placement. Fig. 7 shows the boundaries between the analog and digital

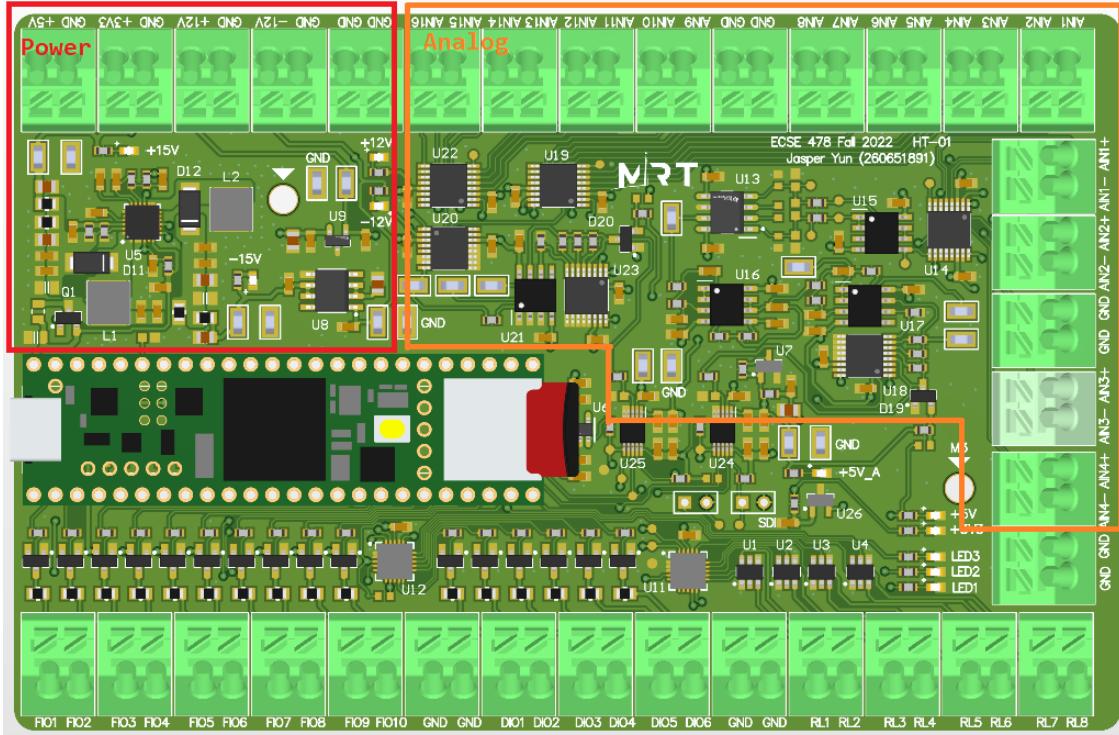


Fig. 7. Analog, digital, and power sections were partitioned on the eval board to reduce coupling between each section. The power section is inside the red rectangle on the top left, the analog section inside the orange box on the right side, and the rest of the board is digital.

sections. Further, the power management circuitry is placed far from both to ensure that switching noise from the boost converters does not couple into analog and digital signals.

The testing results of the eval board will be presented in Section V.

K. DAQ Device PCB Design

The DAQ device PCB was designed during the Winter 2023 semester after testing the eval board. The DAQ device design was similar to the eval board, but the issues found in the eval board and lessons learned during its testing were fixed. Further, the DAQ device implements the full feature set described by the requirements.

The DAQ device uses the same board stackup as the eval board. Most of the circuit schematics are the same as well, but small modifications have been made. For example, as will be seen in Section V, the anti-aliasing filter circuit on the eval board contributed approximately 30 mV of DC offset to signals. The offset was mostly removed by adding compensation resistors, and this was fixed for the DAQ device.

Fig. 8 shows screenshots of the top and bottom views of the PCB. The board was designed using Altium Designer using a similar approach to that used in the design of the eval board.

A major difference between the eval board and DAQ device is the types of connectors used. On the DAQ device, there are D-subminiature (D-sub) connectors similar to those on the LabJack T7 which are not present on the eval board. These D-sub connectors are included to facilitate wiring between the DAQ device and other circuit boards at the test site. However, the green terminal blocks are still included to allow quick, on-the-fly connections to be made.

The testing results of the DAQ device will be presented in Section V.

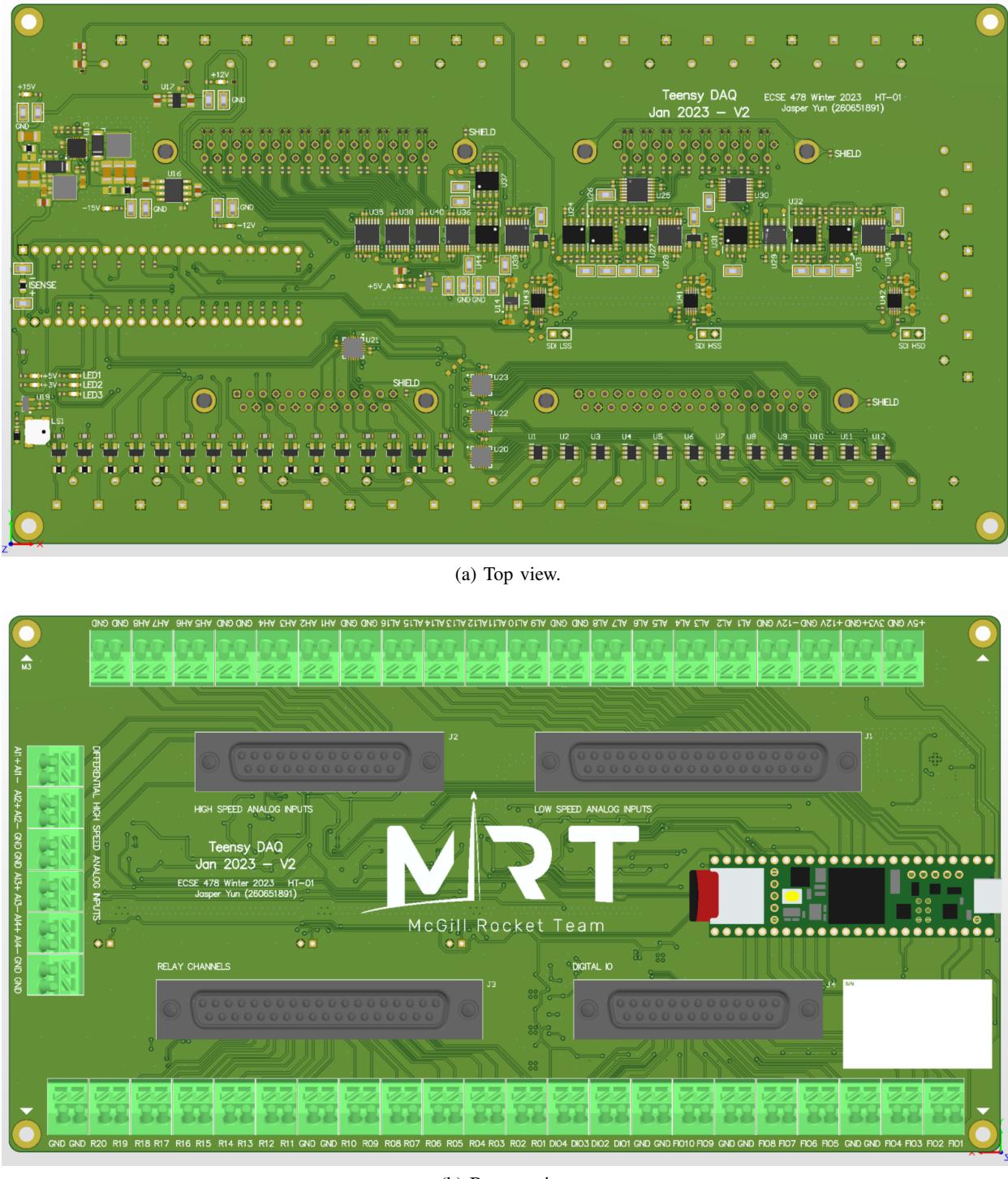


Fig. 8. Renders of the DAQ device board from Altium Designer.

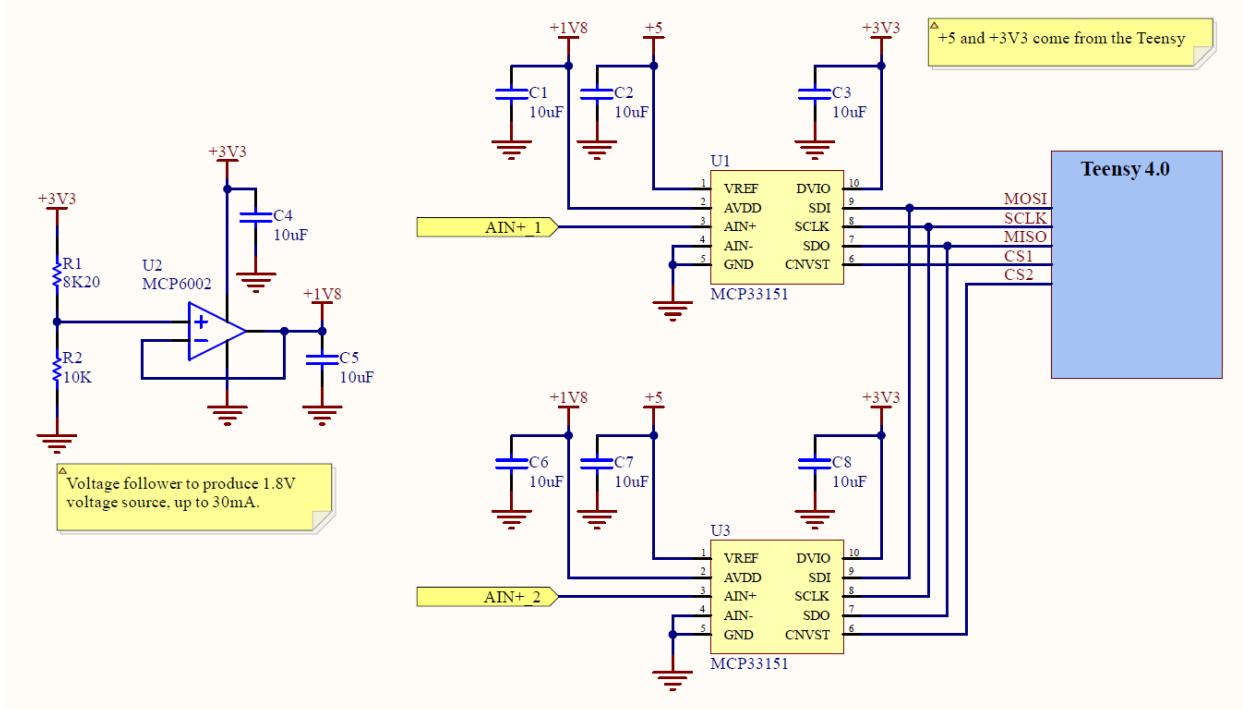


Fig. 9. Schematic of the perfboard prototype.

V. RESULTS

A. ADC Perfboard Prototype

A perfboard prototype was assembled with the MCP33151-10 ADC to experiment with the ADC, Teensy 4.0, and STM32 evaluation boards. The schematic and assembled board are shown in Figs. 9 and 10, respectively. Surface-mount decoupling capacitors are soldered on the bottom of the board.

The goals of experimenting with the perfboard were to determine whether the STM32 microcontroller families or the Teensy 4.0 and Teensy 4.1 had better performance, and what maximum sampling rates could be expected. Code was written for both platforms and the performance was observed.

SPI drivers were written for the STM32F446ZE Nucleo board and the Teensy 4.0 using the information provided by the MCP33151 datasheet [14]. For the STM32, two SPI drivers were written using the STM32 hardware abstraction layer (HAL) and lower layer (LL) libraries provided by STMicroelectronics; only HAL drivers were used for USB communication. The results are presented in Table II. Note that compiler code optimization was enabled (-O2) for the STM32 code, and the Teensyduino compiler was set to “faster”.

STMicroelectronics offers HAL and LL libraries for applications to interact with the hardware without using register-level accesses. However, the HAL library checks for valid accesses and errors, which contributes to significant latency and reduces the fastest possible sampling rate for the ADC. On the other hand, the LL library basically only provides names for registers and functions to access registers; thus, it is the responsibility of the users to ensure that their code is valid. The performance difference is evident from the results in Table II; the sampling speed results are presented in kilo samples per second (ksps). However, none of the STM32 results are at the same performance level as the Teensy 4.0.

The Teensy 4.0 outperformed the STM32F446ZE quite significantly. This can likely be explained by a few reasons. Firstly, the Teensy 4.0 has a core clock speed of 600 MHz, which can be increased through overclocking, whereas the STM32F446ZE has a lower maximum core clock speed of 180 MHz.

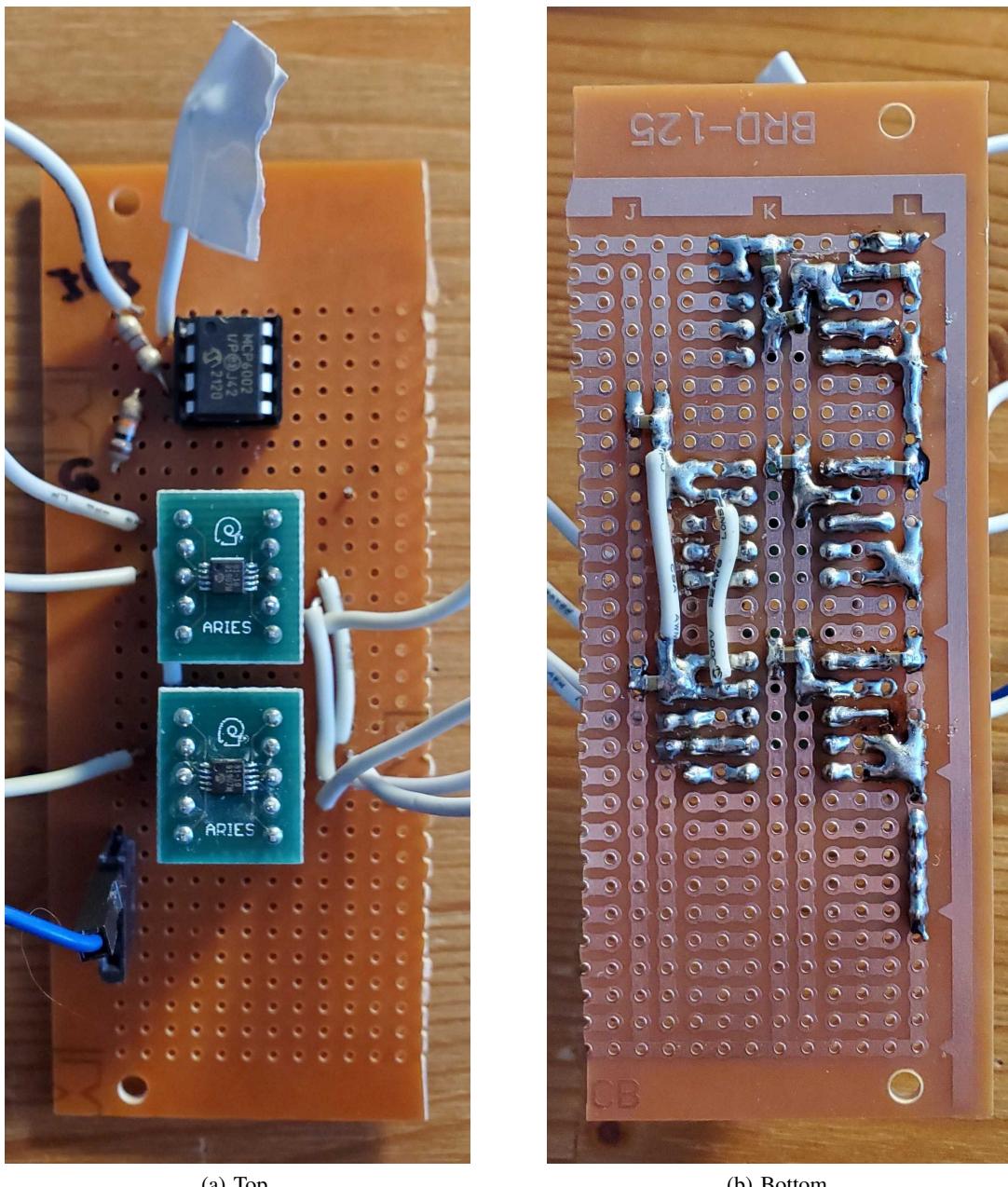


Fig. 10. Pictures of the assembled perfboard for experimenting with the MCP33151-10 ADC. Surface-mount decoupling capacitors are soldered on the bottom.

TABLE II
PERFBOARD PERFORMANCE EVALUATION RESULTS.

Microcontroller	SPI clock (MHz)	Sampling rate (ksps)	Loop description
STM32 (HAL)	42	2.164	Poll ADC, calculate voltage, transmit over USB.
STM32 (LL)	42	22.321	Poll ADC, calculate float, transmit over USB.
STM32 (LL)	42	267.379	Poll ADC, calculate float.
Teensy 4.0	42	675.000	Poll ADC, calculate float, transmit over USB.

Secondly, the Teensy 4.0 and STM32F446ZE use different ARM cores, which are the ARM Cortex-M7 and Cortex-M4 cores, respectively. Thus, the Teensy 4.0 is designed for higher performance.

The results obtained during this testing were a significant factor in choosing to use the Teensy 4.1 as the microcontroller for the DAQ device. Due to the better sampling rate results, built-in USB High Speed instead of USB Full Speed (480 Mbps vs. 12 Mbps), and Ethernet availability through an add-on board, the Teensy 4.1 was chosen over STM32 microcontrollers. The Teensy 4.1 was selected over the Teensy 4.0 because both boards use the same microcontroller but the Teensy 4.1 has more IO pins available.

B. Eval Board – Characterization of Power Supplies

Preliminary testing results have been obtained for the MCP33151 evaluation board. The PCBs arrived during the week of November 21 and were manually assembled by the author shortly afterwards. The board was soldered in sections so that separate circuits could be tested individually. The power supply section was assembled first to ensure that the generated voltage rails are within expected values; otherwise, circuit components powered by the generated voltage rails could be damaged. Then, after verification of the power supplies, the analog and digital sections were soldered.

After the power supplies' components were assembled on the board, as shown in Fig. 11, the voltage regulation circuitry was checked. Using a digital multimeter and oscilloscope, the average voltage on the rails, ripple voltage, and noise were measured. However, these measurements were not representative of the performance of the power supplies because the power rails were not loaded, meaning they were not supplying the currents needed to operate the whole device. Thus, after verifying that the voltages on the power supplies were within the designed values, the rest of the board was assembled. The voltage rails were measured again with the board drawing its quiescent current. The results are presented in Table III. Frequency measurements with “n/a” denote oscilloscope measurements where the noise and ripple waveforms did not show periodic signals. A picture of the fully-assembled board is shown in Fig. 12.

Care was taken during the power rail measurements to ensure that the results are accurate. To that end, the default multimeter probes were switched to hook probes so that a secure, constant connection could be made to the test points on the board. For the oscilloscope, the 200 MHz 10x probe used a ground spring instead of the typical ground wire with an alligator clip in order to minimize the inductance of the probe. The oscilloscope input was AC-coupled and bandwidth-limited to 20 MHz. Fig. 13 shows an image of the probing, and Fig. 14 is a screen capture from the oscilloscope measurement of the 15 V rail. Appendix B-B contains oscilloscope screenshots for the measurements of the other voltage rails.

Table IV presents the minimum, nominal, and maximum voltages expected on each rail which were computed during the design process. Although the values of the average voltage measurements in Table III were slightly different than the nominal values from the design calculations, all of the voltage rails are within the tolerances specified by device datasheets and the design calculations. Refer to Appendix A for detailed design calculations.

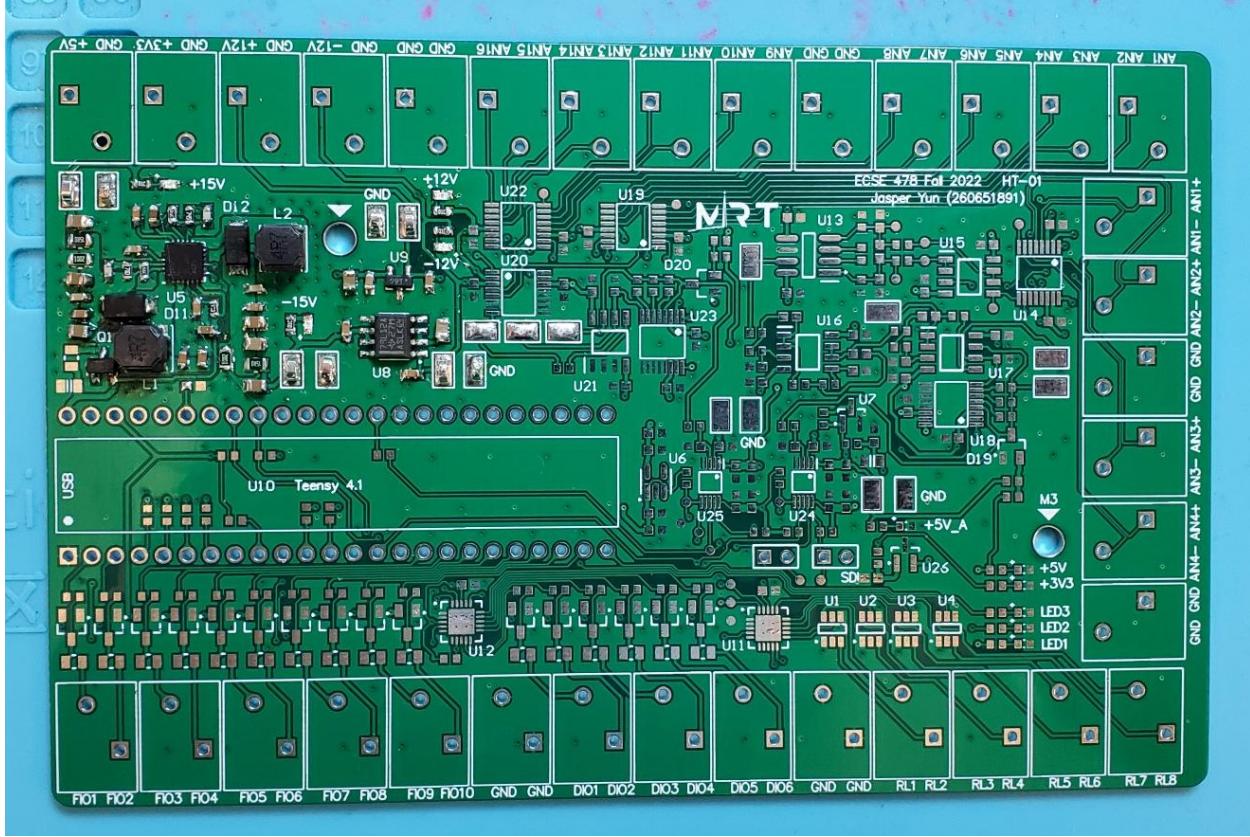


Fig. 11. Top view photograph of the power supply circuitry soldered to the eval board.

TABLE III
MCP33151 EVAL BOARD POWER SUPPLY MEASUREMENTS WITH RAILS LOADED.

Rail Voltage (V)	Average Voltage (V)	Ripple (mVpp)	Frequency (kHz)
+15	14.885	224.00	20.41
-15	-14.533	188.00	25.00
+12	11.909	21.40	n/a
-12	-12.270	12.80	25.00
+5 (analog)	4.999	12.00	n/a
+1.8 (analog)	1.803	10.20	n/a

C. Eval Board – Low-Speed Single-Ended Analog Inputs

The analog multiplexers for the 16 low-speed single-ended analog inputs and non-inverting gain stage were tested on the eval board. First, the firmware needed to switch between multiplexer channels was written for the Teensy. After verifying that each channel selected by the Teensy in the firmware corresponded to the correct connector on the board, the selectable gains were tested. Using a DC power supply and two multimeters, the input voltage to the analog input, input to the ADC, and the value measured by the ADC (read on the Teensy 4.1) were recorded in Table V. Using the measurements, the gain and offset of the gain stage were calculated in Table VI.

The test was set up as follows. Power to the board was provided over the USB connector on the Teensy 4.1, as this is how the DAQ device will likely be powered at the test site. The DC power supply was set to a small voltage value and connected to the analog input. The first multimeter measured the voltage at the analog input. The second multimeter measured the voltage at the input of the ADC. The ADC

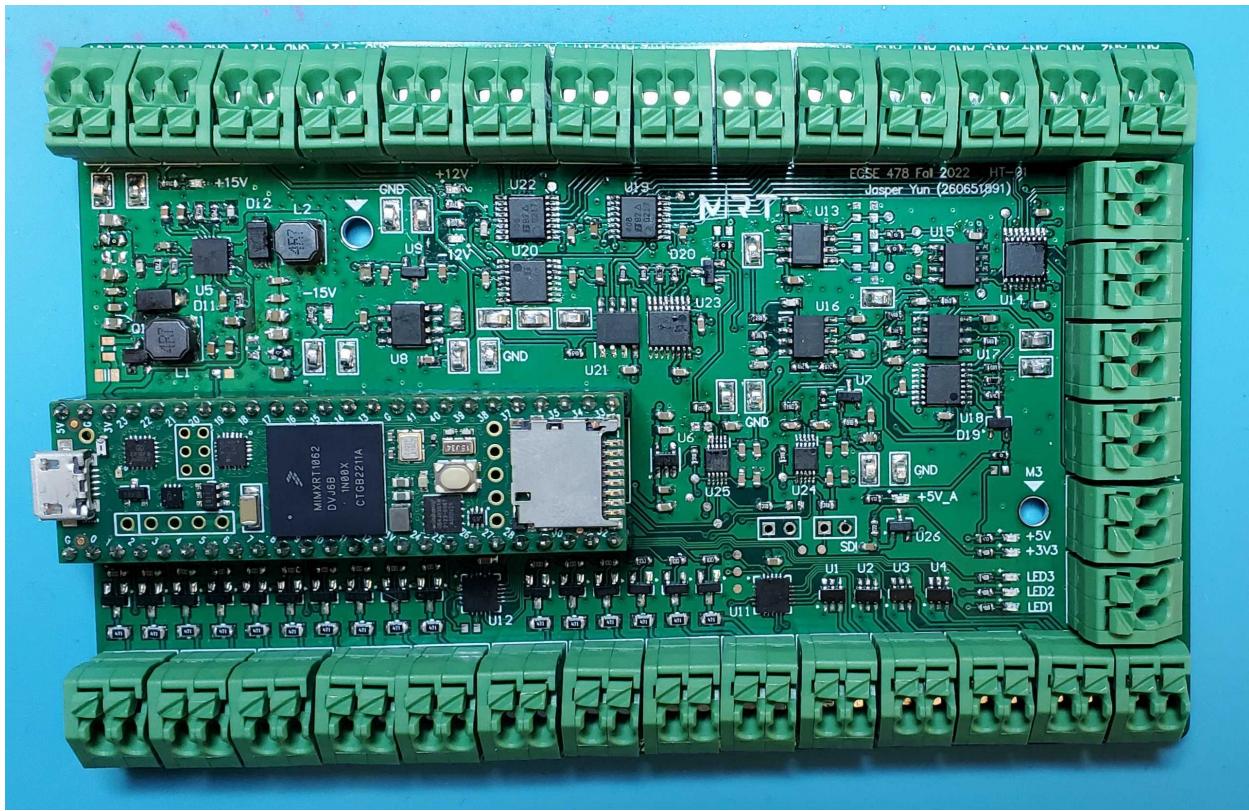


Fig. 12. Top view photograph of the fully-assembled board.

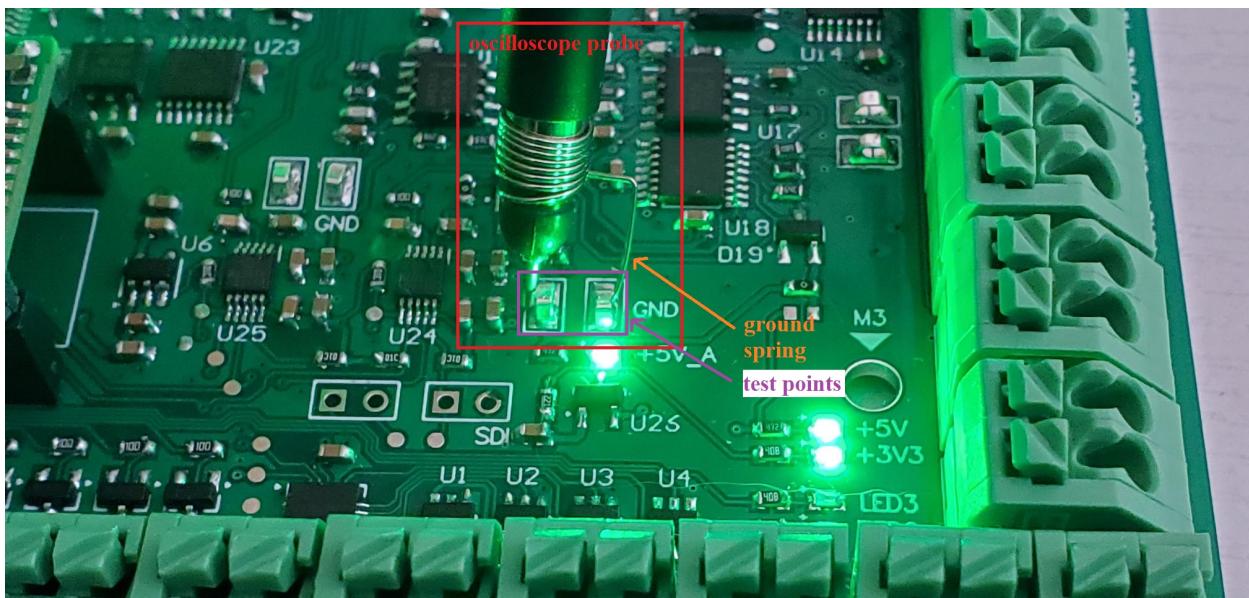


Fig. 13. The oscilloscope probing method used to measure the ripple and noise on the power supply circuitry outputs used a ground spring to minimize inductance of the probe.

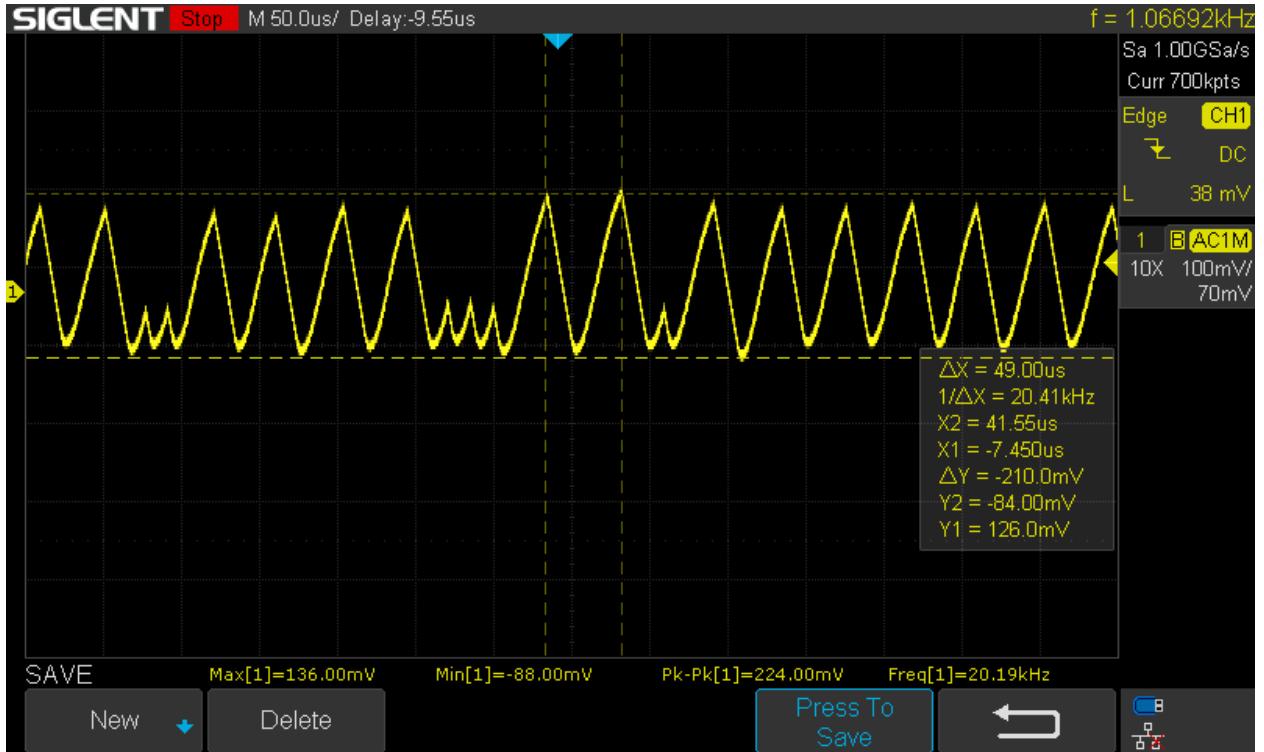


Fig. 14. Screen capture from the oscilloscope measurement of the 15 V rail. The input was bandwidth-limited to 20 MHz, AC-coupled, using a 10x passive probe.

TABLE IV
POWER SUPPLY VOLTAGE OUTPUT TOLERANCES.

Rail Voltage (V)	Minimum (V)	Nominal (V)	Maximum (V)	Average Measured (V)
+15	14.463	14.901	15.327	14.885
-15	-15.155	-14.709	-14.263	-14.533
+12	11.400	12.000	12.600	11.909
-12	-12.600	-12.000	-11.400	-12.270
+5 (analog)	4.995	5.000	5.005	4.999
+1.8 (analog)	1.773	1.800	1.827	1.803

reading results in Table VI were the averaged result of 1000 readings taken at 50 Hz, with the goal of averaging out the noise from the power supplies and on the board itself.

In the design calculations, the range of gain settings were calculated according to the tolerances of components in the amplifier circuit (resistors, analog multiplexer on-state resistance, etc.). The calculation results are presented in Table VII with comparison to the hardware gain results from Table VI.

Evidently, the measured hardware gains were slightly higher than the maxima specified by the design calculations. However, there are a few potential sources of error in both the measurements and the design calculations. The multimeter used to measure the input voltage had limited digits after the decimal point, and the voltage was not constant over the course of the 1000 ADC measurements; the input voltage measurement presented in the results is a best estimate of the average voltage viewed by the experimenter. The input voltage could be stabilized by adding heavy filtering or by using a precision voltage reference, which was unavailable at the time of testing. Additionally, the design calculations did not consider non-ideal behaviors of the op-amp, such as input offset voltage. Nonetheless, these results are promising validations of the design calculations and the design. The high-speed analog inputs use the same gain

TABLE V
LOW-SPEED SINGLE-ENDED ANALOG INPUT ADC MEASUREMENTS.

Gain Setting (V/V)	Input (mV)	Hardware Output (V)	ADC Averaged Reading (V)
1	27.10	0.0283	0.02559
10	27.10	0.2746	1.35090
50	27.10	1.3509	1.33066
100	27.10	2.7422	2.70696
1	37.20	0.0385	0.03504
10	37.20	0.3771	0.37025
50	37.20	1.8555	1.85100
100	37.20	3.7708	3.76934

TABLE VI
LOW-SPEED SINGLE-ENDED ANALOG INPUT GAIN STAGE GAINS AND OFFSETS.

Gain Setting (V/V)	Hardware Gain (V/V)	Offset (mV)
1	1.00990	0.93168
10	10.14851	-0.42475
50	49.96039	-3.02673
100	101.84158	-17.70693

stage circuit and similar PCB layout, thus the high-speed analog inputs were not tested.

D. Eval Board – Anti-Aliasing Filter Magnitude Response

The anti-aliasing filter on the high-speed differential-ended inputs is an important part of the DAQ device. Extensive testing was performed to ensure that the circuit performs as expected. Since the filter design was simulated in LTspice, the frequency response of the circuit on the eval board was tested and compared to the simulation results.

To generate a differential-ended signal, a signal generator was setup to output a 1.00 Vpp sine wave with 2.00 V DC offset and a bench power supply was used to provide a constant 1.50 V output. These two signals were input to channel 1 of the differential inputs. The voltage output of the filter was measured as the frequency of the sine wave was manually varied to determine the magnitude response of the filter, which is shown in Fig. 15 with the LTspice simulation results.

The measured magnitude response corresponds well to the simulated response from LTspice. At measurements above 100 kHz, the amplitude of the filter output signal was almost indistinguishable from the noise on the oscilloscope, so there is potential for error in the measurements. With a sine wave input of 1.00 Vpp and around –60 dB of attenuation, the filter output should be around 1 mV, which was difficult to distinguish on the oscilloscope, even with the oscilloscope acquisition mode set to averaging.

Since the magnitude response matched simulation results, the phase response was not measured. It is expected that the phase response also matches simulation results. During testing of the filter, there was noticeable phase shift as the frequency of the input signal was increased.

TABLE VII
CALCULATED GAIN TOLERANCES OF THE NON-INVERTING GAIN STAGE.

Gain Setting (V/V)	Minimum (V/V)	Maximum (V/V)	Actual Gain (V/V)
1.00	1.008	1.025	1.00990
10.00	10.068	10.121	10.14851
50.00	49.705	49.820	49.96039
100.00	100.808	101.225	101.84158

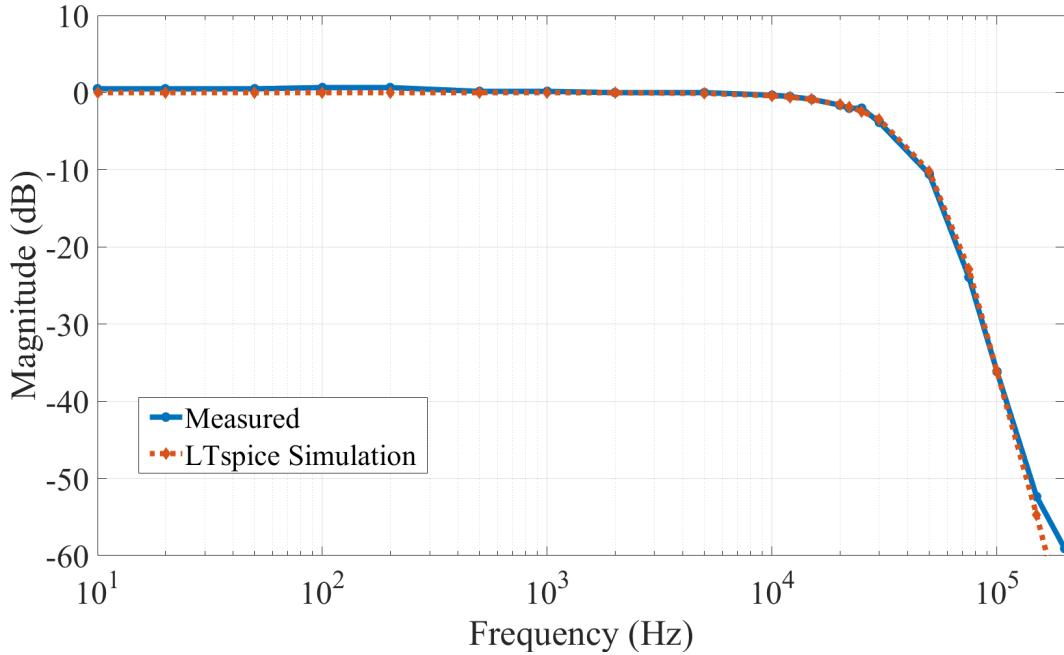


Fig. 15. Eval board anti-aliasing filter magnitude response, measured vs. simulated.

E. Eval Board – Anti-aliasing filter DC Offset

While testing the device, it was discovered that the anti-aliasing filter added around 30 mV of offset to the signal. This offset was found to be almost constant across frequency. Since the eval board and DAQ device use ADCs which interface with microcontrollers, this DC offset could be accounted for in the board firmware. However, the firmware approach is not suitable because the anti-aliasing filter is followed by a gain stage which would amplify the offset.

Recall that the gain stage can be configured to provide 1 V/V, 10 V/V, 50 V/V, and 100 V/V of gain in hardware. Thus, the 30 mV of offset would be amplified to 30 mV, 300 mV, 1.5 V, and 3 V, respectively, for each gain setting. As the input measurement range of the ADC is 0 to 5 V, it is clear that the offset added by the filter must be minimized.

The LTspice simulation did not show any noticeable DC offset from the input to the output of the filter. Therefore, the datasheet for the op-amp used in the filter was examined, and it was hypothesized that the cause of the offset was due to input bias currents of the op-amp. Fig. 16 shows the schematic of the anti-aliasing filter on the eval board. The RC4580 op-amp has a bipolar input stage [16]. The input bias currents are drawn through the two resistors on the non-inverting input of each op-amp, leading to a voltage offset which is directly carried to the next stage of the filter through the direct connection between the inverting and output terminals of the op-amp.

To test the hypothesis, the eval board was reworked to add input bias current compensation resistors between the inverting and output terminals of the op-amps in the filter. The schematic of the reworked circuit is shown in Fig. 17. After testing the filter again, the DC offset was reduced from 30 mV to 0.3 mV. Pictures of the reworked parts of the board are shown in Fig. 18.

F. DAQ Device – Pictures of Assembled PCB

Pictures of the top and bottom view of the assembled DAQ device board are shown in Fig. 19.

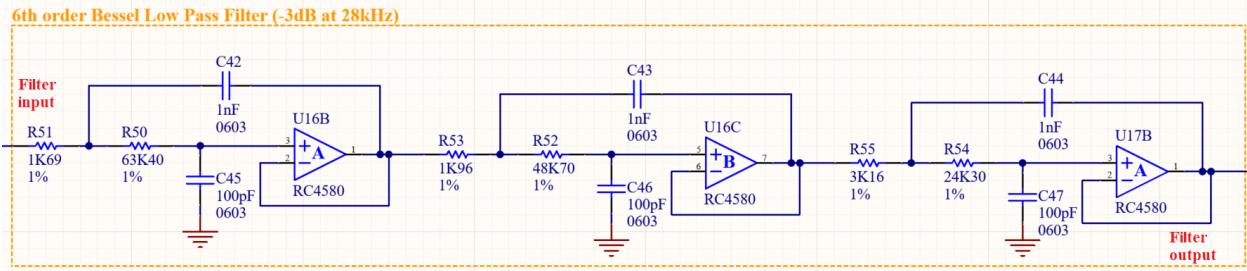


Fig. 16. Eval board anti-aliasing filter schematic, as manufactured.

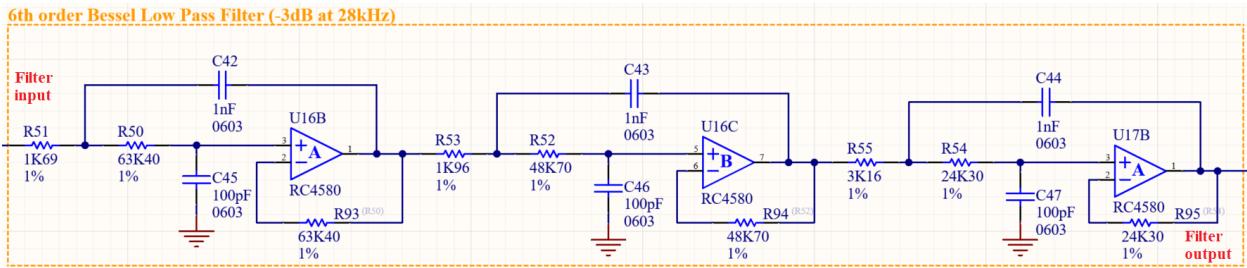


Fig. 17. Eval board anti-aliasing filter schematic with compensation resistors to reduce the offset voltage.

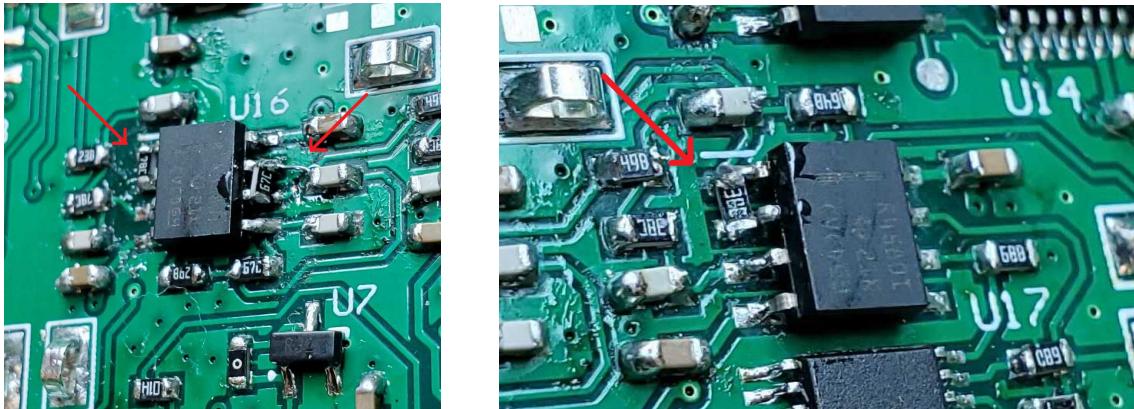
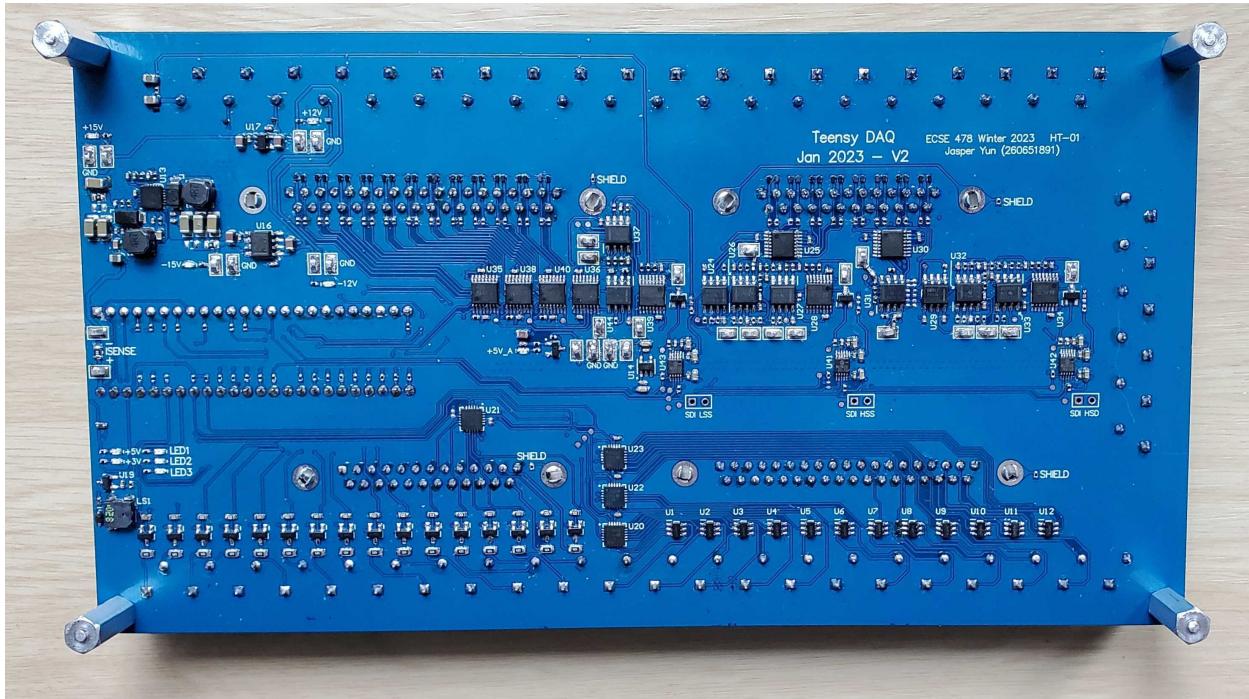


Fig. 18. Reworked eval board to add input bias current compensation resistors.

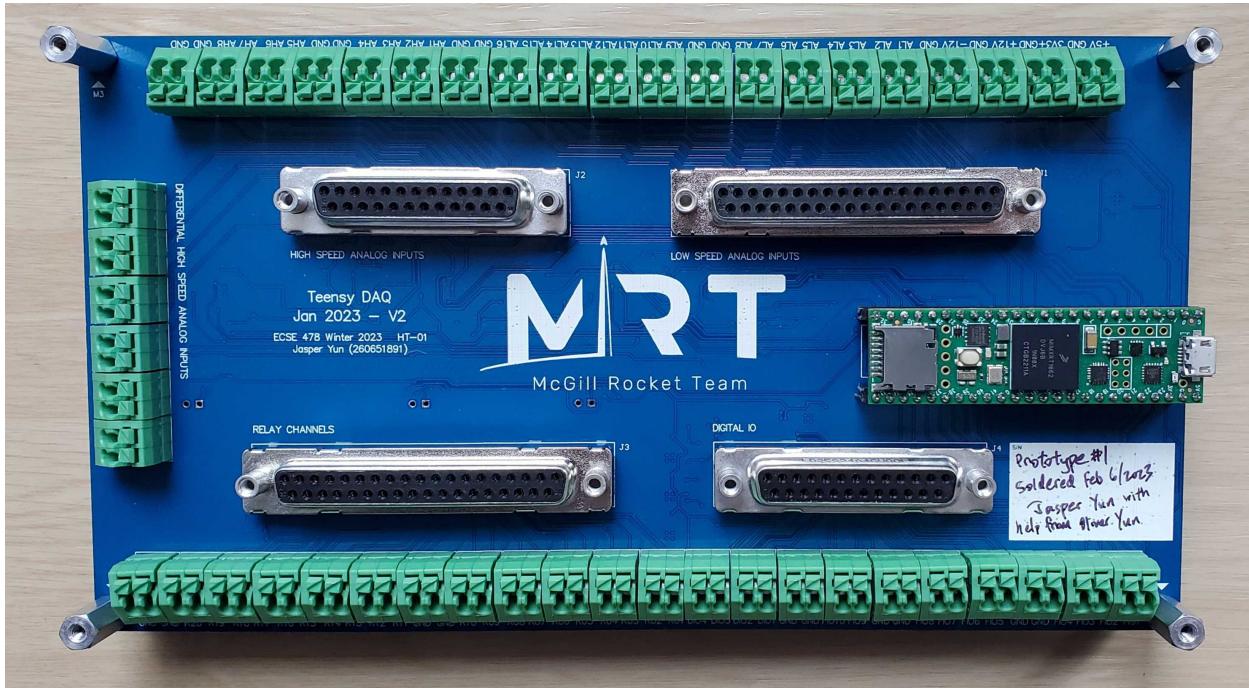
G. DAQ Device – Characterization of Power Supplies

The power rails on the DAQ device were measured Using the same testing methodology as the eval board. The results are presented in Table VIII. Compared to the eval board, the ripple voltages on the DAQ device are all lower, perhaps because the eval board was powered by a phone charger wall adapter whereas the DAQ device was powered by a bench power supply. For better comparison, the measurements should be re-done when both boards are powered by the bench power supply; however, comparing the performance between the eval board and DAQ device is not the goal of this project.

The voltages on the power rails were all within the tolerances given by the design calculations.



(a) Top view.



(b) Bottom view.

Fig. 19. Assembled DAQ device PCB views.

TABLE VIII
DAQ DEVICE POWER SUPPLY MEASUREMENTS WITH RAILS LOADED.

Rail Voltage (V)	Average Voltage (V)	Ripple (mVpp)	Frequency (kHz)
+15	14.485	76.80	22.73
-15	-14.183	64.80	21.28
+12	11.969	6.80	21.28
-12	-12.267	4.40	n/a
+5 (analog)	5.000	10.60	n/a
+1.8 (analog)	1.801	7.00	n/a

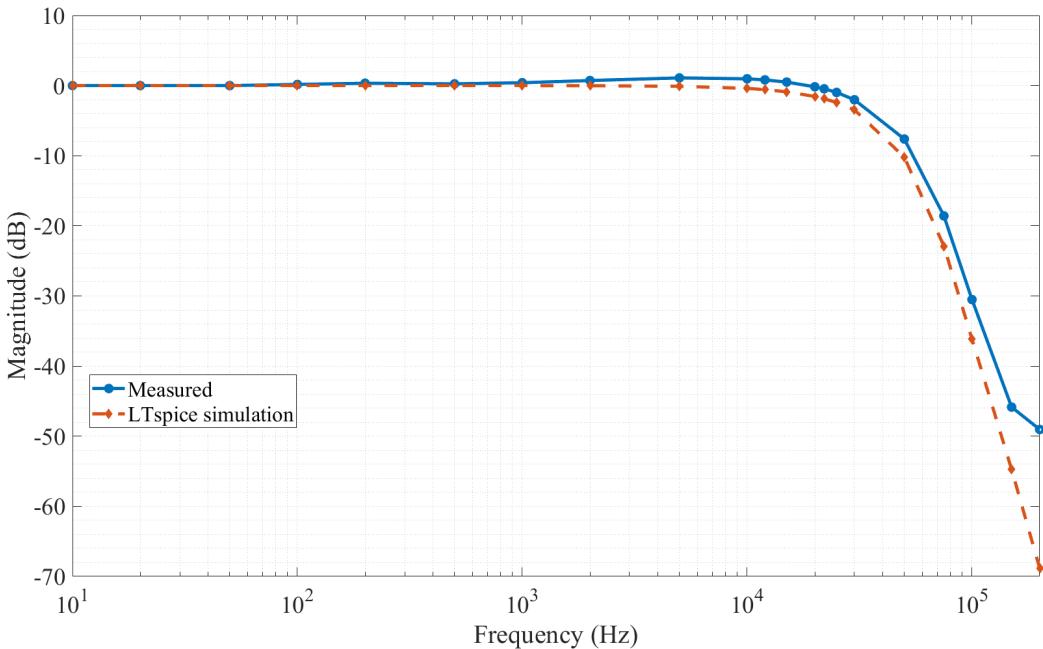


Fig. 20. DAQ device anti-aliasing filter magnitude response measurements vs. LTspice simulation results.

H. DAQ Device – Anti-Aliasing Filter Magnitude Response

The magnitude response of the anti-aliasing filter on the high-speed single-ended analog inputs was measured. The results are plotted in Fig. 20 with comparison to the LTspice simulation results.

The measured response mostly aligns with the simulated response, except at high frequencies above 100 kHz. A possible explanation for the small difference between the simulated and measured response could be the component tolerances of the resistors and capacitors used in the filter. Regardless, the filter behaves as a low-pass filter and will perform filtering to prevent aliasing.

The offset voltage across the anti-aliasing filter on the high-speed single-ended analog inputs was 0.82 mV with a grounded input. The offset voltage across the anti-aliasing filter on the high-speed differential-ended analog inputs was -0.03 mV with grounded inputs. These results are acceptable as they do not significantly reduce the input voltage range of the analog inputs even when using the 100 V/V gain configuration.

I. DAQ Device – High-Speed Single-Ended Analog Inputs

The gain stage on the high-speed single-ended analog inputs was tested and the results are presented in Table IX. The gain stage circuit is identical between the low-speed single-ended, high-speed single-

ended, and high-speed differential analog inputs, therefore only the high-speed single-ended inputs were measured. The other inputs were tested without measuring the results.

The gain stage was tested by providing a 1 kHz sine wave input and measuring the input and output of the gain stage. For each gain setting, the amplitude of the input wave was correspondingly reduced to avoid clipping on the output due to the Schottky diodes present on the output of the op-amp to provide overvoltage and undervoltage protection for the ADC. For this test, the gain of the gain stage is defined as the peak-to-peak output voltage divided by the peak-to-peak input voltage as measured by the oscilloscope in averaging acquisition mode.

TABLE IX
HIGH-SPEED SINGLE-ENDED ANALOG INPUT GAIN STAGE GAINS.

Gain Setting (V/V)	Minimum (V/V)	Maximum (V/V)	Actual Gain (V/V)
1.00	1.008	1.025	1.043
10.00	10.068	10.121	10.191
50.00	49.705	49.820	49.585
100.00	100.808	101.225	99.697

Compared to the expected gain from the design calculations, the actual gains are very close but slightly beyond the minimum and maximum gains. However, this is not a problem because the gain can and should be compensated for in the DAQ device firmware.

J. DAQ Device – High-Speed Differential-Ended Analog Inputs

The only difference between the high-speed single-ended and high-speed differential-ended analog inputs is the use of an instrumentation amplifier to convert differential inputs to single-ended inputs. As such, the performance of the circuitry that is the same between both circuits is expected to be very similar. Consequently, the differential-ended inputs were tested quickly by using a signal generator and DC power supply to provide differential inputs and verifying that the output of the gain stage was as expected. Indeed, the differential analog inputs behaved as expected.

K. DAQ Device – Relay Channels

The relay channels on both the eval board and DAQ device were tested in the same way. A schematic of the test setup is shown in Fig. 21. Relays were setup on a breadboard with an external 5 V power supply. Light-emitting diodes (LEDs) were connected to the relay contacts to act as loads to visualize whether the relays actuated correctly. The relay coils were controlled by the relay drivers on the DAQ device.

All relay channels were successfully controlled by the eval board and DAQ device.

L. DAQ Device – Flexible and Digital IO Channels

As a first test for the digital IO channels to verify that the firmware was correctly written and the hardware was functioning correctly, LEDs were connected to each channel and blinked sequentially. This test was successful.

To verify that the flexible IO and digital IO channels can be used for digital communication with add-ons, a simple test was conducted with an Adafruit BME280 breakout board [17] which can measure temperature, barometric pressure, and relative humidity. The BME280 communicates with microcontrollers over I2C or SPI; in this test, I2C was used. Using the Adafruit Arduino library for the BME280 [18], the DAQ device successfully communicated with the sensor.

Since all of the digital channels were able to blink LEDs and the I2C-capable channels successfully communicated with an external I2C device, all of the digital IO channels were assumed to be functioning correctly.

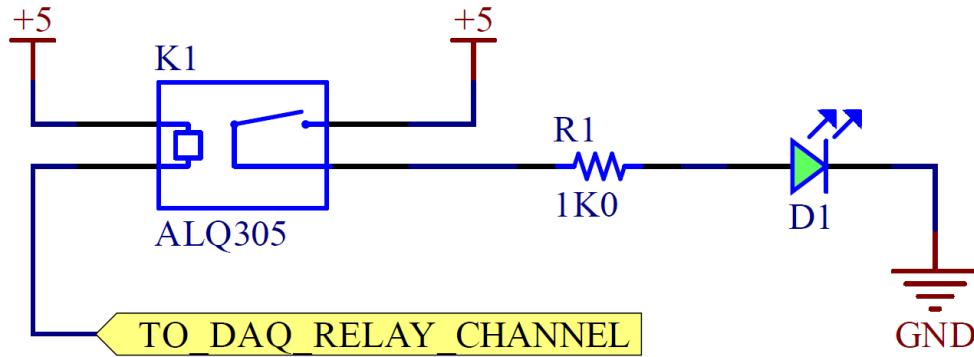


Fig. 21. Relay channel test schematic. The GND on the LED is connected to the DAQ device GND.

M. DAQ Device – Final Device Cost

The hardware cost of the DAQ device was compiled using the bill of materials (BOM) for the PCB and pricing data from MRT's preferred vendors. The prices of components were looked up on Digi-Key's website. The price of the PCB was quoted on JLCPCB's website. The pricing data lookup and USD to CAD currency conversions were performed on March 25, 2023.

It is important to note that MRT receives a 10% educational discount on most components from Digi-Key because the team has a sponsorship agreement with Digi-Key. Most educational groups should be able to contact Digi-Key and benefit from their sponsorship.

JLCPCB manufactures a minimum of 5 PCBs when an order is placed. As such, the price of the PCB is calculated as the quoted cost divided by the number of boards being ordered. In this case, the number of boards is 5, since the team is unlikely to order more than 5 of the DAQ device PCB in a single order.

The total components cost was found to be \$301.56 CAD, excluding tax. The cost for 5 PCBs was \$62.75 CAD (converted from \$45.60 USD), resulting in a cost per board of \$12.55 CAD. Thus, the total cost for the assembled DAQ device is \$314.11 CAD. This total can be reduced by depopulating the terminal blocks and/or the test points if they are found to be unnecessary. The price breakdown is provided in Appendix C-A with the BOM.

Compared to the cost of a LabJack T7, which is \$715.54 (converted from \$520 USD), the DAQ device costs 56.1% less than the T7. This large cost reduction is made possible by the fact that MRT is composed of students who dedicate their extracurricular time to the team and are not paid to do so. Therefore, the monetary cost of labor for assembling the hardware and software development is saved. To that end, this thesis project has achieved its goal of developing a low-cost, in-house DAQ device for MRT.

VI. IMPACT ON SOCIETY AND THE ENVIRONMENT

A. Use of Non-Renewable Resources

PCBs are composed mostly of FR4, copper, and tin or gold. Components that are populated on the board typically use some metals and plastic packages. Overall, bare PCBs and assembled PCBs have little recycling value because the amounts of copper, tin, and other precious metals are low. Thus, to make recycling economical, large volumes of PCBs are required. However, MRT does not produce or purchase PCBs in large volumes. Thus, boards go into the landfill when they reach their end of life. The development of the DAQ device hardware uses non-renewable resources only.

B. Environmental Benefits

Since this project is open-source, it is better for the environment than similar closed-source projects. Open-source projects are much more repairable than closed-source projects because, depending on how much of the project is open-sourced, the schematics, PCB layout, and user manuals are available and do not try to hide information from the end user. In comparison to the closed-source LabJack T7, hardware problems typically require returns to the vendor for repair, which adds carbon emissions due to shipping to and from the vendor. Further, closed-source products can contribute to more electronic waste generation because they are less repairable. With open-source products, problems can probably be fixed without buying a replacement.

C. Safety and Risk

With the current DAQ system at the test site based around the LabJack T7, the data recorded in past hot-fire tests has been valuable for identifying points of improvement in the design of the team's rocket engines. The team has been able to make its engines more performant over consecutive successful hot-fire tests. However, the sampling rates used for instrumentation are inadequate to fully characterize the performance of the rocket engines under test. According to literature [5], there may be high frequency signal content indicating the presence of combustion instabilities. Without sufficiently high sampling rates, these signals cannot be recorded accurately. This problem extends to all of the analog signals being recorded, not just those that may indicate combustion instabilities.

The DAQ device aims to solve this problem and provide higher sampling rates. In doing so, the team will be able to accurately characterize all parts of the engine. With more knowledge of the system, there is increased safety and reduced risk because the behavior of the engine is known in greater detail. Further, being able to identify more flaws in the engine design during testing campaigns means that the team can fix them rather than repeatedly testing iterations of the engine until it performs a rapid unscheduled disassembly. Being able to find problems is one of the first steps to fixing them. Consequently, the team will have more confidence in the performance of its engines at competitions.

D. Benefits to Society

A low-cost, open-source DAQ device with relatively high sampling speeds affords teams with small budgets, such as student design teams and startup companies, access to DAQ equipment with performance comparable to commercial devices which cost much more money. Thus, these teams can compete with teams that have better financial resources, and more market competition leads to better products for society. For the teams that are willing to take time to learn how the DAQ device functions, they have the additional advantage of being able to tailor the device to their needs by changing the hardware or firmware.

Since this project is sponsored by MRT, this device offers an additional benefit to team members that are interested in analog electronics. The design, testing, and documentation can teach engineering students on the team more about real-world analog circuit design considerations and implementation. These students would acquire more experience with practical engineering processes, thus developing better future engineers which benefits society.

VII. CONCLUSION

Over the course of the Winter 2023 semester, the DAQ device design was finished and it was tested. The DAQ device schematics and PCB layout were completed at the beginning of the semester, incorporating the lessons learned from the testing of the eval board. The DAQ device was ordered, manufactured, and manually assembled. From there, firmware was written to enable testing of the various features of the DAQ device.

At this point, the hardware has been tested and performs as expected. However, further development is needed to make this device a usable tool for MRT. The application software must be designed and implemented. The hardware must also be more extensively tested in different conditions, with different inputs. Nonetheless, the results of this thesis project are a big step towards realizing an in-house DAQ device for the team.

This project has been an intense and rewarding learning experience. Theories learned in classes taken during my undergraduate degree are being implemented, and along the way, I discovered the non-ideal behavior of many components. I hope that the team continues my work and helps the team reach new heights.

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APPENDIX A DESIGN CALCULATIONS

Design calculations for the DAQ device are included in this section, starting on the next page. The calculations include, in order:

- Power budget
- Digital input protection
- ADC resolution requirements
- Non-inverting gain stage gain tolerance calculations
- TPS65131 boost converter calculations
- Power rail tolerance calculations
- 5 V analog rail precision reference bias current resistor calculations

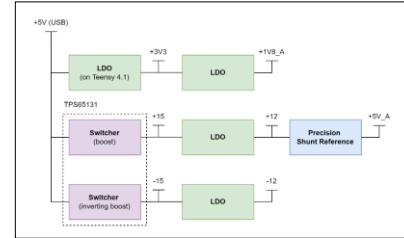
Power Budget

Component	Min (mA)	Nom (mA)	Max (mA)
Loads			
+5V power good LED (debug)	1.05	1.06	1.07
Teensy 4.1 consumption	90	100	110
+/- 15V (TPS65131) boost quiescent current	0.5	0.5	0.724
Derived Voltage Rails			
+15V boost --> +12V LDO	131.843	136.23375	206.7788
-15V boost inverting --> -12V LDO	36.345	37.5	37.545
+3V3 (LDO on Teensy)	4.16086	11.328	12.382
Totals	263.8988	286.62175	368.4998

Must stay below 500mA to respect USB 2.0 spec!

Summary	Min (mA)	Nom (mA)	Max (mA)
+5V	263.899	286.622	368.500
+3V3	4.161	11.328	12.382
+12V	35.158	36.329	55.141
-12V	9.692	10.000	10.012
+5V_A	1.100	1.860	2.370
+1V8_A	0.005	1.980	2.700

Component	Min (mA)	Nom (mA)	Max (mA)
Loads			
MCP33151-10 ADC x 3 (DVIO)	0.00036	1.2	1.5
MCP23008 IO Expansion x 4	0.008	4	4
Relay driver HIGH pull-down in driver	0.792	0.792	0.792
+3V3 power good LED (debug)	3.3	3.3	3.3
+1V8_A LDO quiescent draw	0.05	0.05	0.075
MCP9700T temperature sensor quiescent draw	0.006	0.006	0.015
Derived Voltage Rails			
+1V8_A (LDO from +3V3)	0.0045	1.98	2.7
Totals	4.16086	11.328	12.382



Component	Min (mA)	Nom (mA)	Max (mA)
Loads			
INA821 In-amp	0.6	0.6	0.87
TLV2172 Op-amp x 8	25.6	25.6	36.8
DG408 8:1 mux x 4	0.04	0.2	0.3
DG409 dual 4:1 mux x 5	5	5	10
+12V power good LED (debug)	2	2	3
+12V LDO quiescent draw (LDK320AM120R)	0.07	0.07	0.1
Derived Voltage Rails			
+5V_A (precision shunt reference) quiescent bias	0.748	0.999	1.701
+5V_A rail load	1.10012	1.86	2.37
Totals	35.15812	36.329	55.141

Op Amps	Min (mA)	Nom (mA)	Max (mA)
RC4580	6	6	9
TLV2172	3.2	3.2	4.6

Results in too much current!

Component	Min (mA)	Nom (mA)	Max (mA)
Loads			
DG408 8:1 mux x 4	0.004	0.3	0.3
DG409 dual 4:1 mux x 5	2.5	2.5	2.5
-12V power good LED (debug)	1.188	1.2	1.212
Other			
-12V LDO quiescent draw	6	6	6
Totals	9.692	10	10.012

Component	Min (mA)	Nom (mA)	Max (mA)
Loads			
MCP33151-10 ADC x 3 (VREF)	0.00012	0.66	0.87
+5V_A power good LED (debug)	1.10	1.20	1.50
Totals	1.10012	1.86	2.37

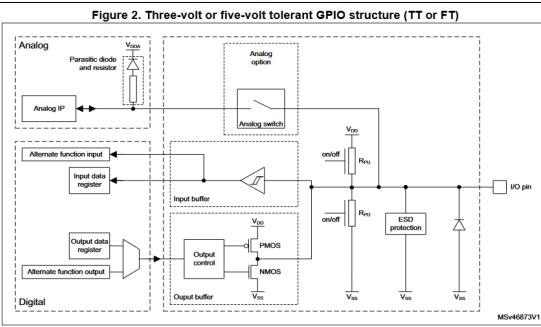
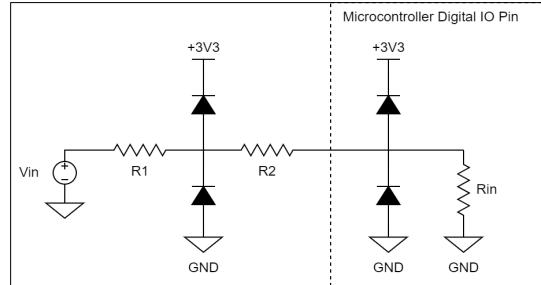
Component	Min (mA)	Nom (mA)	Max (mA)
Loads			
MCP33151-10 ADC x 3 (AVDD)	0.0045	1.98	2.7
Totals	0.0045	1.98	2.7

Digital Input Protection

Parameter	Value	Units	Comments
Maximum design input voltage	27 V		
Minimum design input voltage	-27 V		
Maximum design microcontroller pin source current	15 mA		
Maximum design microcontroller pin sink current	15 mA		
Microcontroller pin source/sink max current	25 mA		
Microcontroller pin max voltage	4 V		FT pins can take up to $3.3+4 = 7.4$
Microcontroller pin min voltage	-0.3 V		All pins
External protection diode max current	125 mA		BAT54S rated for 200mA abs max
External protection diode forward voltage	0.25 V		
Nominal rated input/output voltage high	3.3 V		
Nominal rated input/output voltage low	0 V		
Source: required $R_1 + R_2$	220 Ohm		Assuming pin outputs 3.3V, short to GND
Sink: required $R_1 + R_2$	220 Ohm		

Chosen R1	470 Ohm
Chosen R2	10 Ohm
Resultant max input voltage	62.3 V
Resultant min input voltage	-59 V
Resultant max source/sink current	6.875 mA
R1 max power dissipation	7.34375 W
Current at which P_{diss} of R1 is 0.5W	32.616 mA
Input voltage at which P_{diss} of R1 is 0.5W	18.880 V
Input voltage at which P_{diss} of R1 is 0.5W	-15.5797 V

Note: not accounting for variation of diode forward voltage as function of diode current



Note: The parasitic diode in the analog domain is connected to V_{DDA} and cannot be used as a protection diode.
The voltage level called V_{DD_FT} in some datasheets and reference manuals is inside the ESD protection block.
When the analog option is selected (by enabling analog peripheral on the given pin), the FT I/O is not five-volt tolerant anymore since the pin is supplied with V_{DDA} .

Caution: A TT or FT GPIO pin has no internal protection diode connected to supply (V_{DD}). There is no physical limitation against over-voltage. Therefore, for applications requiring a limited voltage threshold, it is recommended to connect an external diode to V_{DD} .

According to AN4899 from STMicro, cannot rely on internal protection diodes which may/may not exist.

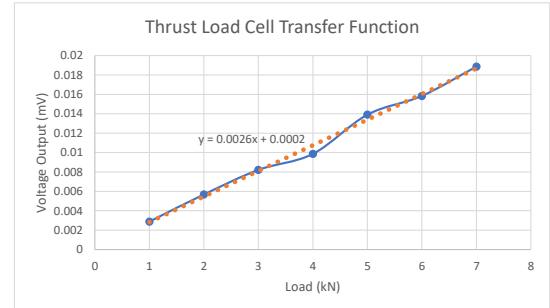
Will proceed with design as if they do not exist.

Teensy 4.0/4.1 pins are all 3.3v only without overvoltage protection.

MSV46873V1

ADC Resolution

Parameter	Value	Units	Comments	Thrust Load Cell Requirements
Minimum sensor output voltage	0 mV		Differential output	0 mV
Maximum sensor output voltage	100 mV		Differential output	23.1308 mV
Sensor resolution	0.05 mV/PSI		Voltage-output pressure transducer is 0.05mV/PSI	0.0026 mV/N
Signal conditioning gain	50 V/V		max gain to keep output voltage within ADC Vref	0.0255 mV/kgf
Minimum ADC sampling voltage	0 mV			kilogram-force
Maximum ADC sampling voltage	5000 mV			
ADC resolution required	2.5 mV/LSB		to resolve single PSI	
ADC reference voltage	5 V			
ADC effective number of bits	12.8 bits			
ADC resolution	0.7011 mV/LSB			
PSIs resolvable	0.2804 PSI			
N resolvable	2.6966 N			
Calculate ENOB				
ADC reference voltage	5 V			kN V
ADC SINAD	80.4 dB	MCP33151 14-bit		1 0.002881
ADC effective number of bits (ENOB)	13.063 bits			2 0.005678
ADC resolution	0.5842 mV/LSB			3 0.008215
Calculate ENOB				4 0.009862
ADC reference voltage	5 V			5 0.013907
ADC SINAD	86.9 dB	MCP33131 16-bit		6 0.01584
ADC effective number of bits (ENOB)	14.143 bits			7 0.018864
ADC resolution	0.2764 mV/LSB			slope 0.0026 mV/N
Options				max load 8896.443 N
- MCP33151-10-E/MS	14-bit SAR 1Msps SPI single-ended			
- MCP33131-10-E/MS	16-bit SRAR 1Msps SPI single-ended			



ADC Tolerance Calculations

Resolution

VREF / 2^{ENOB}

Analog mux: Vishay DG409

Vref

5

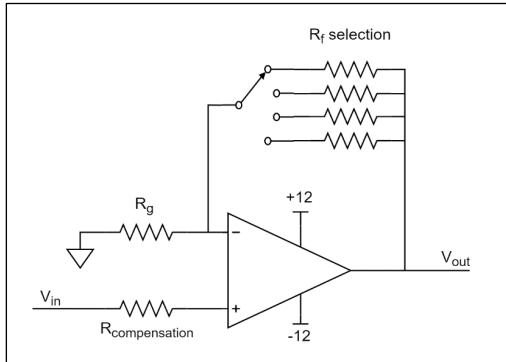
ENOB

12

V/LSB

0.001220703 V/LSB

		Tolerance	Min	Nom	Max	Units	Compensation Resistor
G = 1 V/V	Non-inverting amplifier Rf	0.10%	0	0	0	Ohm	000.000E+0 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	1.008	1.020	1.025	V/V	
G = 10 V/V	Non-inverting amplifier Rf	0.10%	45.255E+3	45.300E+3	45.345E+3	Ohm	4.495E+3 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	10.068	10.098	10.121	V/V	
G = 50 V/V	Non-inverting amplifier Rf	0.10%	242.757E+3	243.000E+3	243.243E+3	Ohm	4.890E+3 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	49.705	49.717	49.820	V/V	
G = 100 V/V	Non-inverting amplifier Rf	0.10%	498.501E+3	499.000E+3	499.499E+3	Ohm	4.941E+3 Ohm
	Non-inverting amplifier Rg	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm	
	Analog mux on-state resistance	-	40	100	125	Ohm	
	Gain = 1 + Rf/Rg	-	100.808	101.020	101.225	V/V	



TPS65131 Dual-Rail Boost Calculations

Parameter	Value	Units	Comments
Positive Boost Converter			
R2 max value	200 kOhm		
Vpos	15 V		Positive boost output voltage value
Vref	1.213 V		Positive boost output reference voltage
R2 chosen value	47.5 kOhm		
Ideal R1	539.886645 kOhm		
Chosen R1	536 kOhm		
Actual Vpos	14.9007474 V		

Inductor Selection (Vpos)		
Vin	5 V	
Vpos rail current requirement	0.08 A	power budget shows 70mA, I added safety margin
Peak inductor current _L_P	0.375 A	
Inductor current ripple	0.075 A	
Converter switching frequency	1.25 MHz	
L1 value	35.555556 uH	datasheet recommends between 3.3uH to 6.8uH

Output Capacitors		
Max allowed ripple (Delta Vpos)	0.005 V	
Minimum output capacitance (C4)	8.5333 uF	
ESR of C4	0.01 Ohm	
Ripple due to ESR	0.0008 V	

Feedforward Capacitor		
C9 value	12.69E-12 F	
Chosen C9 value	13 pF	

Parameter	Value	Units	Comments
Inverting Boost Converter			
R4 max value	200 kOhm		
Vneg	-15 V		
Vref	1.213 V		
R4 chosen value	47.5 kOhm		
Ideal R3	587.38664 kOhm		
Chosen R3	576 kOhm		
Actual Vpos	-14.709221 V		

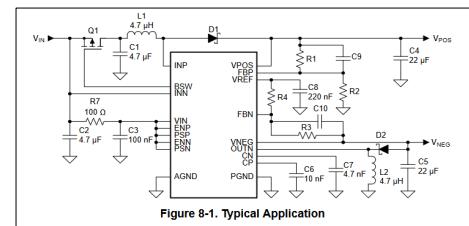


Figure 8-1. Typical Application

Inductor Selection (Vneg)		
Vin	5 V	
Vneg rail current requirement	0.01 A	power budget shows 5mA, I added safety margin
Peak inductor current _L_P	0.0625 A	
Inductor current ripple	0.0125 A	
Converter switching frequency	1.25 MHz	
L2 value	240 uH	datasheet recommends between 3.3uH to 6.8uH

Output Capacitors		
Max allowed ripple (Delta Vneg)	0.005 V	
Minimum output capacitance (C5)	1.2 uF	
ESR of C5	0.01 Ohm	
Ripple due to ESR	0.0001 V	

Feedforward Capacitor		
C10 value	13.02E-12 F	
Chosen C10 value	13 pF	

Power Rail Tolerance Calculations

Parameter	Tolerance (%)	Min	Nom	Max	Units	Comments
+15V boost						
R1	1%	530.64	536	541.36	kOhm	
R2	1%	48.213	48.7	49.187	kOhm	
Vref	-	1.2	1.213	1.225	V	
Output voltage	-	14.14586	14.56347	14.97992	V	
-15V inverting boost						
R3	1%	570.24	576	581.76	kOhm	
R4	1%	48.213	48.7	49.187	kOhm	
Vref	-	1.2	1.213	1.225	V	
Output voltage	-	-14.7814	-14.3468	-13.912	V	
+12V LDO						
Dropout	-	0.7	1	1.2	V	
Minimum input voltage required		12.7	13	13.2	V	satisfied
Output voltage accuracy		-3%	0%	3%		
Output voltage		11.64	12	12.36	V	
-12V LDO						
Dropout	-	1.7	1.7	1.7	V	
Minimum input voltage required		-13.7	-13.7	-13.7	V	satisfied
Output voltage		-11.4	-12	-12.6	V	provided in datasheet
+1V8_A LDO						
Dropout		0.35	0.35	0.695	V	
Minimum input voltage required		2.15	2.15	2.495	V	satisfied
Output voltage accuracy	-	-1.50%	0%	1.50%		
Output voltage		1.773	1.8	1.827	V	

5V_A Precision Reference Biasing

Parameter	Tolerance	Min	Nom	Max	Units	Comments
ADC VREF current (load)	-	0.00012	0.66	0.87	mA	
Shunt reference bias current	-	1	1	1	mA	Min. 60uA. Cannot exceed 15mA.
Total current through Rbias	-	1.00012	1.66	1.87	mA	
Supply voltage (input to shunt)	-	11.9	12	12.1	V	100mV of ripple is a lot
Shunt reference output voltage	-	4.995	5	5.005	V	
Vin - Vshunt_out		6.895	7	7.105	V	
Rbias		3.69	4.22	7.10	kOhm	
Rbias calculated from Eqn 3	-		4.22		kOhm	verifies my nominal calculation above
Chosen resistor value		1%	4.18	4.22	4.26	kOhm
Resultant bias current		0.748	0.999	1.701	mA	Meets requirements!

APPLICATIONS INFORMATION

The ADR5040/ADR5041/ADR5043/ADR5044/ADR5045 are a series of precision shunt voltage references. They are designed to operate without an external capacitor between the positive and negative terminals. If a bypass capacitor is used to filter the supply, the references remain stable.

For a stable voltage, all shunt voltage references require an external bias resistor (R_{BIAS}) between the supply voltage and the reference (see Figure 19). The R_{BIAS} sets the current that flows through the load (I_L) and the reference (I_{IN}). Because the load and the supply voltage can vary, the R_{BIAS} needs to be chosen based on the following considerations:

- R_{BIAS} must be small enough to supply the minimum I_{IN} current to the ADR5040/ADR5041/ADR5043/ADR5044/ADR5045, even when the supply voltage is at its minimum value and the load current is at its maximum value.
- R_{BIAS} must be large enough so that I_{IN} does not exceed 15 mA when the supply voltage is at its maximum value and the load current is at its minimum value.

Given these conditions, R_{BIAS} is determined by the supply voltage (V_S), the ADR5040/ADR5041/ADR5043/ADR5044/ADR5045 load and operating current (I_L and I_{IN}), and the ADR5040/ADR5041/ADR5043/ADR5044/ADR5045 output voltage (V_{OUT}).

$$R_{BIAS} = \frac{V_S - V_{OUT}}{I_L + I_{IN}} \quad (3)$$

APPENDIX B MCP33151 EVALUATION BOARD

A. Introduction

This appendix contains the schematics and other documentation for the MCP33151 Eval Board prototype. Specifically,

- Schematics
- Draftsman document (layers, assembly)
- Bill of Materials
- User manual
- Testing results
- Testing data

MCP33151-10 Eval Board

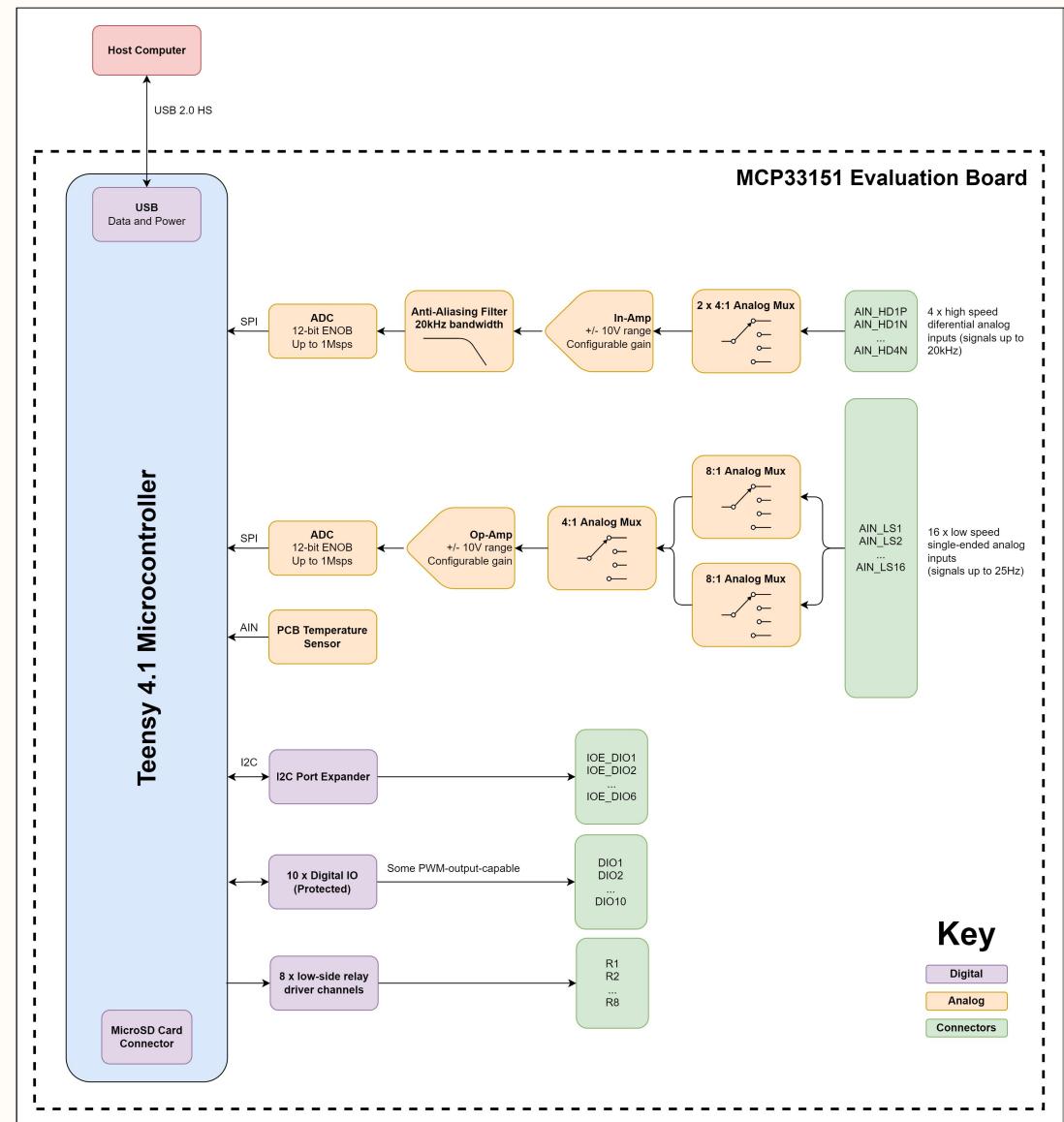
Table of Contents

- 1 Cover
- 2 Connectors
- 3 Power
- 4 Microcontroller
- 5 IO Expansion
- 6 Digital IO Protection
- 7 Analog - High Speed Differential
- 8 Analog - Low Speed Single-Ended
- 9 ADC
- 10 Relay Drivers
- 11 Debug

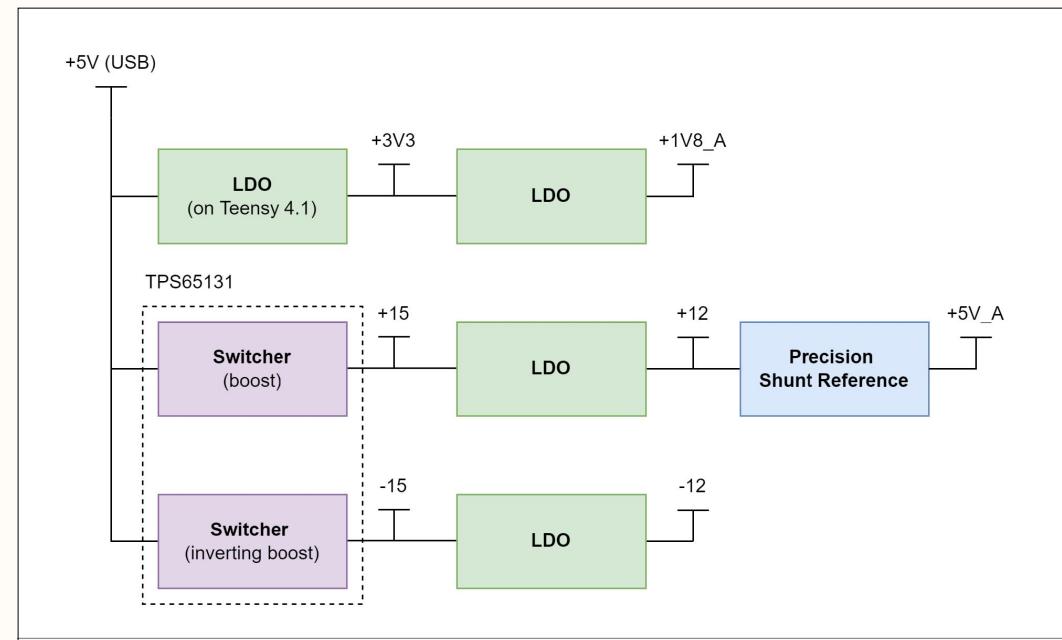
Port Colors



Main Block Diagram



Power Architecture



Revision: fe513d38ca26ea1f94add3fb0afb592a349a031f [Ahead of server]

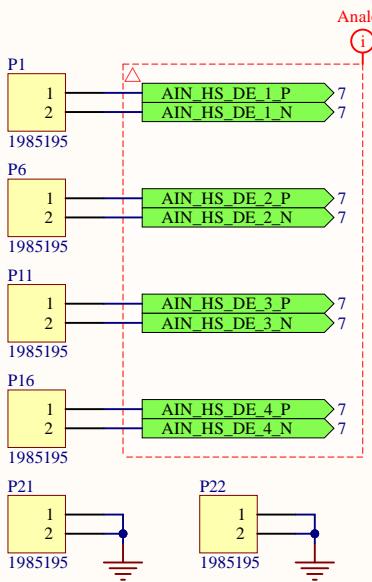
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Date: 2022-11-23	Time: 12:23:33 PM	Sheet 1 of 11		
File: C:\Users\jaspe\Desktop\ecse478_honours_thesis\1 Hardware\MCP33151 Eval Board\Cover.SchDoc				

Connectors

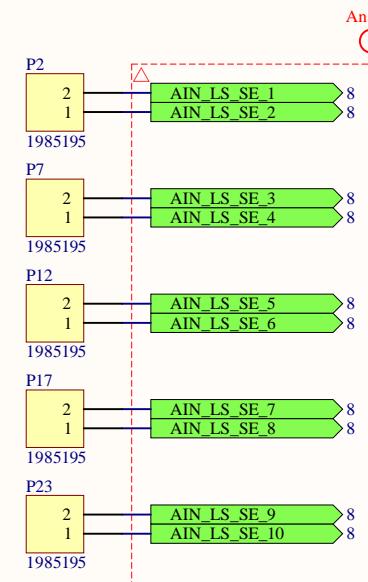
DE = differential-ended
SE = single-ended

All terminal blocks for ease of prototyping.

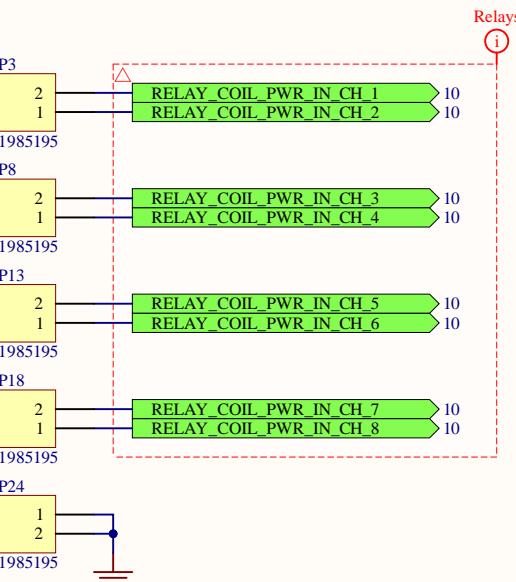
High Speed DE Analog



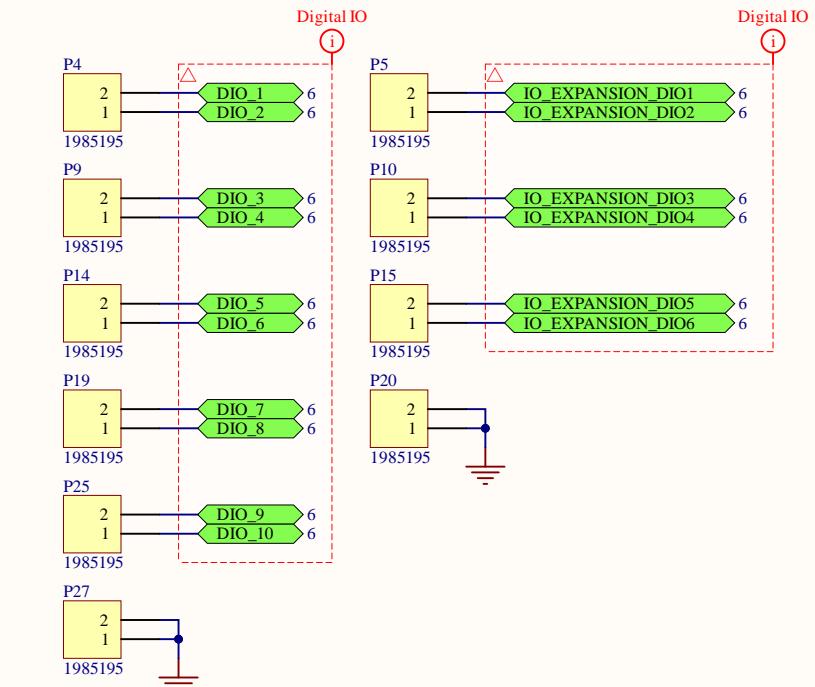
Low Speed SE Analog



Relay Coils (Low Side)



Digital IO Pins

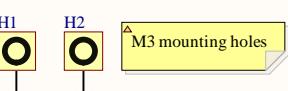


Power



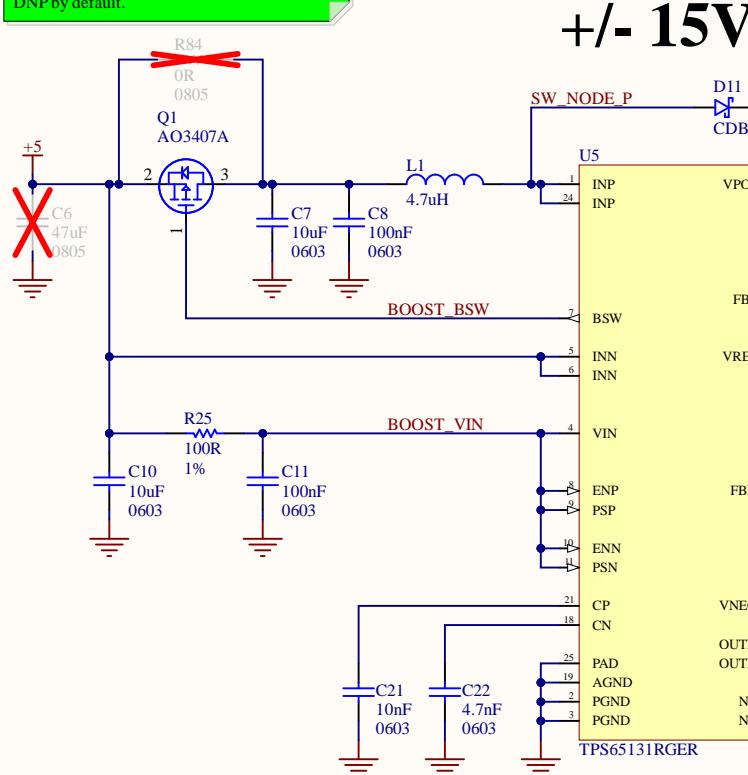
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File: C:\Users\jaspe\Desktop\ecse478_honours_thesis\1 Hardware\MCP33151 Eval Board\Connectors.SchDoc						



Power

R84 is a jumper to bypass Q1. DNP by default.
C6 is in place in case we need more capacitance.
DNP by default.



+/- 15V

Vref = 1.213V
R22 = R23 * (Vpos / Vref - 1)
R26 = -R24 * (Vneg / Vref)

C4 in place if we need more capacitance.
DNP by default.

R82 + C78 form low-pass filter, cutoff around 225Hz. R82 may be depopulated to use external +15V supply.

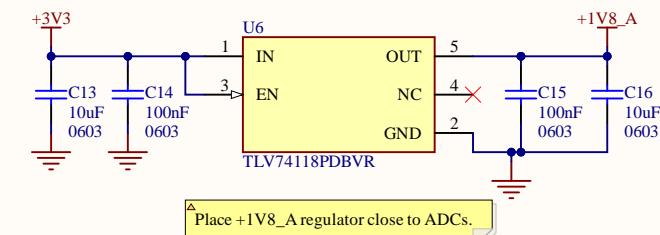
+5V (from USB port on Teensy :))

Nothing to be done.

+3V3 (from Teensy :))

Nothing to be done.

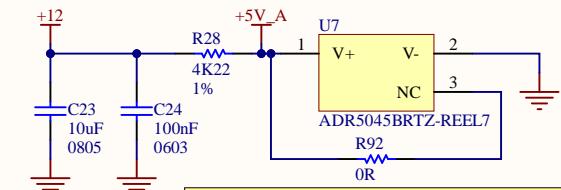
+1V8_A (ADC)



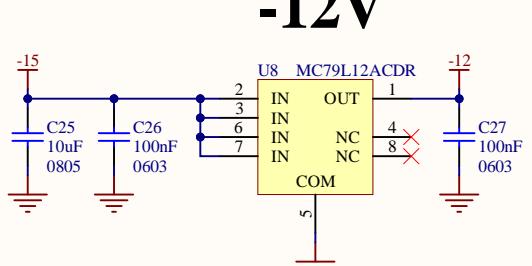
Place +1V8_A regulator close to ADCs.

+5V_A (Analog Reference)

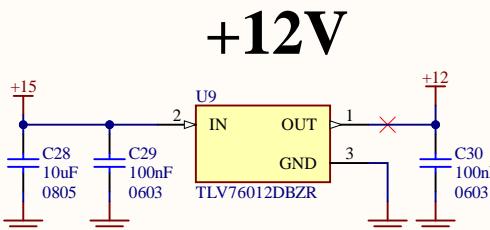
Voltage reference IC. Keep away from noisy sources and place close to ADCs.



4K22 resistor biases the shunt to approximately 1mA.
R92 is a jumper to connect pin 3 to pin 1. Option to remove if using other pin-compatible shunt references.



-12V



+12V

Revision:

Title
Power

Size: B Revision: Drawn By: Jasper Yun

Date: 2022-11-23 Time: 12:23:34 PM Sheet 3 of 11

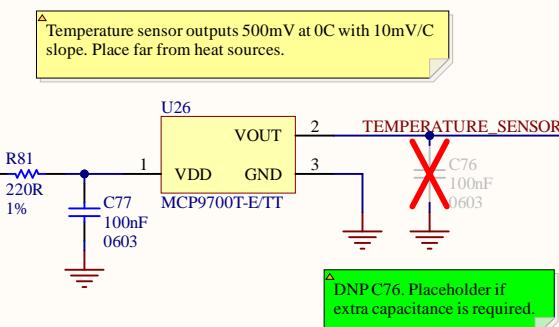
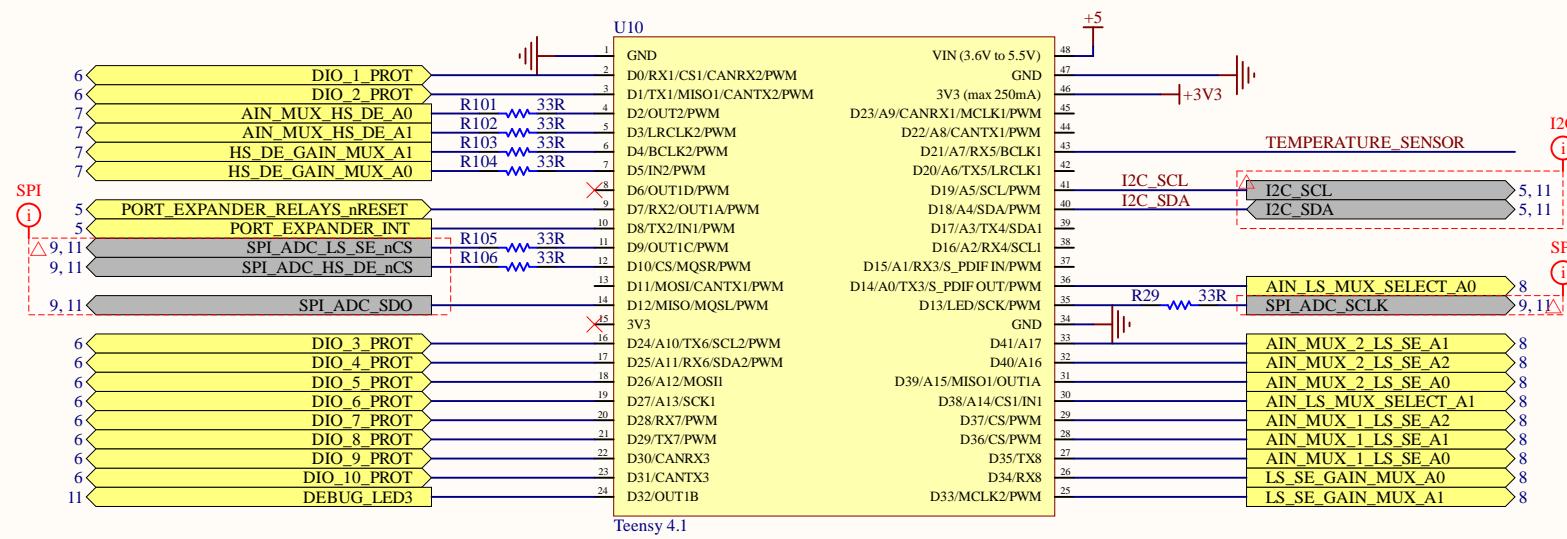
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Avionics
McGill Rocket Team
McGill University
Montreal, Quebec



Microcontroller

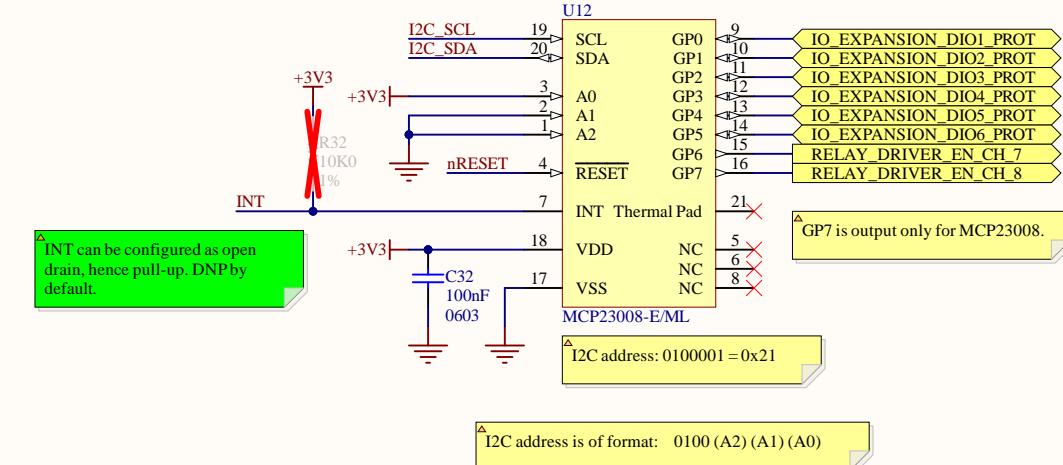
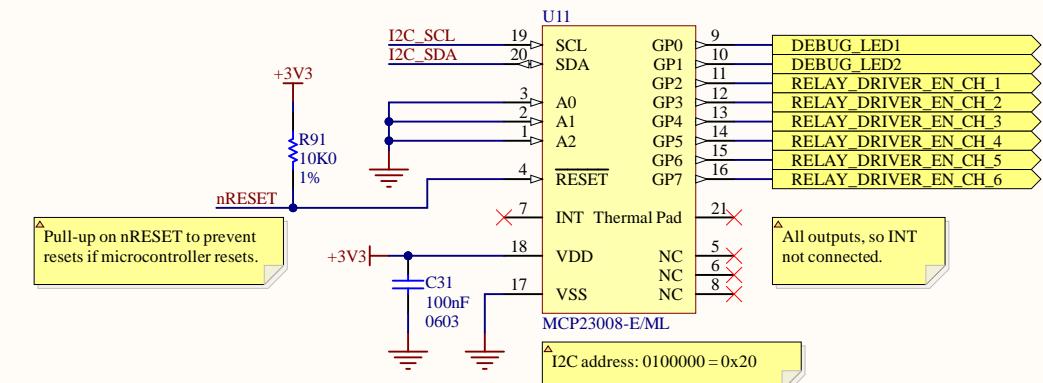
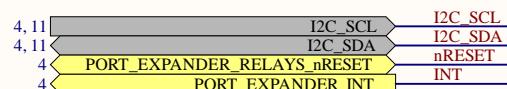
▲ Teensy will be interfaced by USB thus powered by USB. Board is thus limited to 500mA from the +5V rail.
 ▲ Use Teensy 4.1 Ethernet kit to add Ethernet capability to the board.
 ▲ Teensy 4.1 has built-in SD card which interfaces using 4-bit SDIO. No need for SD card on this board.



Revision:

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Size:	B	Revision:	Drawn By:	Jasper Yun
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IO Expansion



Revision:

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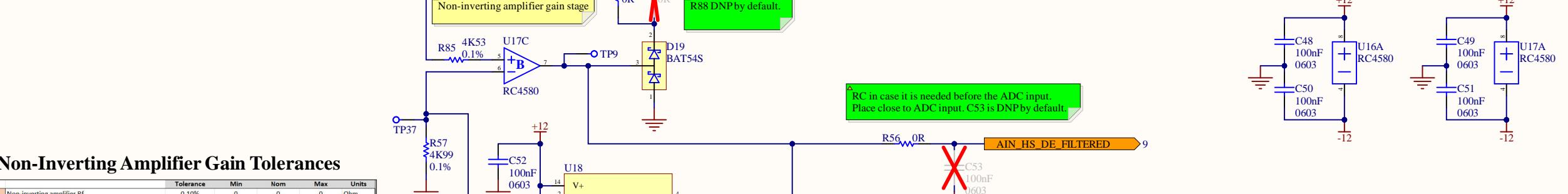
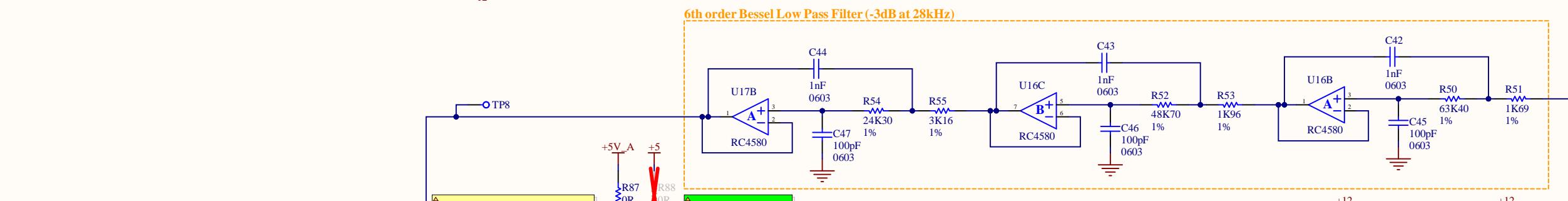
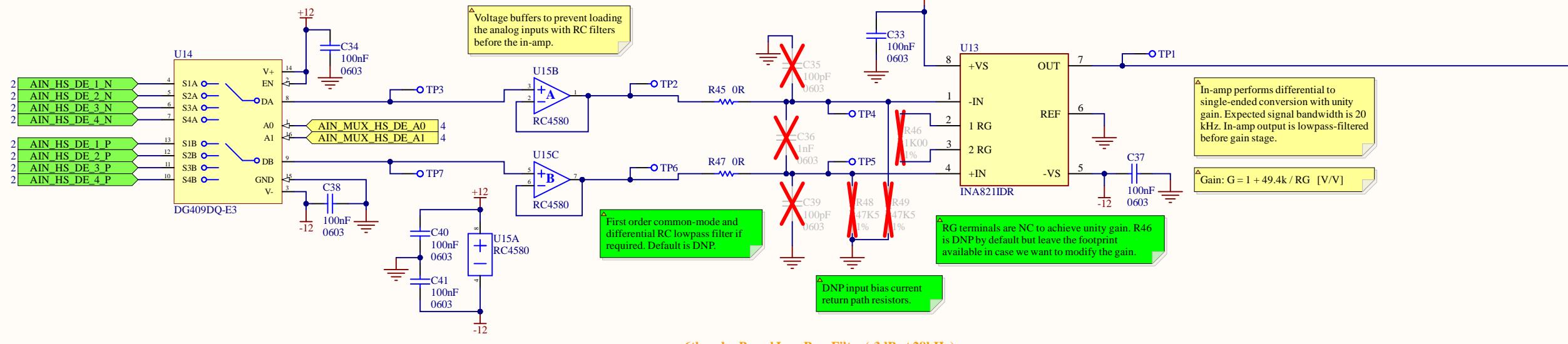
Digital IO Protection



Revision:

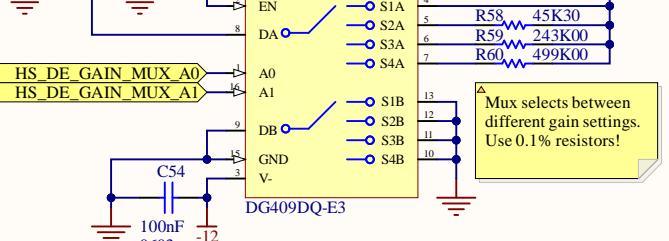
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File: C:\Users\jaspe\Desktop\ecse478_honours_thesis\1 Hardware\MCP33151 Eval Board\Digital IO Protection.SchDoc			MRT

Analog - High Speed Differential



Non-Inverting Amplifier Gain Tolerances

	Tolerance	Min	Nom	Max	Units
$G = 1 \text{ V/V}$	0.10%	0	0	0	Ohm
Non-inverting amplifier Rf	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm
Non-inverting amplifier Rg	-	40	100	125	Ohm
Analog mux on-state resistance	-	1.008	1.020	1.025	V/V
$G = 10 \text{ V/V}$	0.10%	45.255E+3	45.300E+3	45.345E+3	Ohm
Non-inverting amplifier Rf	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm
Non-inverting amplifier Rg	-	40	100	125	Ohm
Analog mux on-state resistance	-	10.068	10.098	10.121	V/V
$G = 50 \text{ V/V}$	0.10%	242.757E+3	243.000E+3	243.243E+3	Ohm
Non-inverting amplifier Rf	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm
Non-inverting amplifier Rg	-	40	100	125	Ohm
Analog mux on-state resistance	-	49.705	49.717	49.820	V/V
$G = 100 \text{ V/V}$	0.10%	498.501E+3	499.000E+3	499.499E+3	Ohm
Non-inverting amplifier Rf	0.10%	4.985E+3	4.990E+3	4.995E+3	Ohm
Non-inverting amplifier Rg	-	40	100	125	Ohm
Analog mux on-state resistance	-	100.808	101.020	101.225	V/V

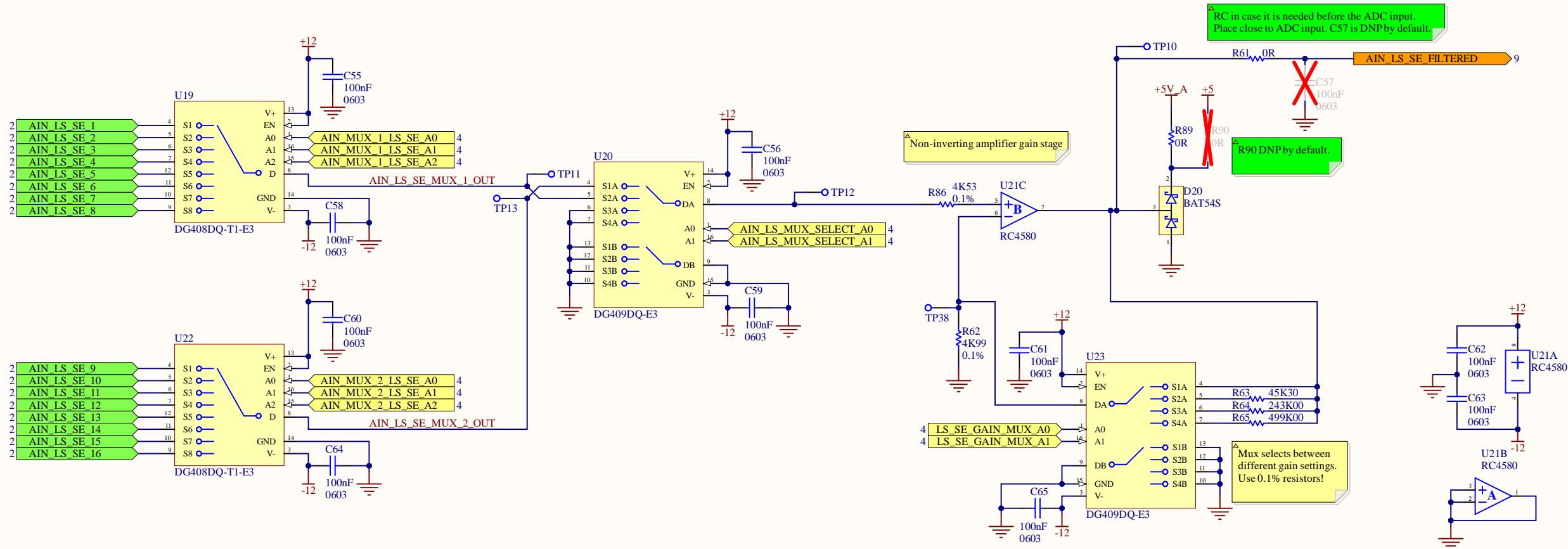


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Sheet 7 of 11	
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Analog - Low Speed Single-Ended



Non-Inverting Amplifier Gain Tolerances

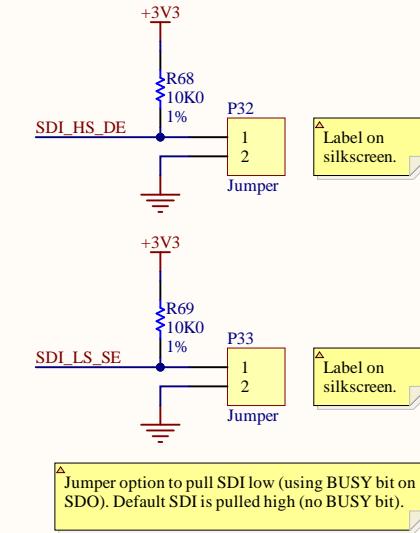
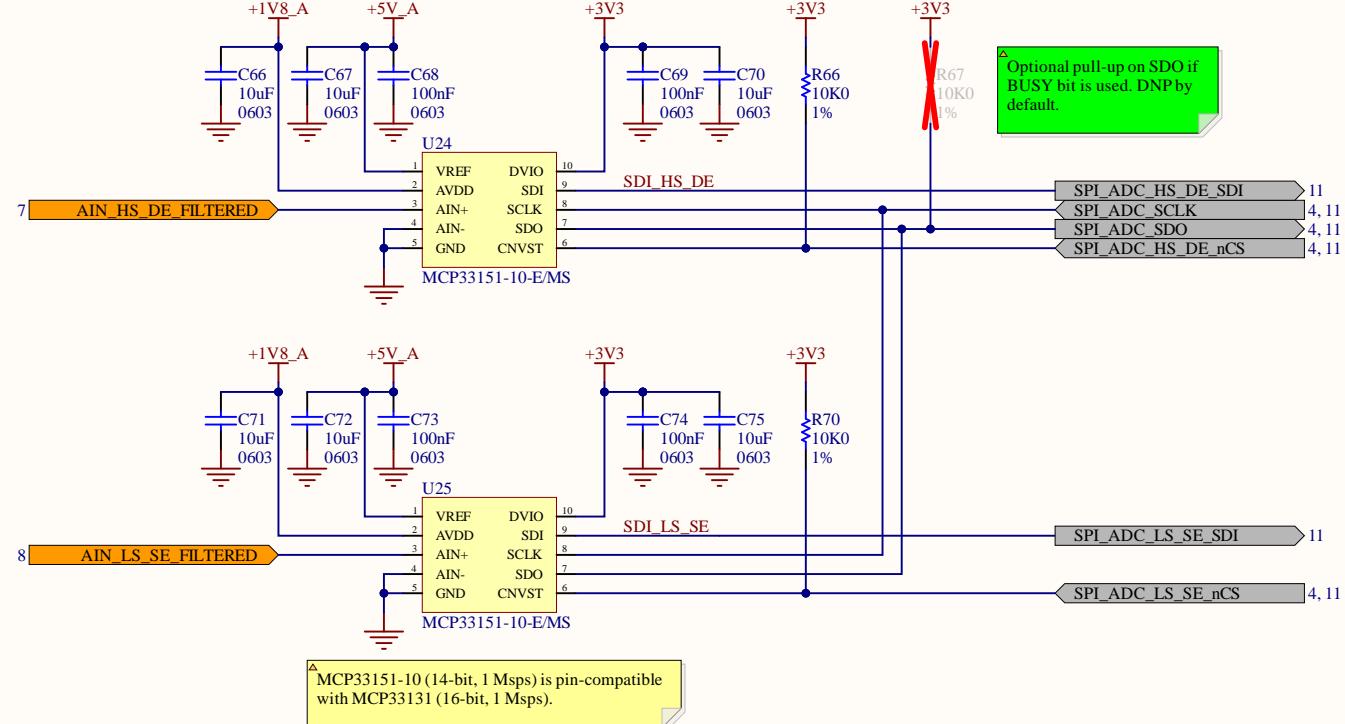
	Tolerance	Min	Nom	Max	Units
$G = 1 \text{ V/V}$	Non-inverting amplifier R_f	0.10%	0	0	0mΩ
	Non-inverting amplifier R_g	0.10%	4.985E+3	4.990E+3	4.995E+3 Ohm
	Analog mux on-state resistance	-	40	100	125 Ohm
	$\text{Gain} = 1 + R_f/R_g$	-	1.008	1.020	1.025 V/V
$G = 10 \text{ V/V}$	Non-inverting amplifier R_f	0.10%	45.255E+3	45.300E+3	45.345E+3 Ohm
	Non-inverting amplifier R_g	0.10%	4.985E+3	4.990E+3	4.995E+3 Ohm
	Analog mux on-state resistance	-	40	100	125 Ohm
	$\text{Gain} = 1 + R_f/R_g$	-	10.068	10.098	10.121 V/V
$G = 50 \text{ V/V}$	Non-inverting amplifier R_f	0.10%	242.757E+3	243.000E+3	243.434E+3 Ohm
	Non-inverting amplifier R_g	0.10%	4.985E+3	4.990E+3	4.995E+3 Ohm
	Analog mux on-state resistance	-	40	100	125 Ohm
	$\text{Gain} = 1 + R_f/R_g$	-	49.705	49.717	49.820 V/V
$G = 100 \text{ V/V}$	Non-inverting amplifier R_f	0.10%	498.501E+3	499.000E+3	499.499E+3 Ohm
	Non-inverting amplifier R_g	0.10%	4.985E+3	4.990E+3	4.995E+3 Ohm
	Analog mux on-state resistance	-	40	100	125 Ohm
	$\text{Gain} = 1 + R_f/R_g$	-	100.808	101.020	101.225 V/V

Revision:

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Size: B	Revision:	Drawn By: Jasper Yun		
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Analog to Digital Conversion

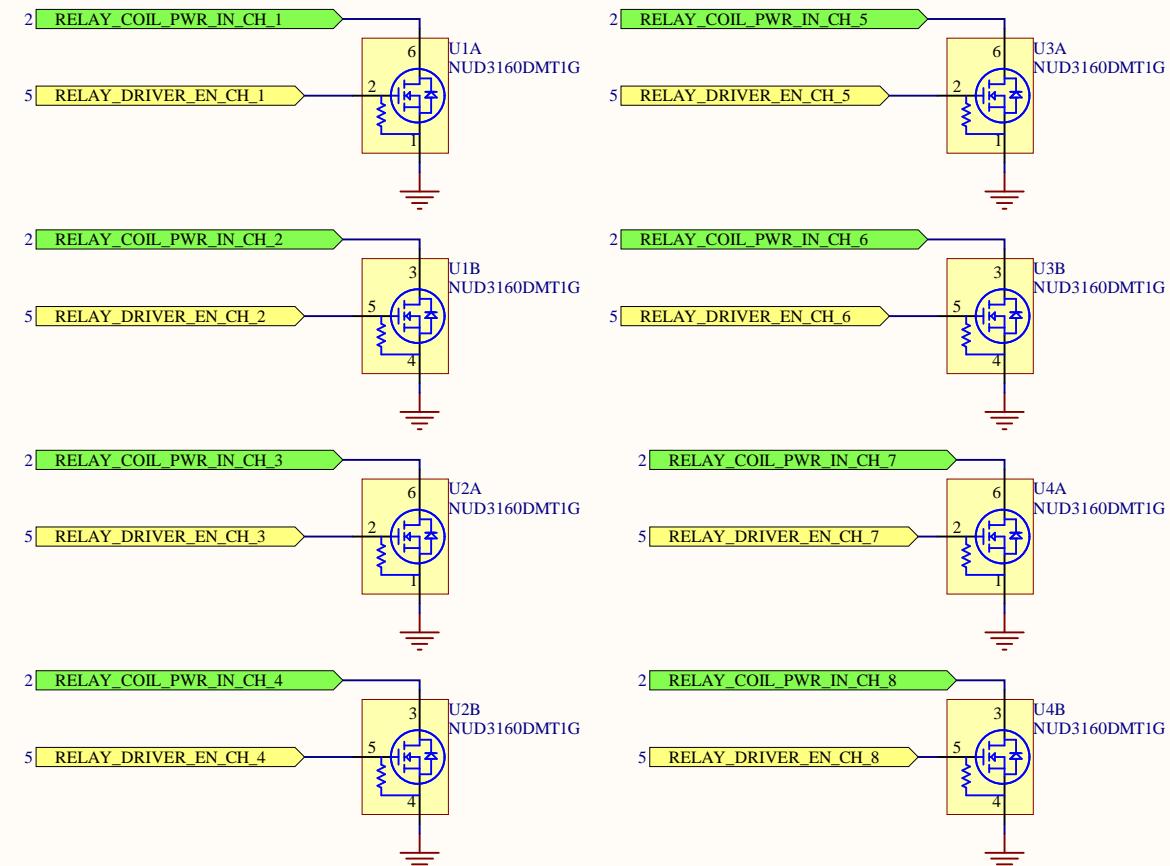


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File: C:\Users\jaspe\Desktop\ecse478_honours_thesis\1 Hardware\MCP33151 Eval Board\ADC.SchDoc			MRT

Relay Drivers

Relay drivers are low-side nFETs which are rated to 60V drain-source. Relay coil outputs are connected to RELAY_COIL_PWR_IN_CH_XY.

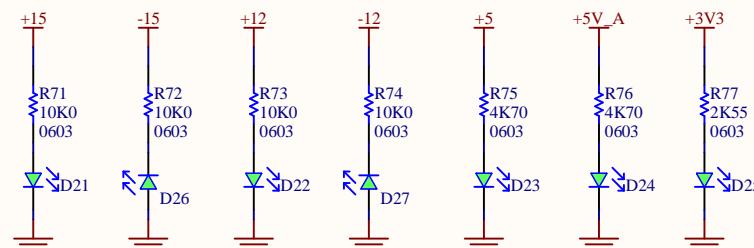


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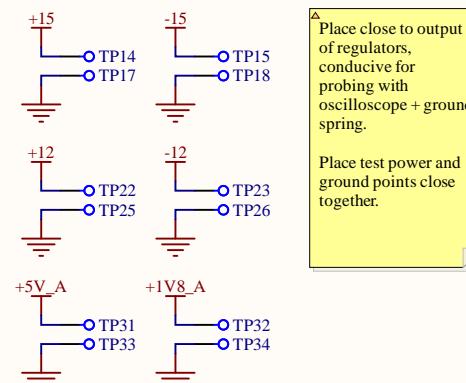
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Debug

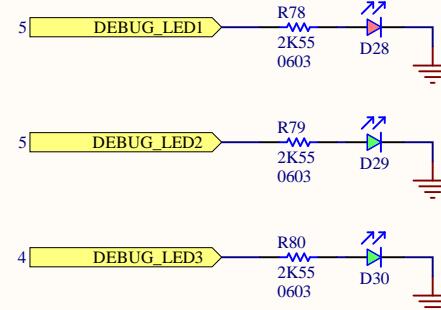
Power LEDs



Power Rails Test Points

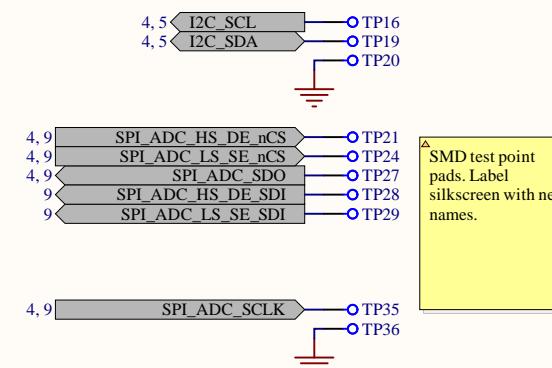


Program Debug LEDs



Analog Test Points

See analog sheets.



Revision:

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A

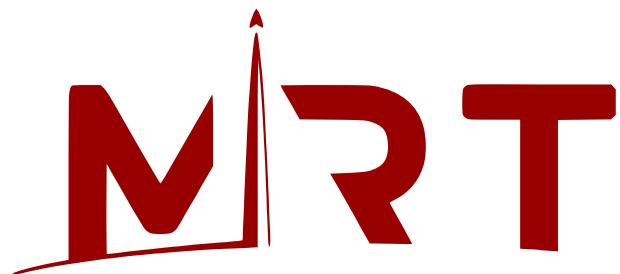
B

C

D

E

MCP33151 Eval Board



Thickness: 1.6 mm

Width: 8.46 cm

Length: 12.95 cm

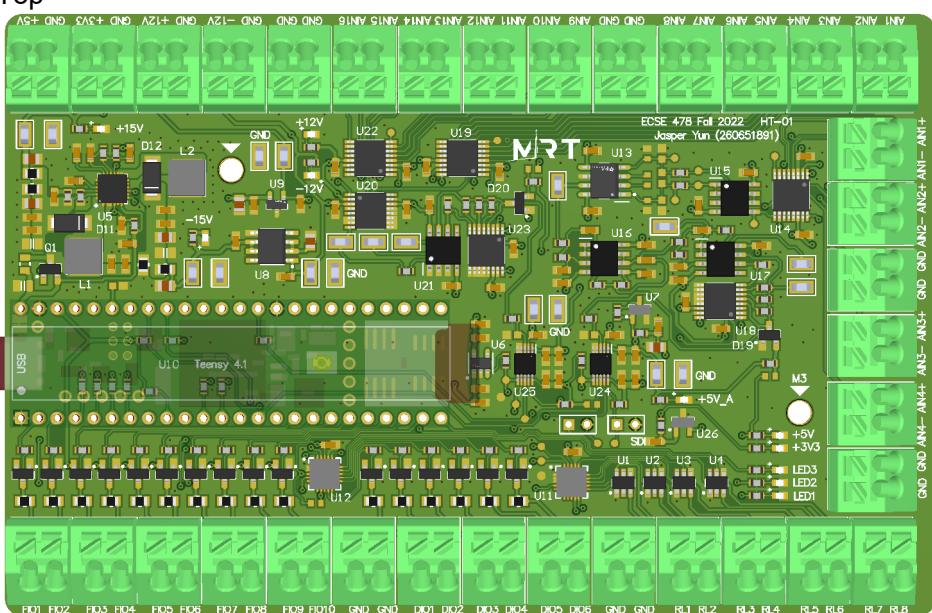
Layers: 4

ECSE 478 (Fall 2022) - HT-01
Jasper Yun (260651891)

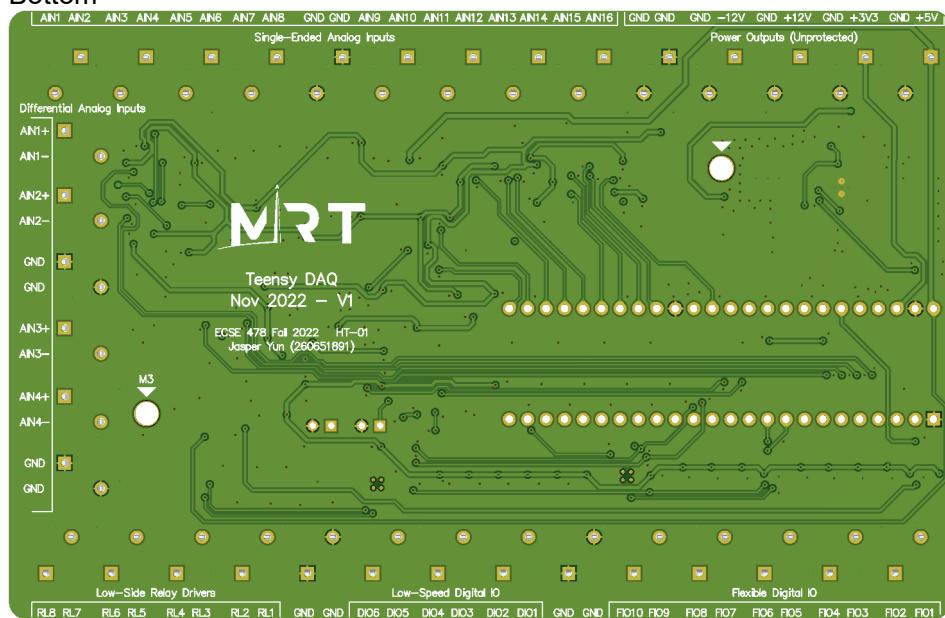
Advisor: Prof. Gordon Roberts

McGill University

Top



Bottom



A

B

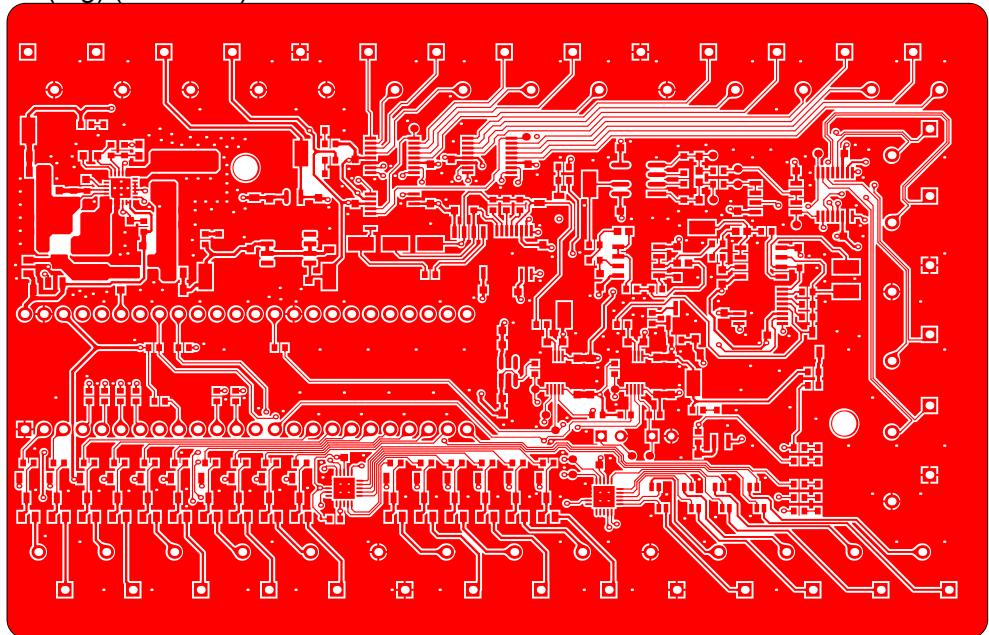
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D

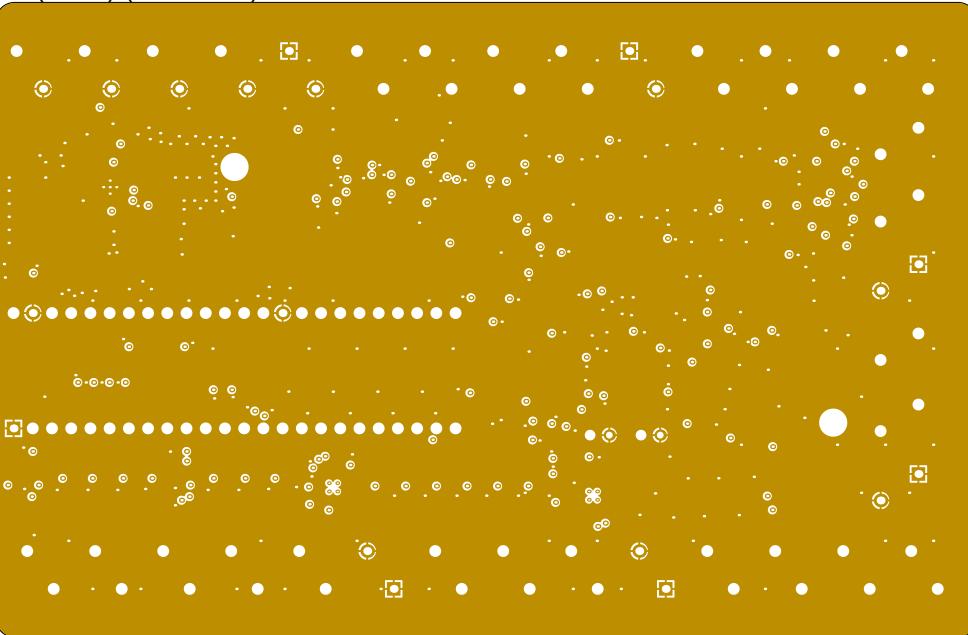
E

Layers

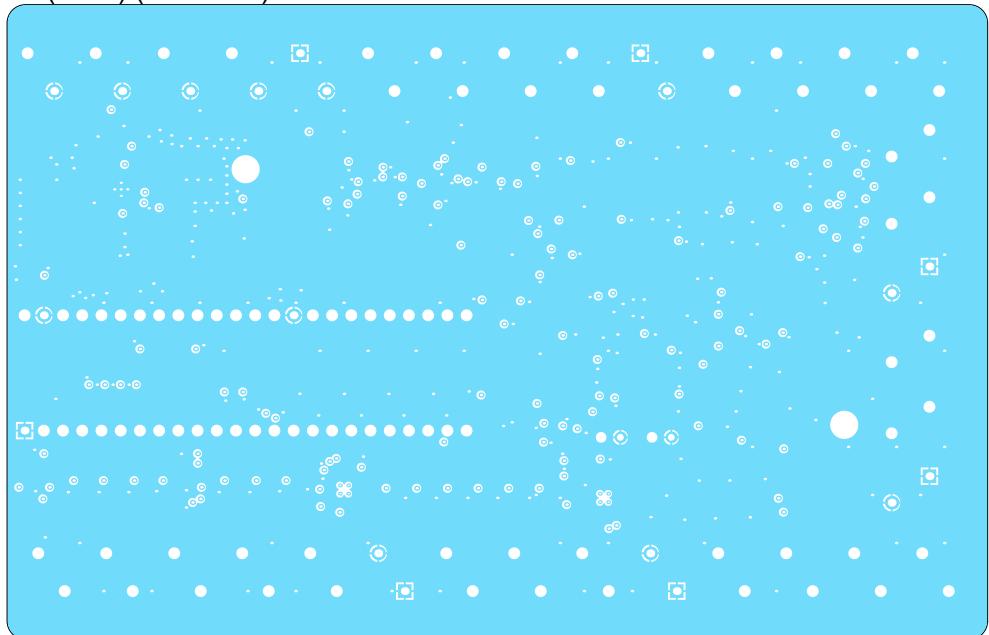
L1 (Sig) (Scale 1:1)



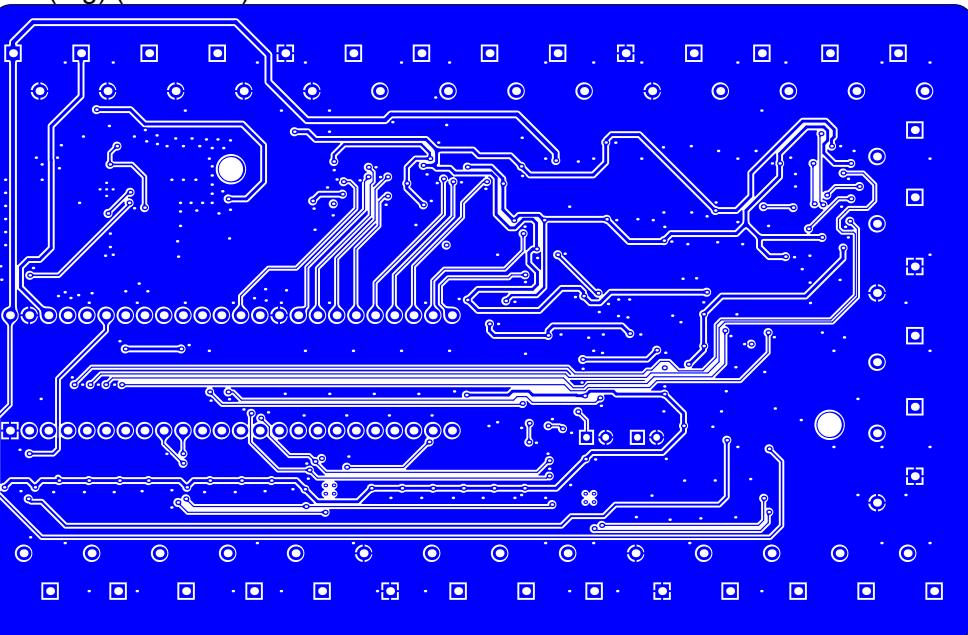
L2 (GND) (Scale 1:1)



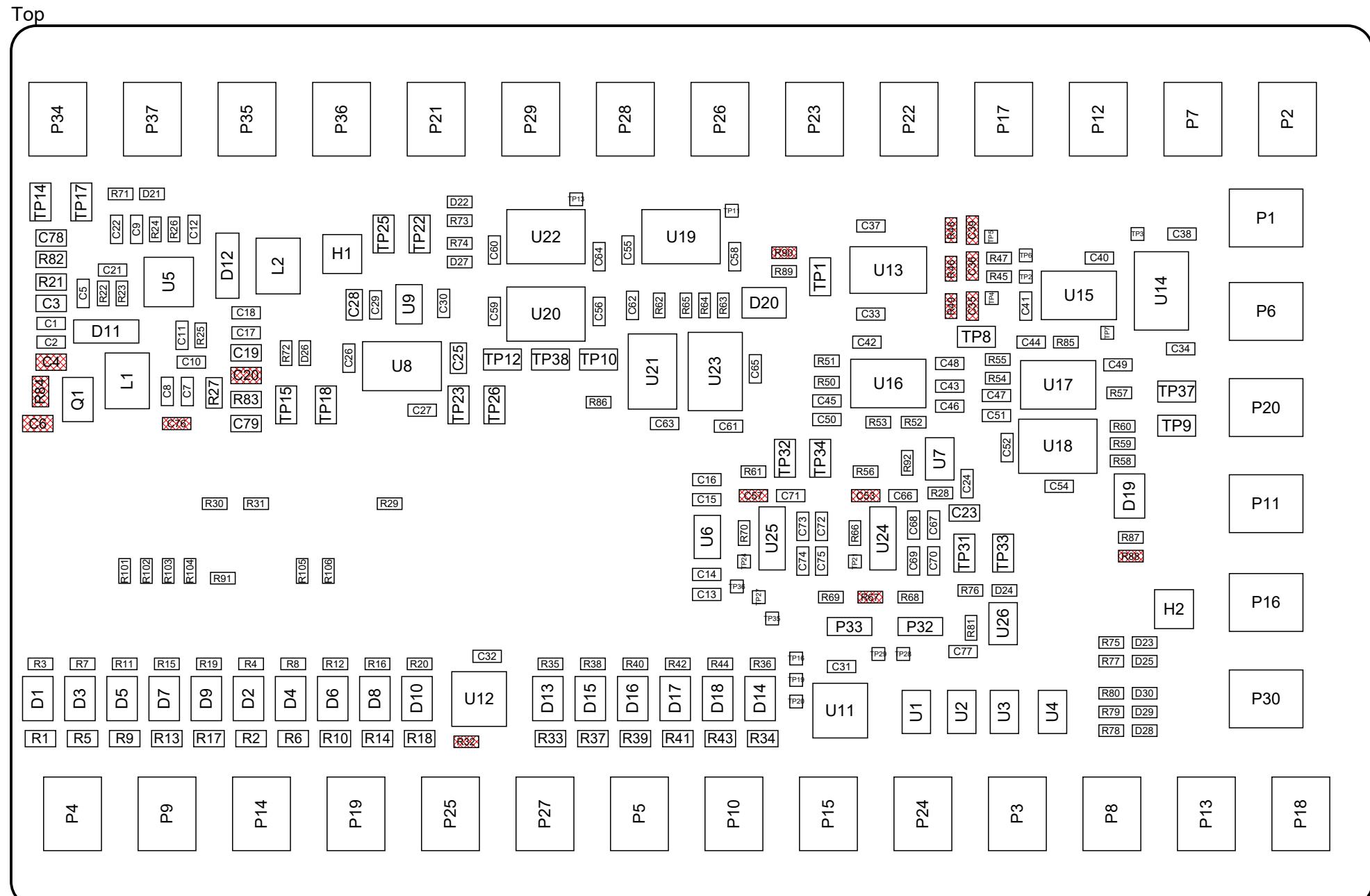
L3 (GND) (Scale 1:1)



=L4 (Sig) (Scale 1:1)



Assembly View



A

B

C

D

E

A

B

C

D

E

MCP33151 Eval Board Documentation

Jasper Yun (260651891)

Project Advisor: Prof. Gordon Roberts

HT-01
ECSE 478 (Fall 2022)

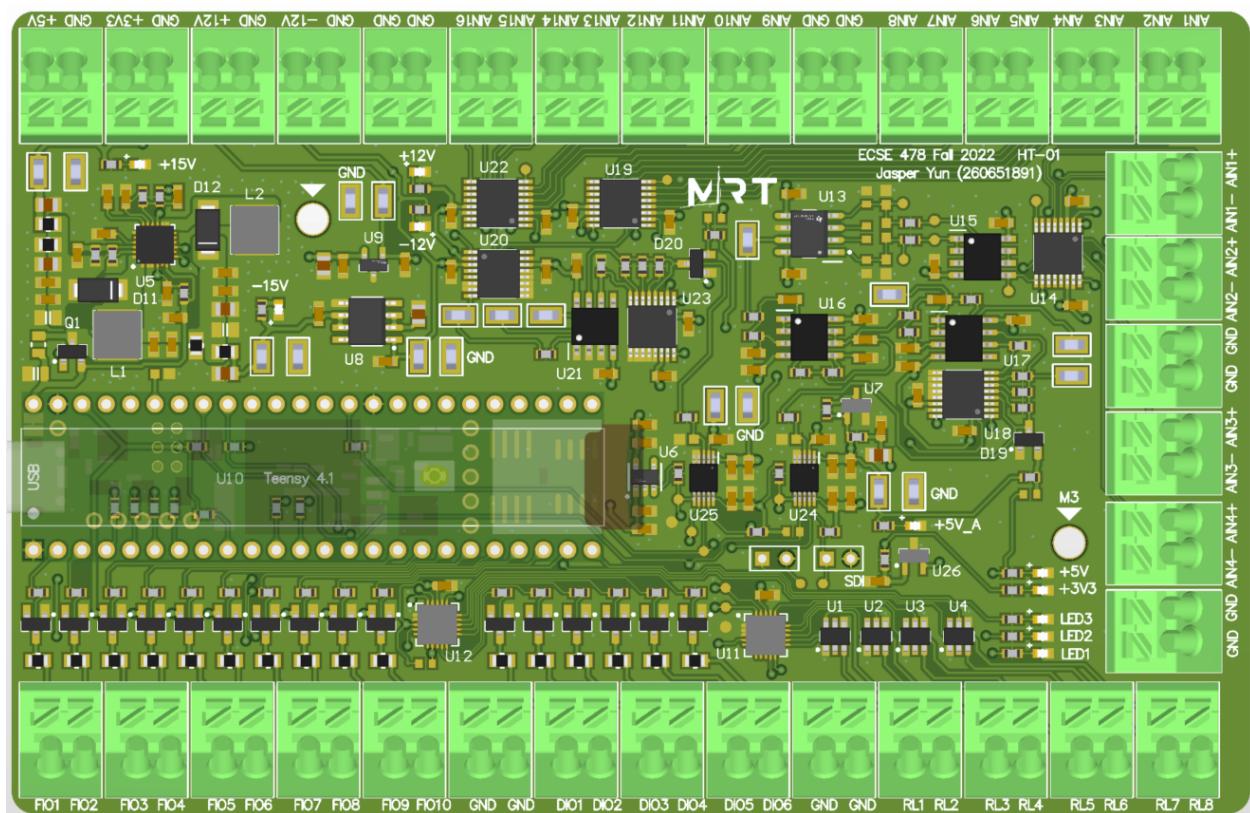


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Introduction

This document is intended as a sort of user's guide / datasheet / reference manual for the MCP33151 Eval Board prototype. All project files can be found in the GitHub repository linked [here](#). Fig. 1 shows a top view of the layout.

The board is a 1.6 mm thick 4-layer PCB using the JLCPCB 7628 stackup. The layers are organized as follows:

- Top: signal + GND pour
- Inner Layer 1: GND pour
- Inner Layer 2: GND pour
- Bottom: signal + GND pour

A 4-layer board was chosen to provide close reference GND planes to the top and bottom layers because the SPI communication between the microcontroller and ADCs may have clock speeds up to 100 MHz.

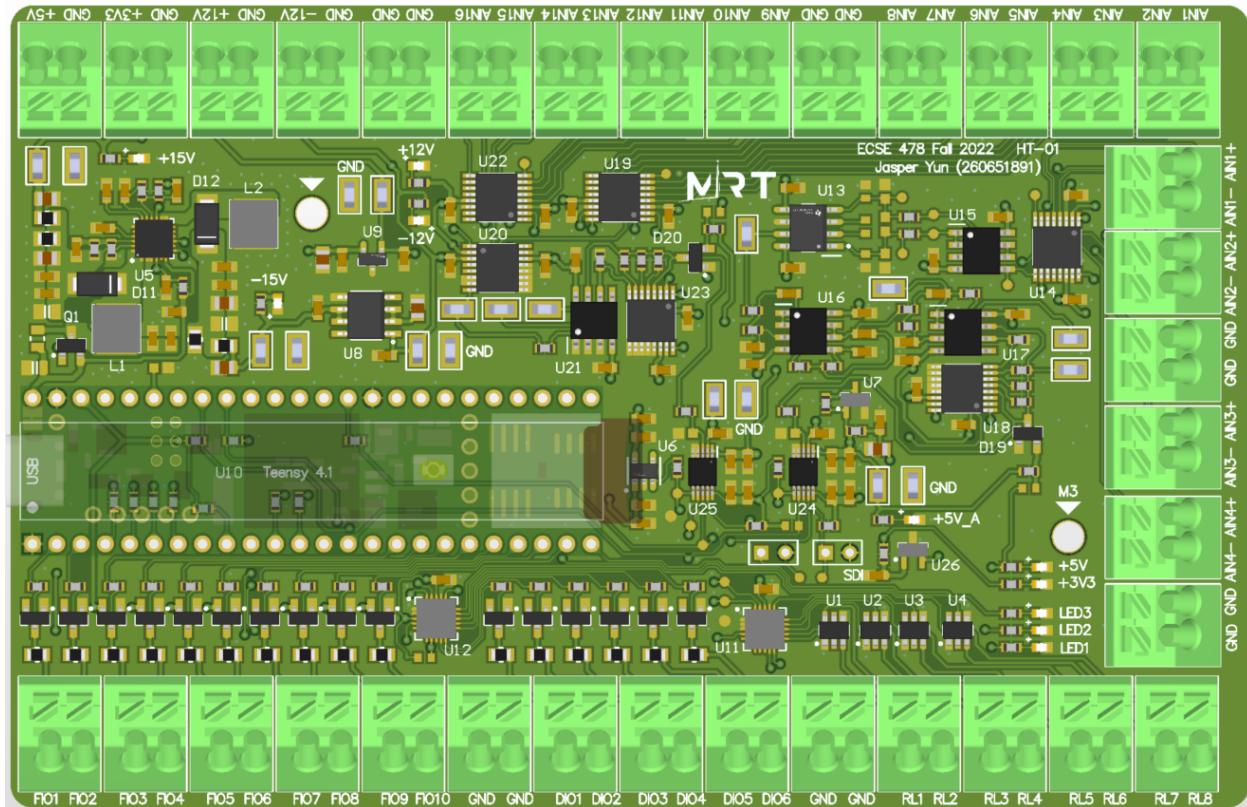


Fig. 1. Top view of MCP33151 Eval Board.

Block Diagram

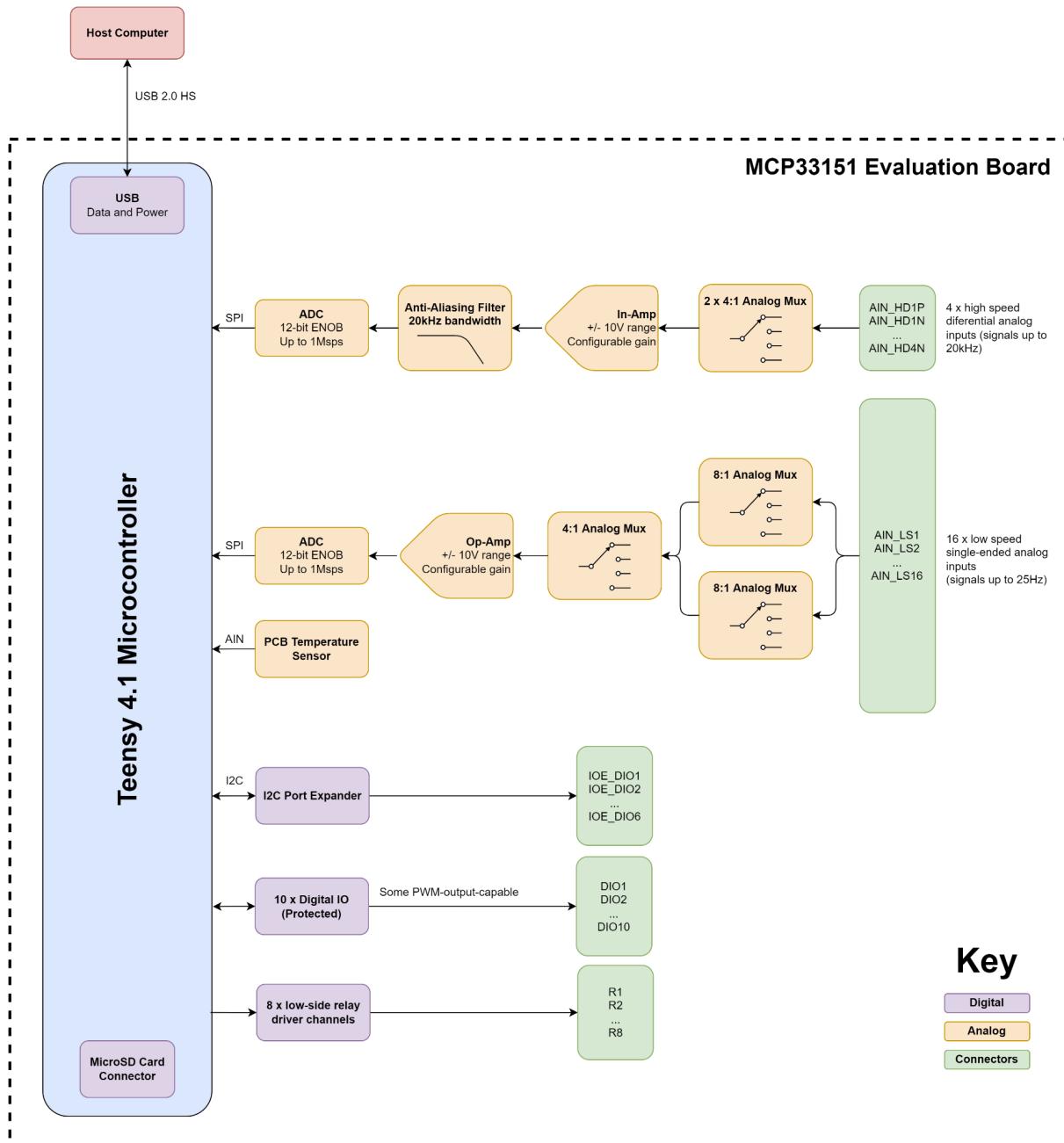


Fig. 2. MCP33151 Eval Board block diagram.

Hardware Overview

Analog Inputs

- 2 x MCP33151-10 ADCs which are 14-bit 1 Msps SAR converters
 - Sampling rate depends on mux settings
- 4 x differential analog inputs (filtered, muxed)
 - Using anti-aliasing 6th order Bessel filter with -3dB frequency at 28kHz

- 16 x single-ended analog inputs (unfiltered, muxed)
- Input voltage range: +/- 10V
- Hardware gain settings: 1 V/V, 10 V/V, 50 V/V, 100 V/V
- Temperature sensor

Digital IO

- All digital IO are protected against overvoltage and undervoltage up to +/- 15V
- 10 x flexible IO (FIO), connected straight to the microcontroller. Please note that not all of the listed peripherals are available simultaneously (i.e. they may be muxed). Refer to Table 1 or the schematics for further information
 - Digital input / output (inputs are interrupt-capable)
 - Analog input (10 bits ENOB, 3.3V max)
 - CAN (requires external transceiver)
 - SPI
 - I2C
 - UART
 - Digital IO, interrupt-capable
 - PWM
- 6 x digital IO (DIO) (through I2C IO expander)
 - Simple bidirectional IO, with possibility for interrupt on change
 - Will be slower than the FIO due to I2C interface
- 8 x relay drivers (RL)
 - Low-side N-channel MOSFET-based relay drivers
 - Drain-source capable up to 60V Vds,max

Table 1. Flexible IO pin capabilities.

FIO Pin	Capabilities
FIO1	D0 / UART1 RX / SPI1 CS / CAN2 RX / PWM
FIO2	D1 / UART1 TX / SPI1 MISO / CAN2 TX / PWM
FIO3	D24 / A10 / UART6 TX / I2C2 SCL / PWM
FIO4	D25 / A11 / UART6 RX / I2C2 SDA / PWM
FIO5	D26 / A12 / SPI1 MOSI
FIO6	D27 / A13 / SPI1 SCK
FIO7	D28 / UART7 RX / PWM
FIO8	D29 / UART7 TX / PWM
FIO9	D30 / CAN3 RX
FIO10	D31 / CAN3 TX

Microcontroller

- [Teensy 4.1](#) from PJRC
- Ethernet communication can be easily added by using the [Ethernet kit](#)

Power Supplies

- Refer to the power architecture diagram in Fig. 2.
- +/-12V, 5V, 3.3V are available on terminal blocks for connections to external circuits
 - These rails are unprotected (no fuses / reverse polarity) and have limited output current

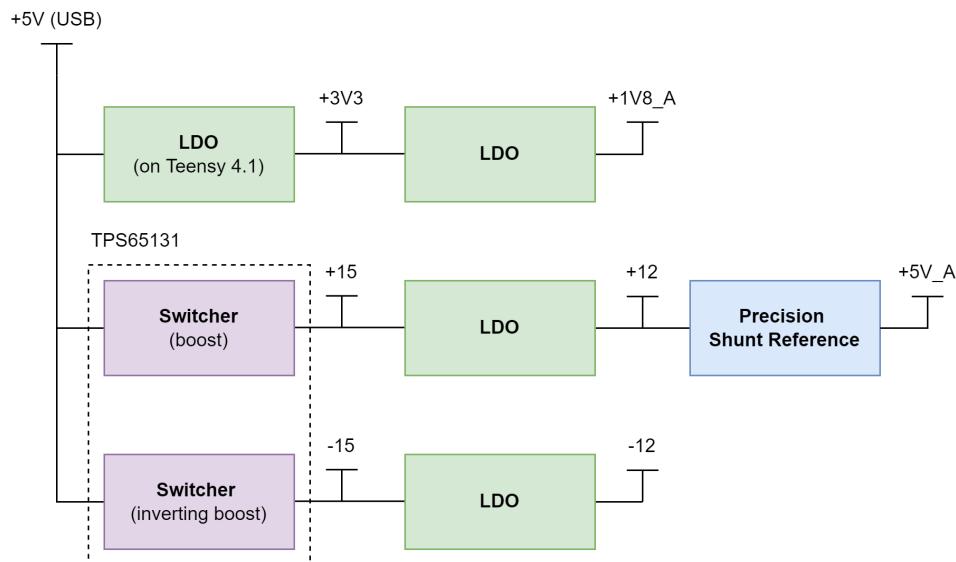


Fig. 2. Power architecture diagram.

Mechanical Data

- Dimensions are 5.10 in x 3.33 in (12.95 cm x 8.46 cm)
- Mounting: 2 x M3 mounting holes available. Hole locations shown in Fig. 3
- Thickness: 1.6 mm

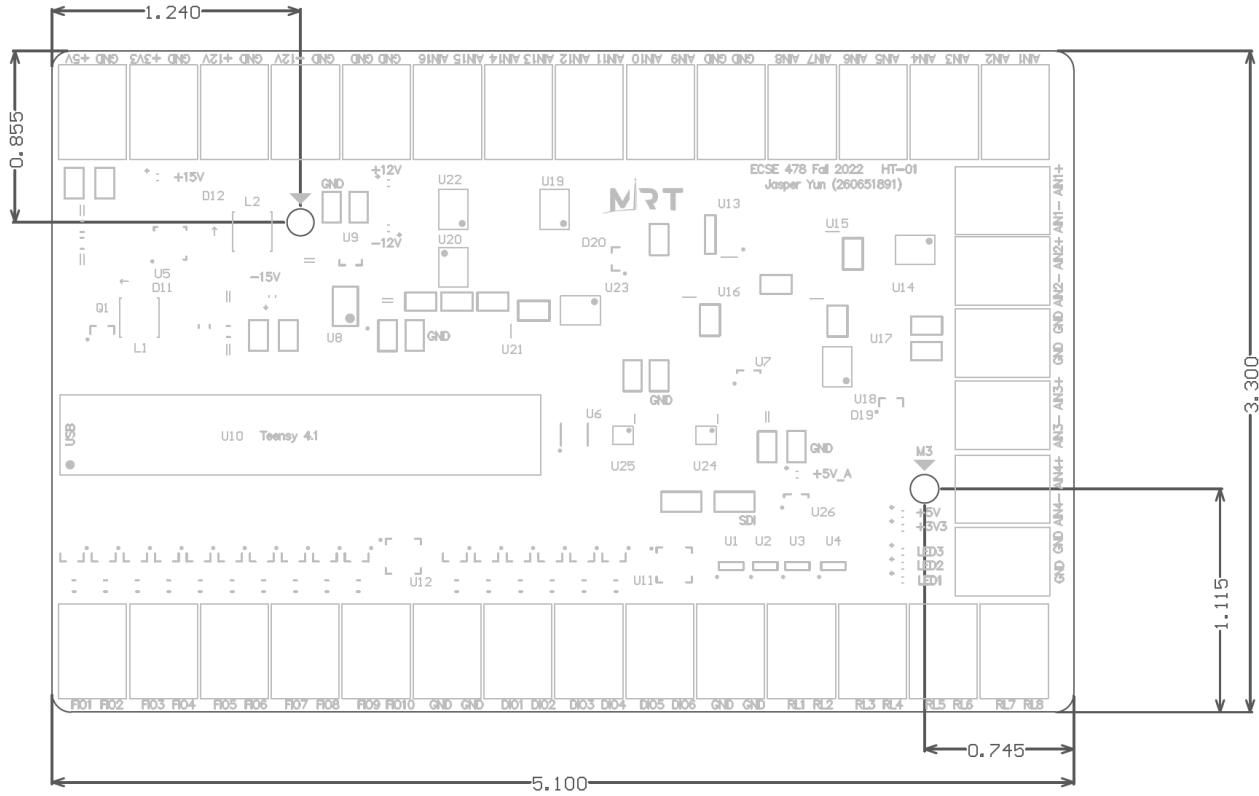


Fig. 3. Board dimensions and hole locations (top view).

Connectors

- USB connector for data and power to Teensy (communicates at USB HS 480 Mbit/s)
- Terminal blocks for all other connections
- microSD card connector built-in on Teensy 4.1 (uses 4-bit SDIO)

Schematics

Linked [here](#), temporary. The link will need to be updated once the dev_Hardware branch is merged or deleted.

Component Locations

All components are on the top layer. The current board size is constrained by the number of terminal blocks rather than component placement. Fig. 4 shows the component locations by designator. SMD resistors and capacitors also have their values marked out.

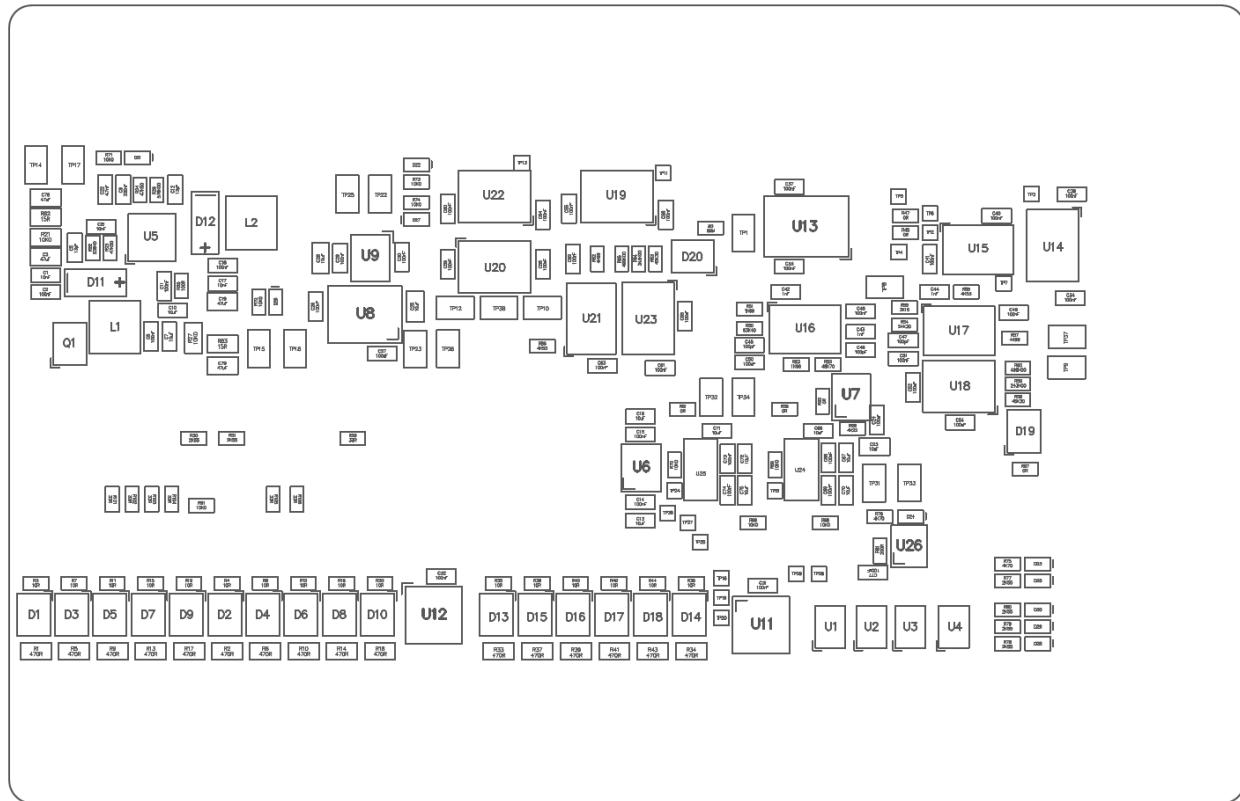


Fig. 4. Top view of the top layer assembly drawing. Please see project files for the high-resolution PDF version.

Test Points

As this is a prototype board, there are many test points for probing. Table 2 presents a list of test point reference designators and the associated net. The test point locations on the board can be found in Fig. 5.

Table 2. Test point descriptions.

Test Point Reference Designator	Net and Description
TP1	U13 Instrumentation amplifier output
TP2	U15B voltage buffer output
TP3	U14 dual 4:1 analog mux drain A output
TP4	U13 Instrumentation amplifier negative input
TP5	U13 Instrumentation amplifier positive input
TP6	U15C voltage buffer output

TP7	U14 dual 4:1 analog mux drain B output
TP8	Anti-aliasing filter output / non-inverting amplifier non-inverting input
TP9	U17C non-inverting amplifier output (differential analog inputs)
TP10	U21C non-inverting amplifier output (single-ended analog inputs)
TP11	U19 8:1 analog mux drain output
TP12	U20 dual 4:1 analog mux drain A output
TP13	U22 8:1 analog mux drain output
TP14	+15V
TP15	-15V
TP16	Internal I2C SCL (port expanders)
TP17	GND
TP18	GND
TP19	Internal I2C SDA (port expanders)
TP20	GND
TP21	SPI nCS for differential analog inputs ADC
TP22	+12V
TP23	-12V
TP24	SPI nCS for single-ended analog inputs ADC
TP25	GND
TP26	GND
TP27	SPI MISO for ADCs
TP28	Differential analog inputs ADC SDI pin
TP29	Single-ended analog inputs ADC SDI pin
TP31	+5V_A
TP32	+1V8_A
TP33	GND
TP34	GND

TP35	SPI SCLK
TP36	GND
TP37	U17C non-inverting amplifier inverting input
TP38	U21C non-inverting amplifier inverting input

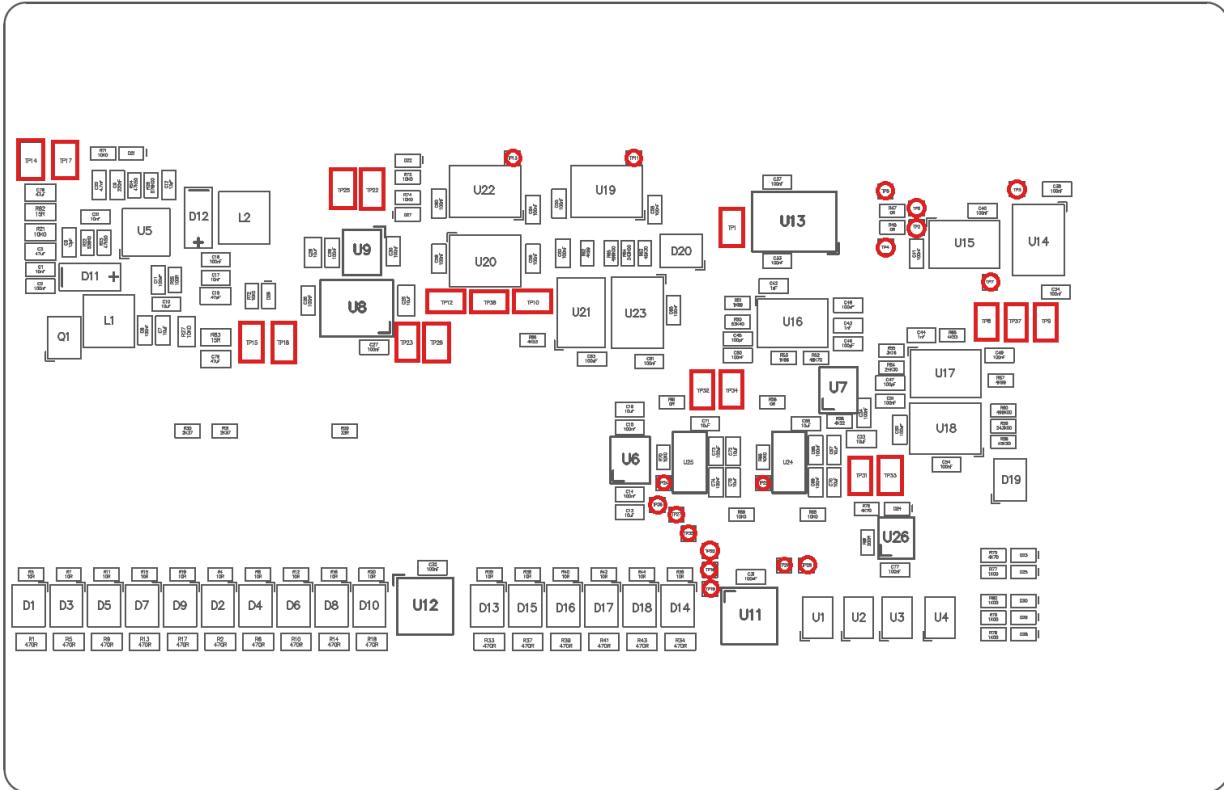


Fig. 5. Test point locations. Red rectangles represent probe clip test points (Keystone 5015) and red circles represent SMD pads. (to be updated)

Software Overview

Has not begun yet 😞

B. Testing Results

The testing methodology for the power supply characterization was described in Section V. This appendix section presents the oscilloscope screen captures for each rail.

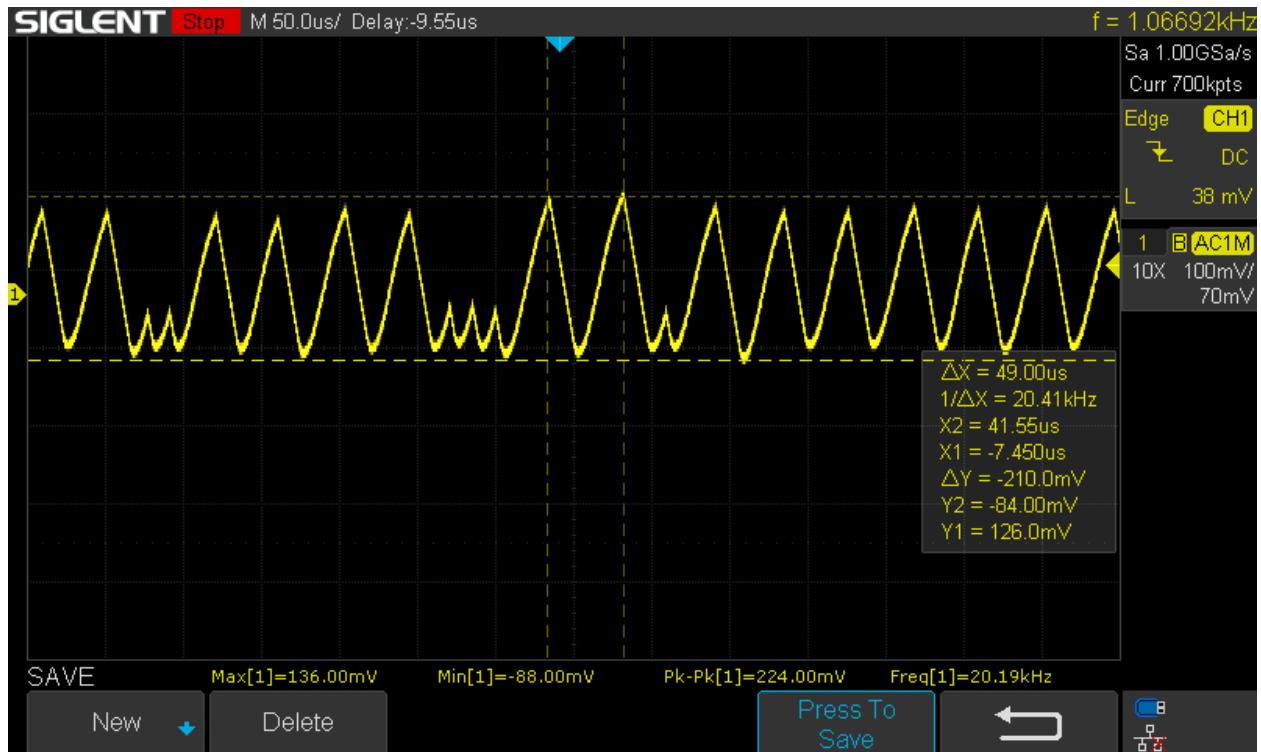


Fig. 1. Screen capture from the oscilloscope measurement of the 15 V rail.

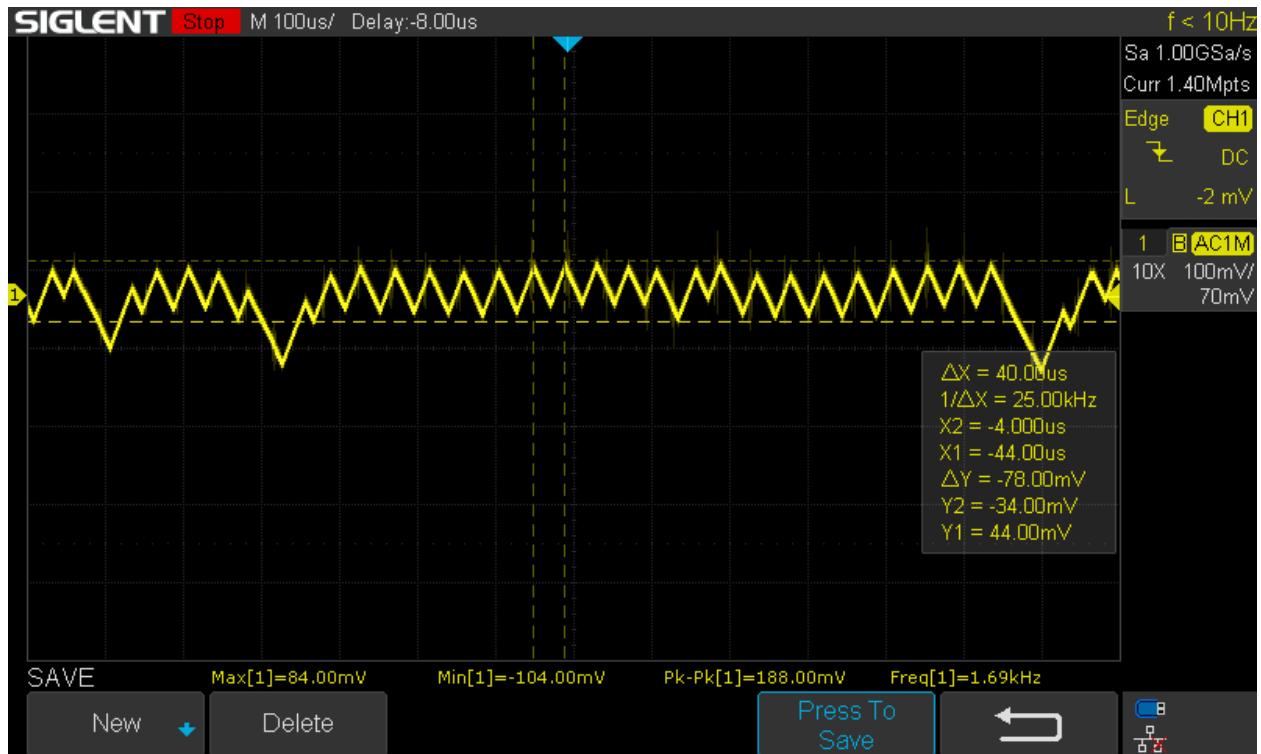


Fig. 2. Screen capture from the oscilloscope measurement of the -15 V rail.

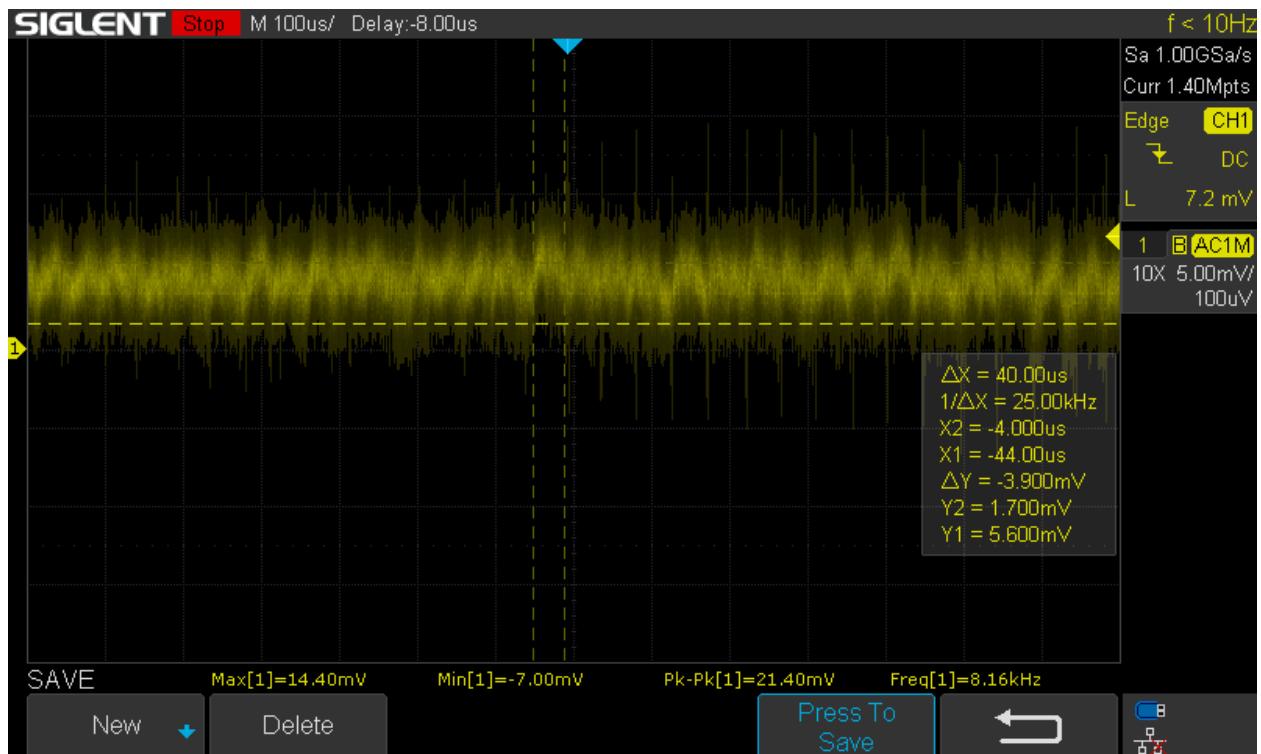


Fig. 3. Screen capture from the oscilloscope measurement of the 12 V rail.

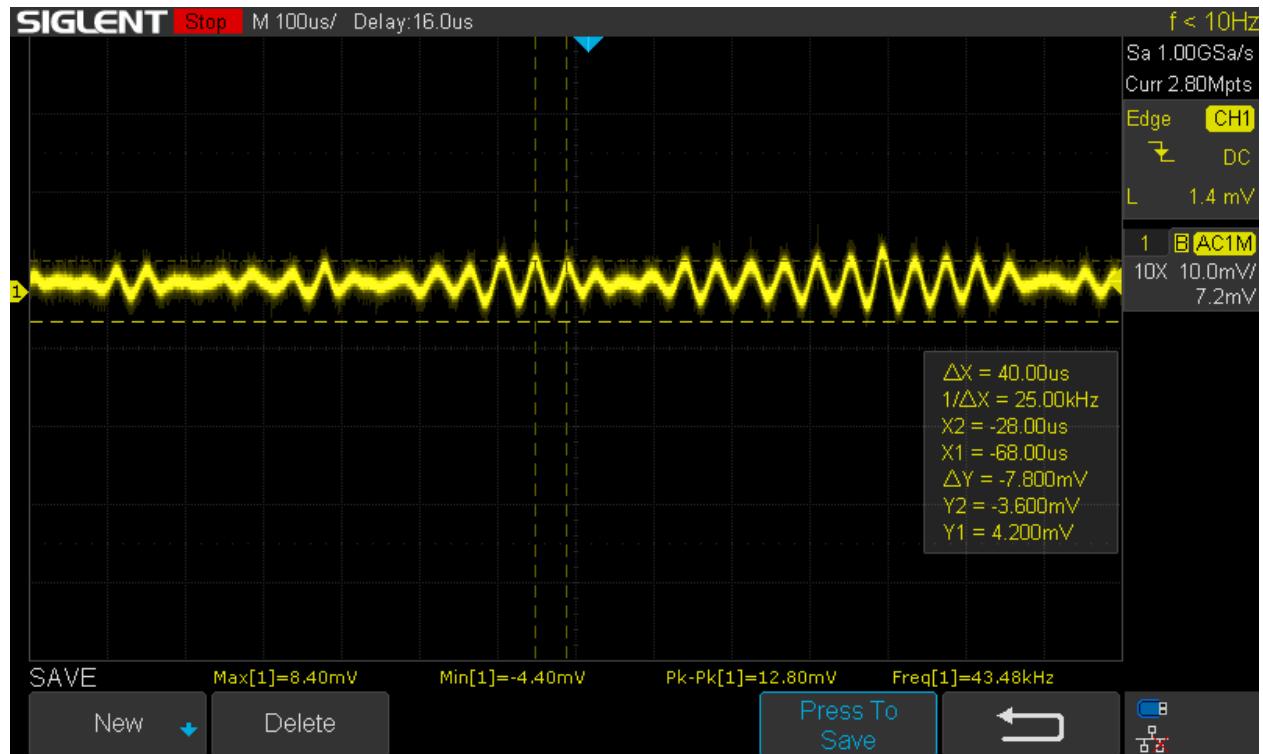


Fig. 4. Screen capture from the oscilloscope measurement of the -12 V rail.

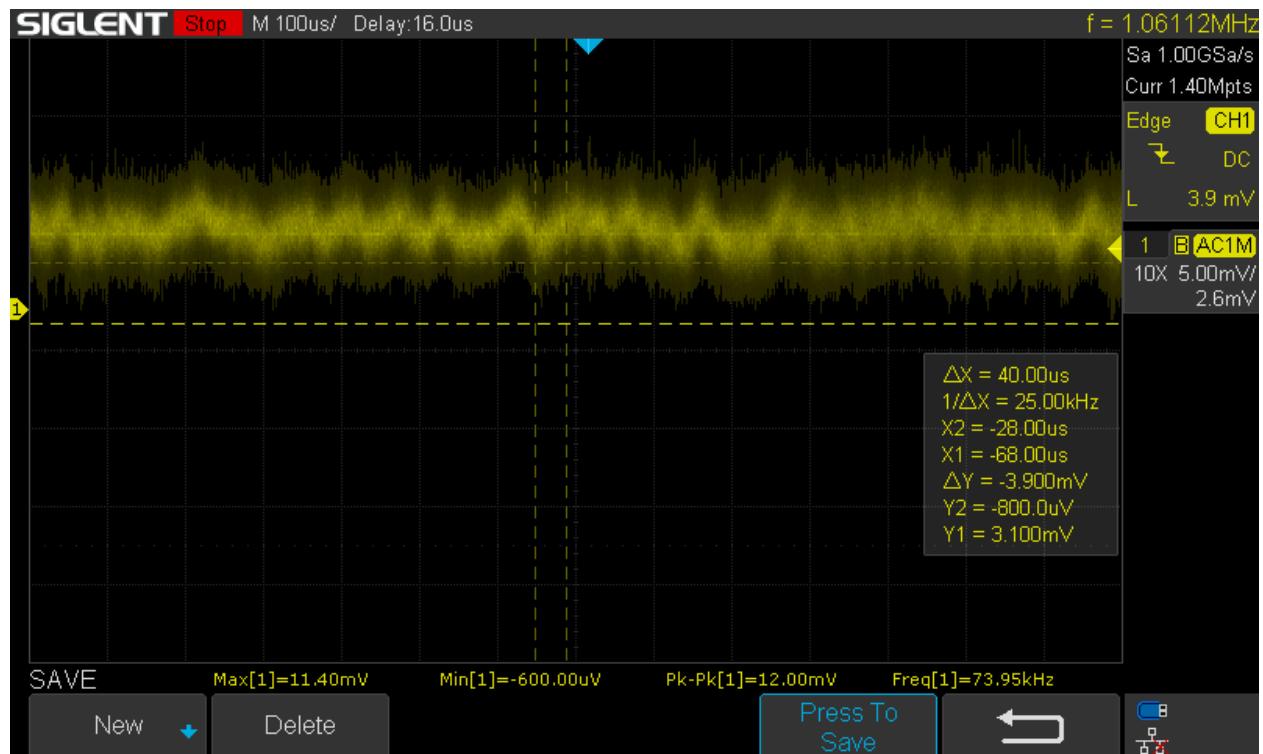


Fig. 5. Screen capture from the oscilloscope measurement of the 5 V analog rail.

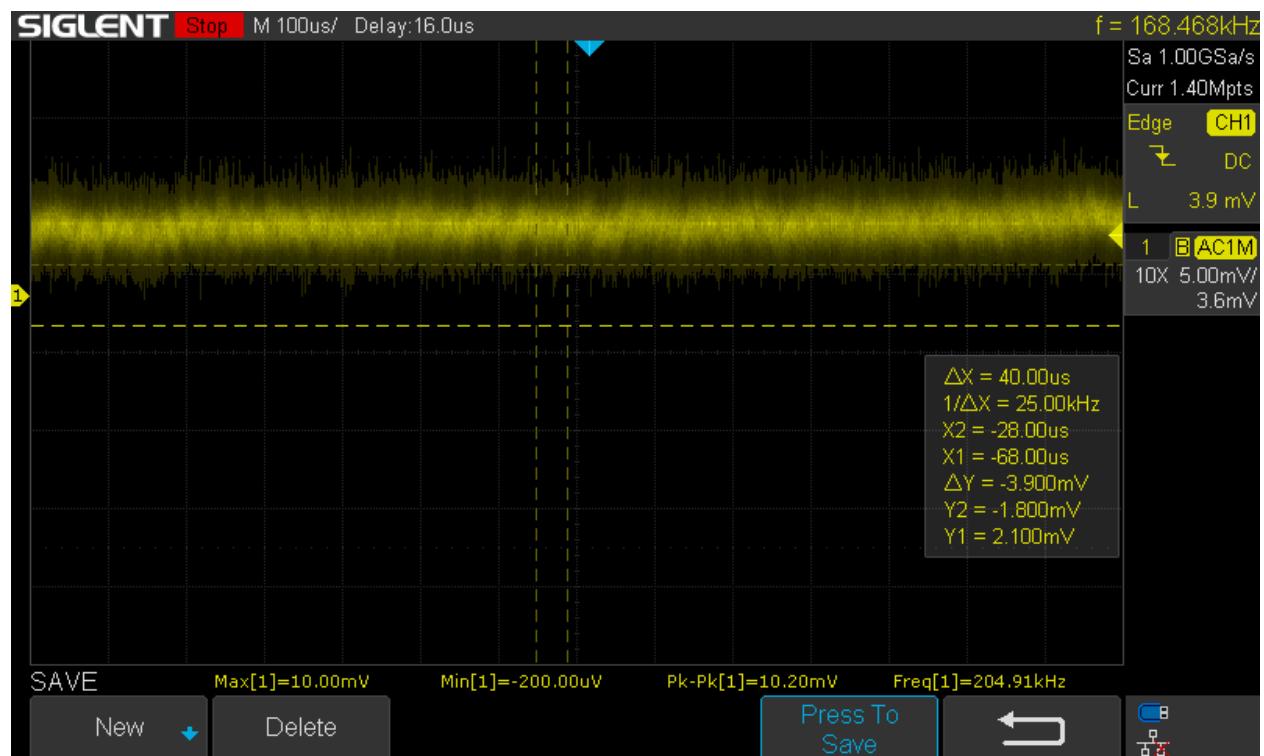


Fig. 6. Screen capture from the oscilloscope measurement of the 1.8 V analog rail.

C. Testing Data

The included PDF file contains the testing measurements and data from the testing done for the eval board.

Power Rail Measurements

with multimeter and hook probes

Rail	Voltage (V)
+15V rail	14.885
-15V rail	-14.533
+12V rail	11.909
-12V rail	-12.270
+5V (USB)	5.066
+3V3 rail	3.3189
+5V_A	4.979
+1V8_A	1.8027

with oscilloscope (settings below)

rail	ripple (mVpp)	ripple frequency	oscilloscope screenshot filename
+15V rail	224.00	20.41	25
-15V rail	188.00	25 26, 27	
+12V rail	21.40 n/a		28
-12V rail	12.80	25	29
+5V_A	12.00 n/a		31
+1V8_A	10.20 n/a		30

oscilloscope settings:

probe: 10x

bandwidth limited to 20M

rails loaded by board only (no external connections)

probe with ground spring

ac coupled

200MHz probe

probing the test points for the rails

board powered by phone charger brick

ADC Gain and Offset Measurements

Input (mV)	Hardware Output (V)	ADC averaged reading (V)	Hardware Gain (V/V)	Perceived Gain (V/V)
27.1	0.0283	0.02559	1.04428	0.94428
27.1	0.2746	0.26571	10.13284	9.80480
27.1	1.3509	1.33066	49.84871	49.10185
27.1	2.7422	2.70696	101.18819	99.88782
37.2	0.0385	0.035037	1.03495	0.94185
37.2	0.3771	0.37025	10.13710	9.95296
37.2	1.8555	1.851	49.87903	49.75806
37.2	3.7708	3.76934	101.36559	101.32634

measured with OWON B35T+
through alligator cables

measured with FLIR
clipped with hook probes

Gain Setting	Gain (V/V)	Offset (mV)
1x	1.00990099	0.931683168
10x	10.14851485	-0.424752475
50x	49.96039604	-3.026732673
100x	101.8415842	-17.70693069

Methods

Input measured at input to gain stage

Hardware Output measured at output of gain stage

ADC averaged reading used 1000 samples measured at 50 Hz

Hardware gain = Hardware Output / Input

Perceived gain = ADC averaged reading / Input

Gain and Offset calculated for ADC assuming ADC is linear and has gain and offset

Trying to Add Input Pulldown Resistors to Prevent Floating Inputs

Measurements

1 Meg pull-down (R_{pd} in picture)

Connector voltage	191 mV
Mux output	191 mV
Op-amp non-inv input	n/a not measured

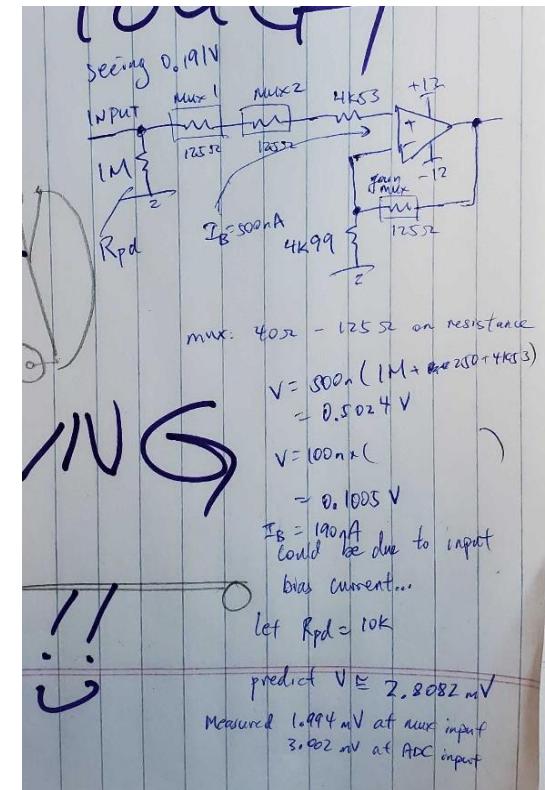
10K pull-down

Connector voltage	1.994 mV
Mux output	1.994 mV
Op-amp non-inv input	2.905 mV
ADC input	3.032 mV
Gain	1.043718 V/V

Cause: hypothesis that it is most likely due to op-amp input bias current

Calculations to estimate expected offset voltages due to bias currents:

Parameter	Min	Nom	Max	Units
RC4580 input bias current	10	100	500 nA	
2 x mux on-state resistance	80	100	250 Ohm	
Non-inv input compensation resistor	4525.47	4530	4534.53 Ohm	
Pull-down resistance on input	990000	1000000	1010000 Ohm	
Voltage at non-inv input due to bias current	9.946055	100.463	507.3923 mV	
RC4580 input bias current	10	100	500 nA	
2 x mux on-state resistance	80	100	250 Ohm	
Non-inv input compensation resistor	4525.47	4530	4534.53 Ohm	
Pull-down resistance on input	9900	10000	10100 Ohm	
Voltage at non-inv input due to bias current	0.145055	1.463	7.442265 mV	



Anti-Aliasing Filter Offset Voltage Estimations

Parameter	Tolerance	Min	Nom	Max	Units
First stage					
Anti-aliasing filter input voltage from in-amp		0.000	0.000	0.000	V
RC4580 input bias current		10.000	200.000	500.000	nA
R51	0.10%	1.688	1.690	1.692	kOhm
R50	0.10%	63.337	63.400	63.463	kOhm
Offset voltage due to bias current in this stage		0.650	13.018	32.578	mV
Non-inv input voltage		0.650	13.018	32.578	mV
Output voltage (voltage follower)		0.650	13.018	32.578	mV
Second stage					
Second stage input voltage		0.650	13.018	32.578	mV
RC4580 input bias current		10.000	200.000	500.000	nA
R53	0.10%	1.958	1.960	1.962	kOhm
R52	0.10%	48.651	48.700	48.749	kOhm
Offset voltage due to bias current in this stage		0.506	10.132	25.355	mV
Non-inv input voltage		1.156	23.150	57.933	mV
Output voltage (voltage follower)		1.156	23.150	57.933	mV
Third stage					
Third stage input voltage		1.156	23.150	57.933	mV
RC4580 input bias current		10.000	200.000	500.000	nA
R55	0.10%	3.157	3.160	3.163	kOhm
R54	0.10%	24.276	24.300	24.324	kOhm
Offset voltage due to bias current in this stage		0.274	5.492	13.744	mV
Non-inv input voltage		1.431	28.642	71.677	mV
Output voltage (voltage follower)		1.431	28.642	71.677	mV
Anti-aliasing filter output voltage		1.431	28.642	71.677	mV

Anti-Aliasing Filter Offset Voltage Measurements

Measurements (tested at DC)

First stage

Anti-aliasing filter input voltage from in-amp	0.281 mV
Non-inv input voltage	13.026 mV
Output voltage	13.686 mV

Second stage

Non-inv input voltage	23.001 mV
Output voltage	24.338 mV

Third stage

Non-inv input voltage	29.269 mV
Output voltage	29.843 mV
Gain	1.020 V/V

Gain stage

Non-inv input voltage	30.64 mV
Final output voltage	31.042 mV

Total offset voltage developed across filter

30.761 mV

Test setup

Multimeter measures voltages (probed sequentially)

SPD3303X-E DC power supply provides 3.20V to shorted differential inputs

Gain stage on HS DE inputs was set to unity gain

Anti-Aliasing Filter Offset

Voltage Measurements

Before adding compensation resistors

	ADC reading	units	
Vout-1v/v	0.03	v	Adding compensation resistors to each stage of the AA filter to reduce offset voltage developed across the filter
Vout-10v/v	0.3	v	
Vout-50v/v	1.49	v	
Vout-100v/v	3.03	v	observed trend is that offset voltage reduces significantly with each added compensation resistor

Add 63k4

Vout-1v/v	0.01739	v
Vout-10v/v	0.16354	v
Vout-50v/v	0.80611	v
Vout-100v/v	1.63206	v

Add 48k7

Vout-1v/v	0.0061	v
Vout-10v/v	0.05065	v
Vout-50v/v	0.24623	v
Vout-100v/v	0.49886	v

Add 24k3

Vout-1v/v	forgot	v
Vout-10v/v	forgot	v
Vout-50v/v	forgot	v
Vout-100v/v	forgot	v

Testing on op amp only board,
measurements with FLIR DM92

sad forgot to check vout of third stage which is different from final vout (output of gain stage)

RC4580 op amp	Filter Vin (V)	First Stage Vout (V)	Second Stage Vout (V)	Final Vout (V)	Final Vout - Vin (mV)
GNDed input to AA filter (at in-amp)	0.000013	0.01311	0.02349	0.029953	29.94
2.5V input to AA filter, unity gain	2.5263	2.539	2.5491	2.5555	29.2
3.3V input, unity gain	3.3164	3.329	3.339	3.3453	28.9

Conditions: No compensation resistors (no rework), powered by +/-12V from SPD3303x-e supply in slave mode, unity

TLV2172 op amp	Filter Vin (V)	First Stage Vout (V)	Second Stage Vout (V)	Final Vout (V)	Final Vout - Vin (mV)
GNDed input to AA filter (at in-amp)	-0.000017	0.000294	0.00043	0.000076	0.093
2.5V input to AA filter, unity gain	2.5264	2.5268	2.527	2.5266	0.2
3.3V input, unity gain	3.3165	3.3169	3.317	3.3168	0.3

Conditions: same as RC4580 op amp

TLV2172 op amp with compensation	Filter Vin (V)	First Stage Vout (V)	Second Stage Vout (V)	Final Vout (V)	Final Vout - Vin (mV)
GNDed input to AA filter (at in-amp)	0.000001	0.000303	0.000436	0.000088	0.087
2.5V input to AA filter, unity gain	2.5268	2.5271	2.5274	2.5271	0.3
3.3V input, unity gain	3.3171	3.3174	3.3176	3.3173	0.2

TLV2172 op amp with reworks but 0 ohm	Filter Vin (V)	First Stage Vout (V)	Second Stage Vout (V)	Final Vout (V)	Final Vout - Vin (mV)
GNDed input to AA filter (at in-amp)	0.000002	0.000297	0.000436	0.000083	0.081
2.5V input to AA filter, unity gain	2.527	2.5273	2.5274	2.5271	0.1
3.3V input, unity gain	3.3171	3.3174	3.3176	3.3173	0.2

RC4580 op amp with compensation (on)	Filter Vin (V)	First Stage Vout (V)	Second Stage Vout (V)	Final Vout (V)	Final Vout - Vin (mV)
GNDed input to AA filter (at in-amp)	0.000298	-0.0975	-0.08669	-0.02721	-27.508
2.5V input to AA filter, unity gain	2.527	2.5273	2.5274	2.5271	0.1
3.3V input, unity gain	3.3171	3.3174	3.3176	3.3173	0.2

RC4580 with compensation, check vout	Vin- (V)	Vin+ (V)	output of in-amp	output of gain stage
			Vout_ina (V)	Vout_final (V)
Unity gain	1.50	1.50	0.0011	-0.0242
	1.50	1.55	0.051	0.0281
	1.50	1.60	0.1008	0.0789
	1.50	1.65	0.1504	0.1294
	1.50	1.75	0.25	0.2303
	1.50	2.00	0.5006	0.4842
	1.50	2.25	0.749	0.7376
	1.50	2.50	0.998	0.9905
	1.50	3.00	1.496	1.4972
	1.50	3.50	1.995	2.0041
	1.50	4.00	2.494	2.5107
	1.50	4.50	2.992	3.0182
	1.50	6.00	4.49	4.539

RC4580 with compensation, check vout	Vin- (V)	Vin+ (V)	Vout_ina (V)	Vout_final (V)
10x gain	1.50	1.50	0.0011	-0.0363
	1.50	1.51	0.0105	0.0566
	1.50	1.52	0.0206	0.1581
	1.50	1.53	0.0307	0.2614
	1.50	1.54	0.0408	0.3628
	1.50	1.55	0.0509	0.4656
	1.50	1.60	0.1008	0.9697
	1.50	1.65	0.1505	1.4724
	1.50	1.70	0.2006	1.9802
	1.50	1.75	0.2501	2.4793
	1.50	1.80	0.2998	2.9835
	1.50	1.90	0.4002	3.9981
	1.50	1.95	0.4501	4.498

RC4580 with compensation, check vout		Vin- (V)	Vin+ (V)	Vout_ina (V)	Vout_final (V)
50x gain		1.50	1.50	0.0007	-0.1599
		1.50	1.51	0.0101	0.2696
		1.50	1.52	0.0201	0.7695
		1.50	1.53	0.0306	1.2836
		1.50	1.54	0.0407	1.7894
		1.50	1.55	0.0507	2.2924
		1.50	1.56	0.0608	2.7956
		1.50	1.57	0.0709	3.2993
		1.50	1.58	0.0805	3.7745
		1.50	1.59	0.0905	4.27
		1.50	1.60	0.1005	4.773

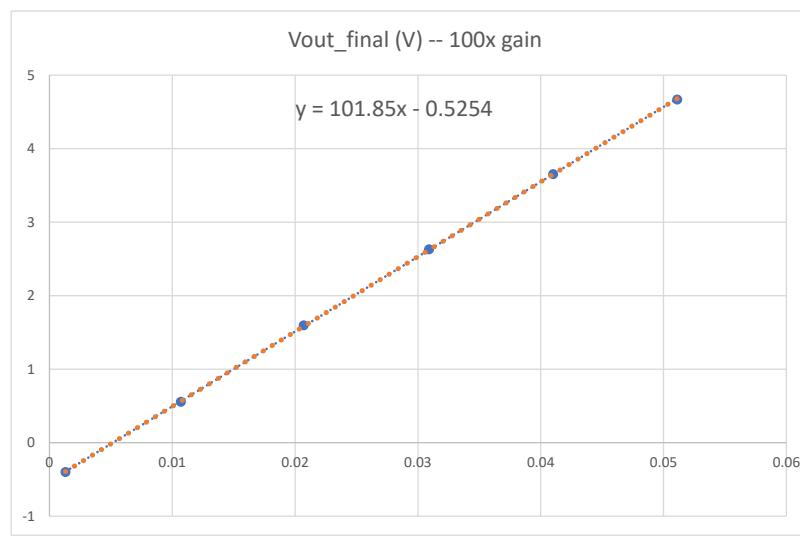
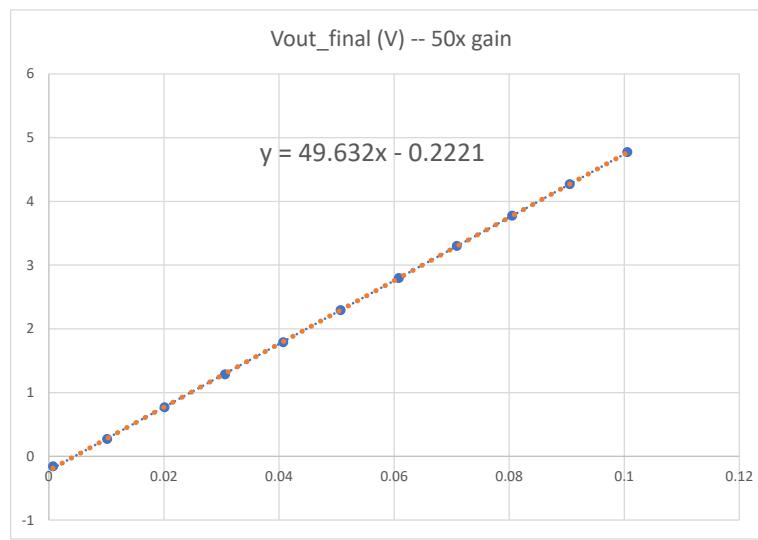
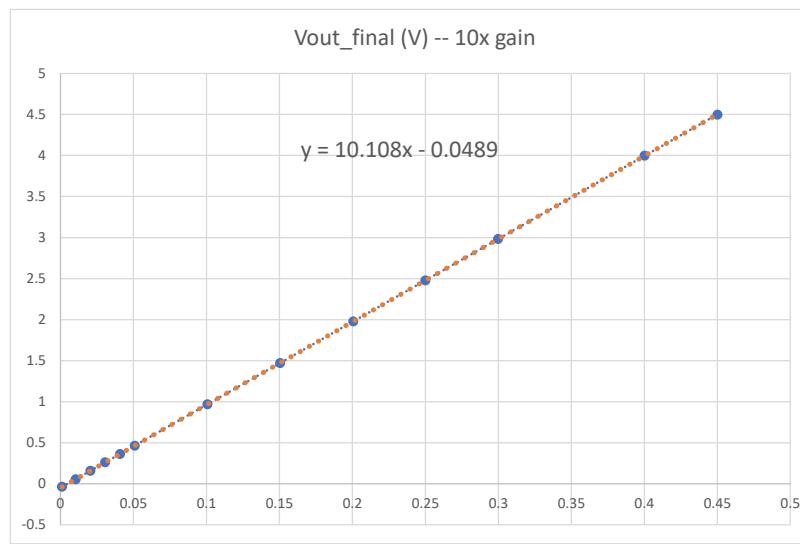
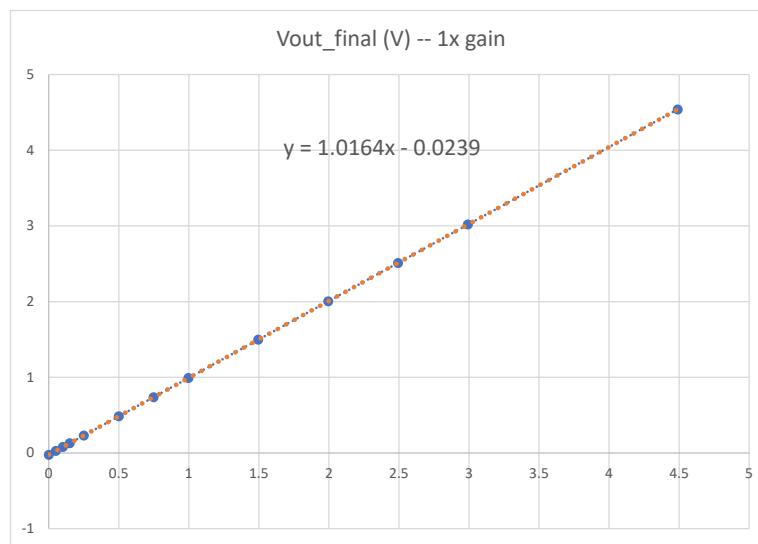
RC4580 with compensation, check vout		Vin- (V)	Vin+ (V)	Vout_ina (V)	Vout_final (V)
100x gain		1.50	1.50	0.0013	-0.3979 clamped
		1.50	1.51	0.0107	0.5564 by schottky diode
		1.50	1.52	0.0207	1.5953
		1.50	1.53	0.0309	2.6301
		1.50	1.54	0.041	3.6529
		1.50	1.55	0.0511	4.669

Manual calculations of gain and offset	x1 (V)	y1 (V)	x2 (V)	y2 (V)
1x gain	0.0011	-0.0242	4.49	4.539
10x gain	0.0011	-0.0363	0.4501	4.498
50x gain	0.0007	-0.1599	0.1005	4.773
100x gain	0.0013	-0.3979	0.0511	4.669

	gain (V/V)	offset (V)	trend gain (V/V)	trend offset (V)
1x gain	1.0166	-0.0253	1.0164	-0.0239
10x gain	10.0987	-0.0474	10.108	-0.0489
50x gain	49.4279	-0.1945	49.632	-0.2221
100x gain	101.7450	-0.5302	101.85	-0.05254

1x, 10x gains are within tolerance

50x, 100x gains are slightly outside, probably due to imprecise multimeter measurements.
should redo with averaging of e.g. 10000 samples over 2 sec, use labjack?

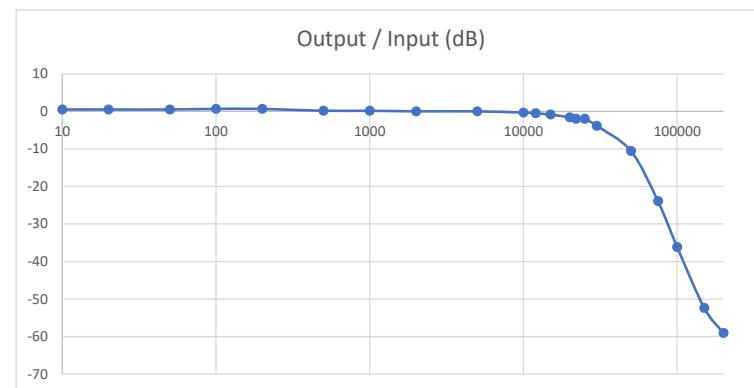
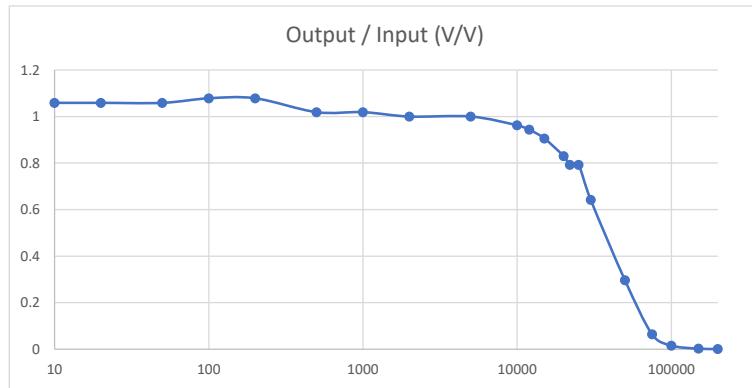


Anti-Aliasing Filter Magnitude Response

Keeping AA filter as designed in schematic, no compensation resistors in feedback path

In+ is a sinusoid from signal generator

Input+ sinusoid (1Vpp)					Hardware output sinusoid				
In-(DC) (V)	In+ offset (V)	In+ Freq (Hz)	In+ mean (oscope) (V)	Input Vpp (V)	Output mean (V)	Output freq (Hz)	Output Vpp (V)	Output / Input (V/V)	Output / Input (dB)
1.4989	2.00	10	1.99	1.02	0.52893	10	1.08	1.058823529	0.496472
1.4991	2.00	20	2.01	1.02	0.5335	20	1.08	1.058823529	0.496472
1.4991	2.00	50	2	1.02	0.5335	20	1.08	1.058823529	0.496472
1.4991	2.00	100	2	1.02	0.52929	100	1.1	1.078431373	0.65585
1.4991	2.00	200	2.01	1.02	0.53395	199.98	1.1	1.078431373	0.65585
1.4991	2.00	500	2	1.06	0.5295	499.99	1.08	1.018867925	0.162358
1.4991	2.00	1000	2.01	1.06	0.53255	1000	1.08	1.018867925	0.162358
1.4991	2.00	2000	2.01	1.06	0.5323	2000	1.06	1	0
1.4991	2.00	5000	2.01	1.06	0.5323	5000	1.06	1	0
1.4991	2.00	10000	2.01	1.06	0.53202	10000	1.02	0.962264151	-0.33411 noticeable phase shift occurring
1.4991	2.00	12000	2.01	1.06	0.5268	12000	1	0.943396226	-0.50612
1.4991	2.00	15000	2	1.06	0.5177	15000	0.96	0.905660377	-0.86069 averaging 128 samples on acquisition from now on
1.4991	2.00	20000	2.01	1.06	0.53135	20000	0.88	0.830188679	-1.61646
1.4991	2.00	22000	2.01	1.06	0.53806	22000	0.84	0.79245283	-2.02053
1.4991	2.00	25000	1.99	1.06	0.5215	25000	0.84	0.79245283	-2.02053
1.4991	2.00	30000	1.98	1.06	0.51345	30000	0.68	0.641509434	-3.85594
1.4991	2.00	50000	1.99	1.08	0.5162	50000	0.32	0.296296296	-10.5655
1.4991	2.00	75000	1.98	1.08	0.5314	75000	0.0688	0.063703704	-23.9167
1.4991	2.00	100000	1.98	1.08	0.53082	100000	0.0168	0.015555556	-36.1623
1.4991	2.00	150000	1.98	1.08			0.0026	0.002407407	-52.369
1.4991	2.00	200000	1.98	1.08			0.0012	0.001111111	-59.0849 looked like a flat line...
									oscilloscope doesn't go smaller than 5mV/div



Ltspice filter simulation points for graphing

Freq (Hz) Mag (dB)

10	0
20	0
50	0
100	0
200	0
500	-0.001
1000	-0.004
2000	-0.016
5000	-0.101
10000	-0.399
12000	-0.576
15000	-0.883
20000	-1.556
22000	-1.878
25000	-2.413
30000	-3.467
50000	-10.2
75000	-22.903
100000	-36.157
150000	-54.75
200000	-68.852

APPENDIX C MCP33151 EVALUATION BOARD

A. *Introduction*

This appendix contains the schematics and other documentation for the DAQ device PCB. Specifically,

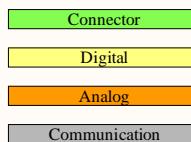
- Schematics
- Draftsman document (layers)
- Bill of Materials with cost analysis
- Testing data

ECSE478 - DAQ Device

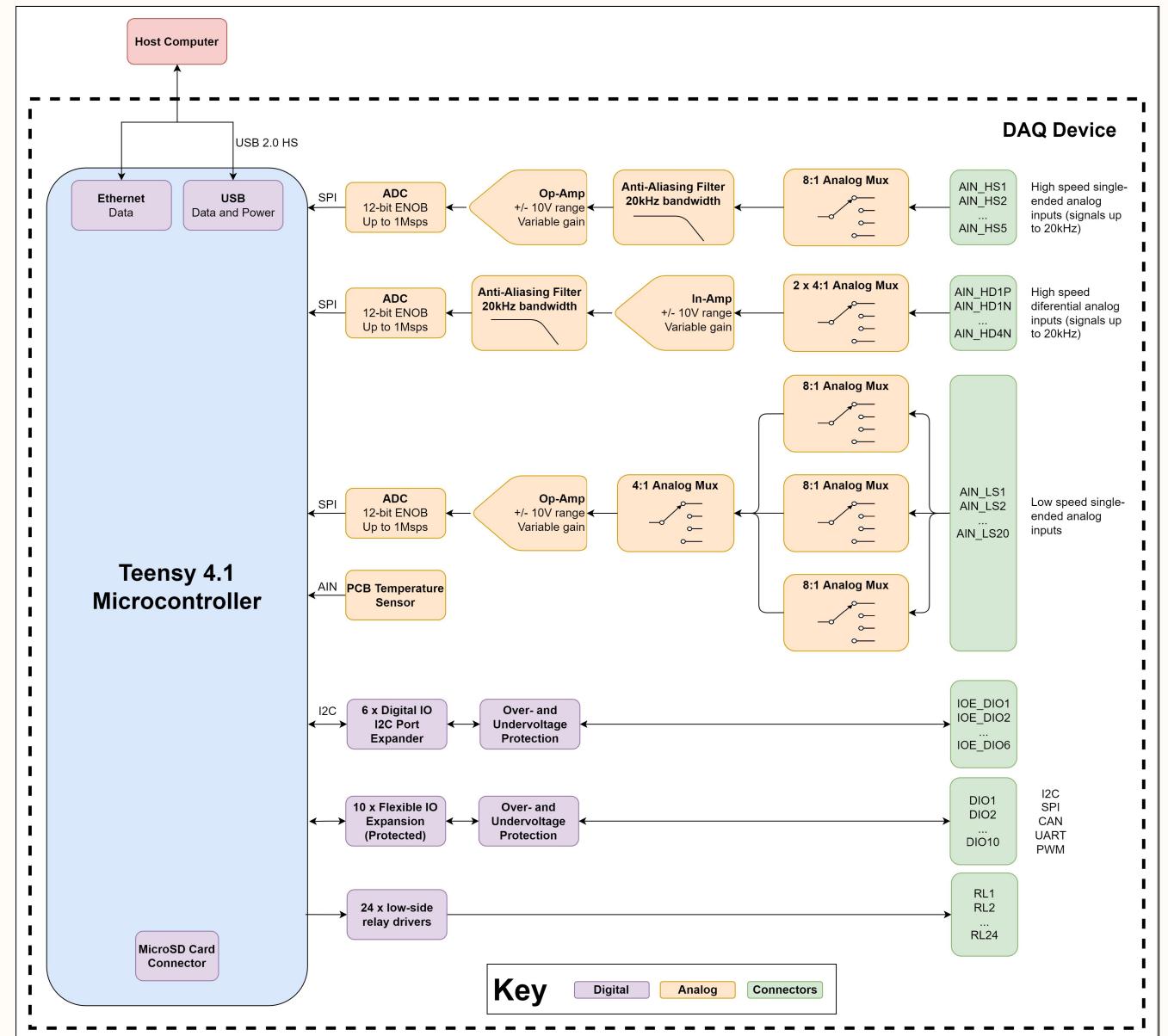
Table of Contents

- 1 Cover
- 2 Connectors - Analog
- 3 Connectors - Digital
- 4 Power
- 5 Microcontroller
- 6 IO Expansion
- 7 Digital IO Protection
- 8 Relay Drivers
- 9 Analog - High Speed Single-Ended
- 10 Analog - High Speed Differential
- 11 Analog - Low Speed Single-Ended
- 12 ADC
- 13 Debug

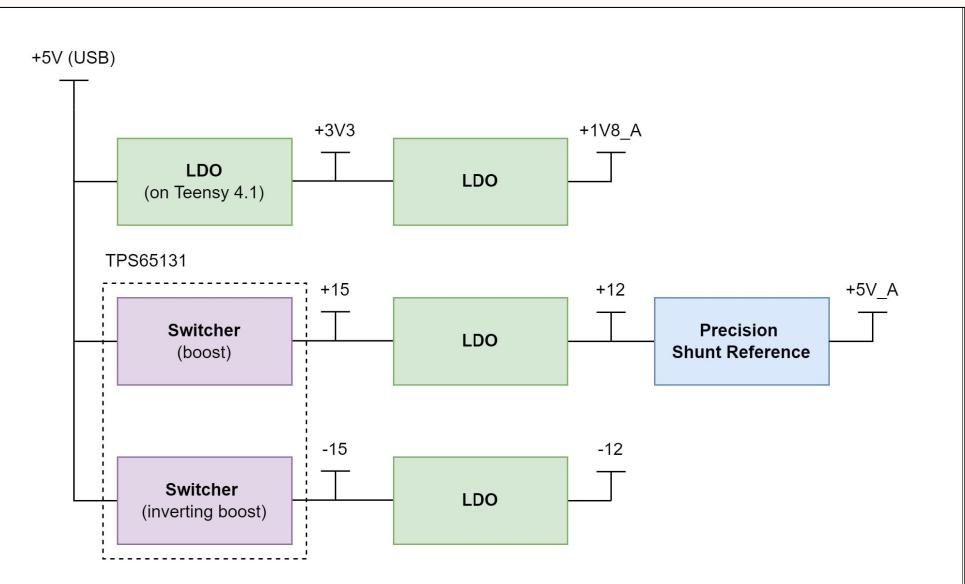
Port Colors



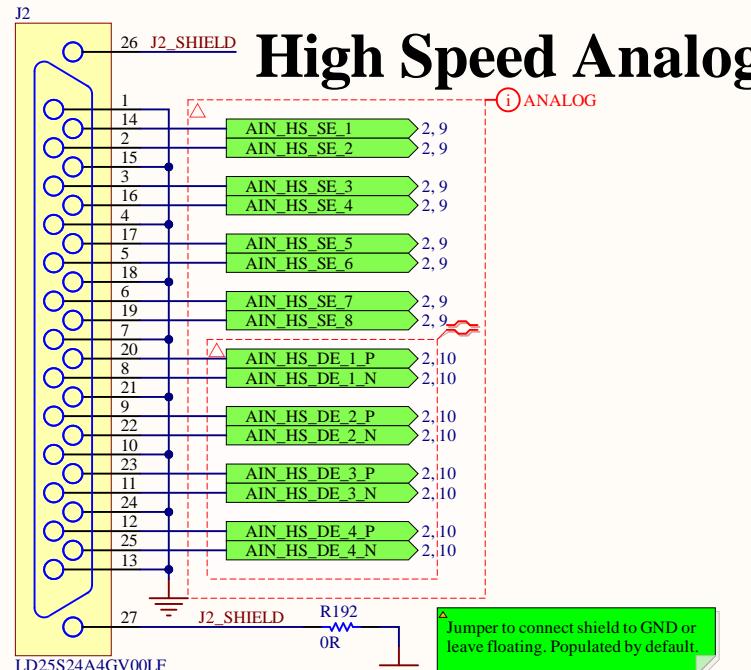
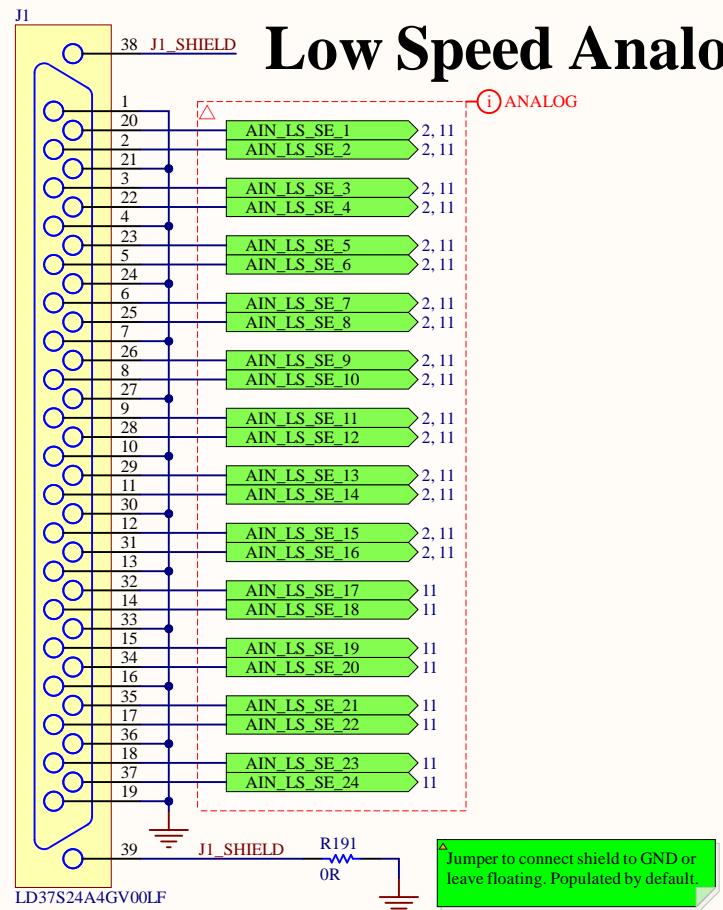
Main Block Diagram



Power Architecture

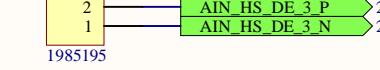
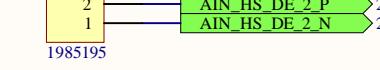
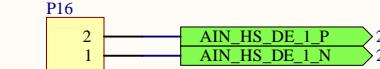
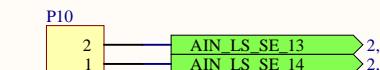
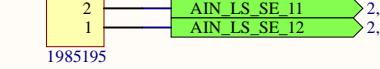
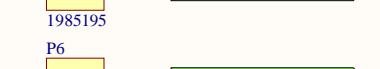
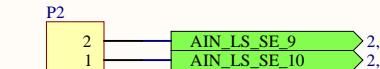
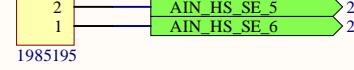
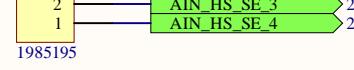
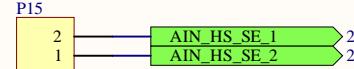
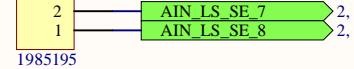
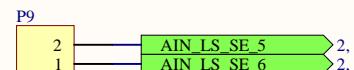
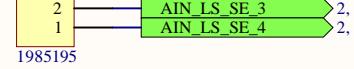
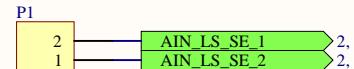


DE = differential-ended
SE = single-ended

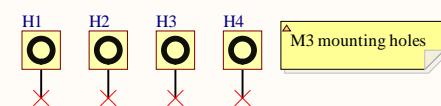
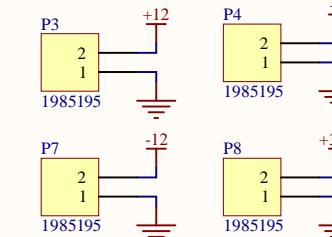


Connectors - Analog

Terminal blocks are used alongside DB25 and DB37 connectors to allow quick connections, e.g. during prototyping, and full expansion use.



Power



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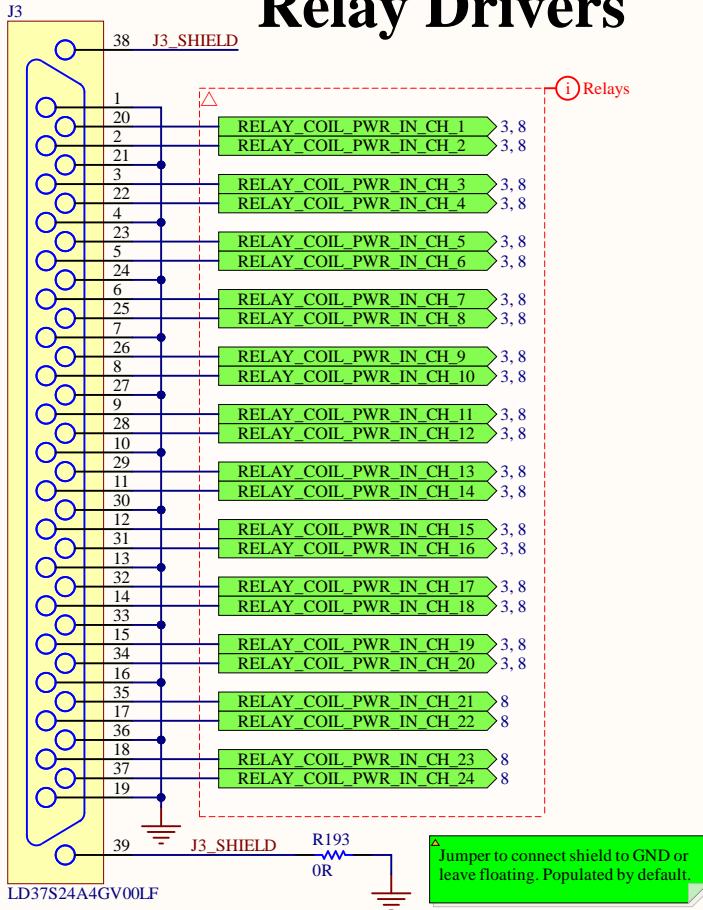
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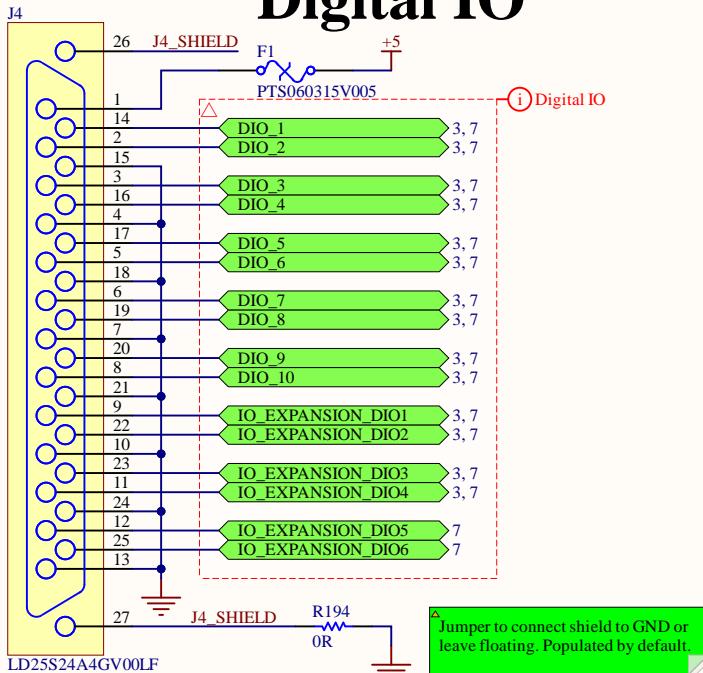
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Relay Drivers

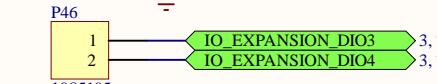
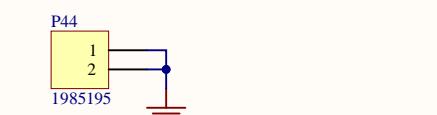
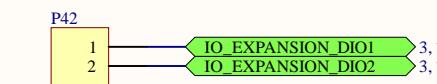
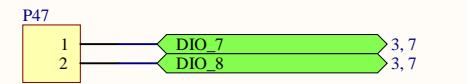
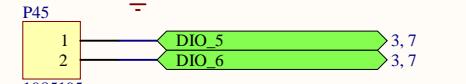
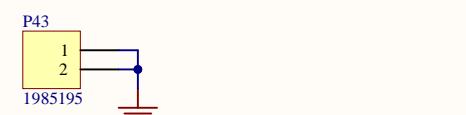
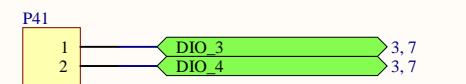
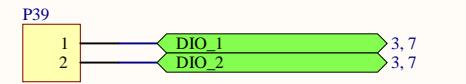
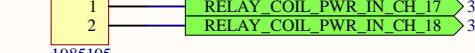
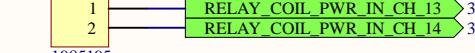
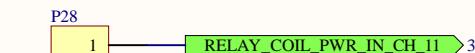
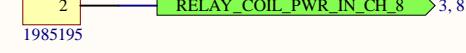
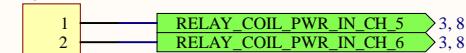
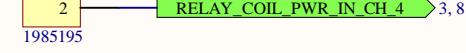
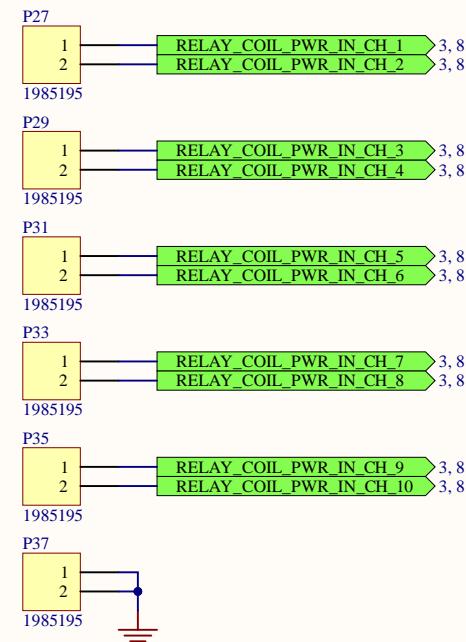


Digital IO



Connectors - Digital

Terminal blocks are used alongside DB25 and DB37 connectors to allow quick connections, e.g. during prototyping, and full expansion use.

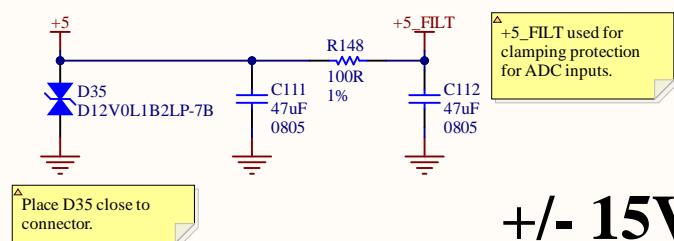


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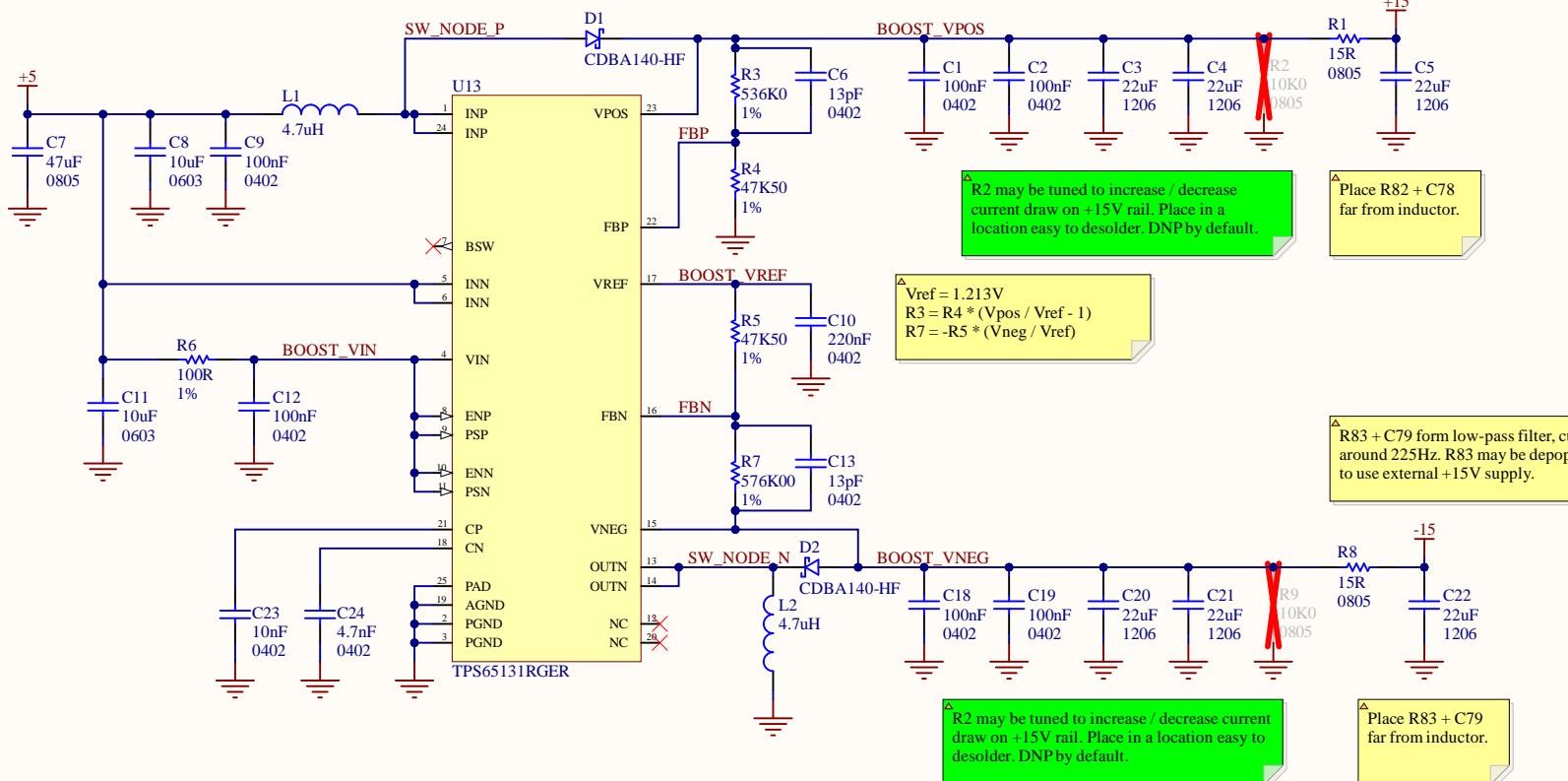


Power



+/- 15V

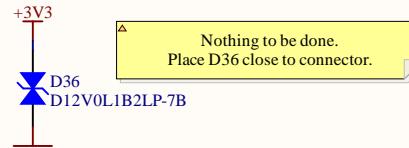
Rail	Min	Nom	Max
+15 V	14.47 V	14.90 V	15.33 V
-15 V	-15.15 V	-14.71 V	-14.26 V



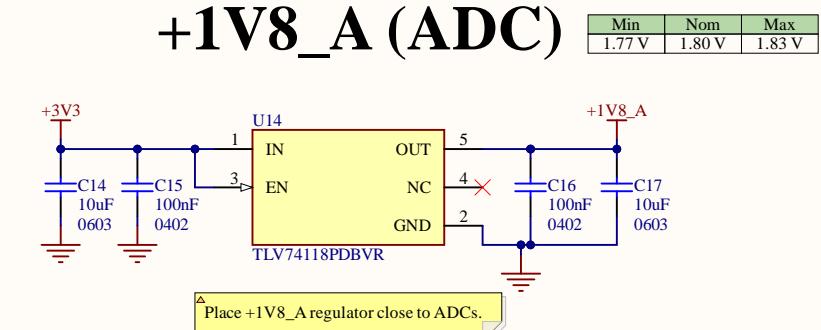
+5V (from USB port on Teensy :))

Nothing to be done.

+3V3 (from Teensy :))

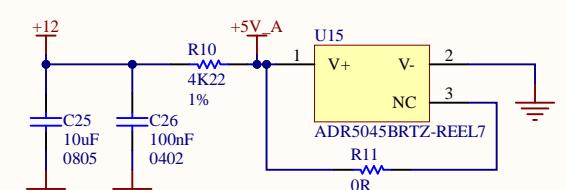
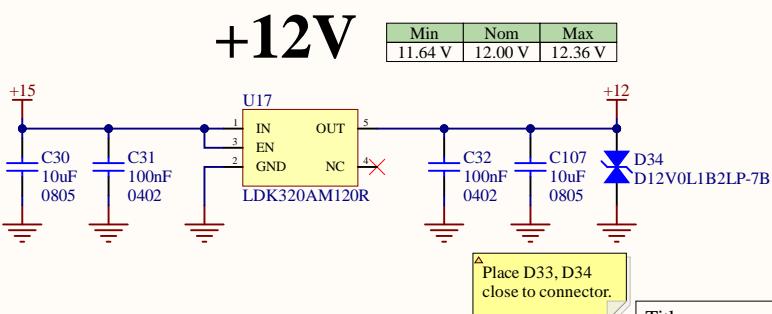
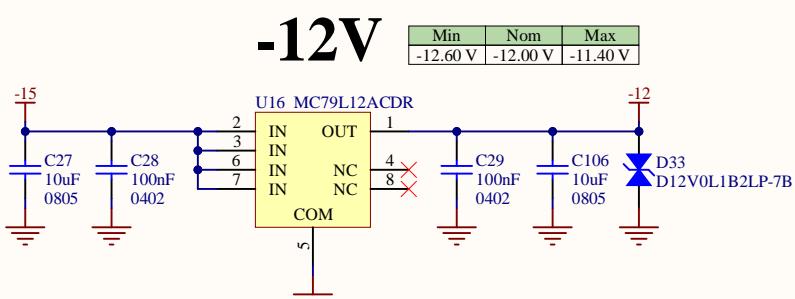


+1V8_A (ADC)



+5V_A (Analog Reference)

Voltage reference IC. Keep away from noisy sources and place close to ADCs.



Title **Power**

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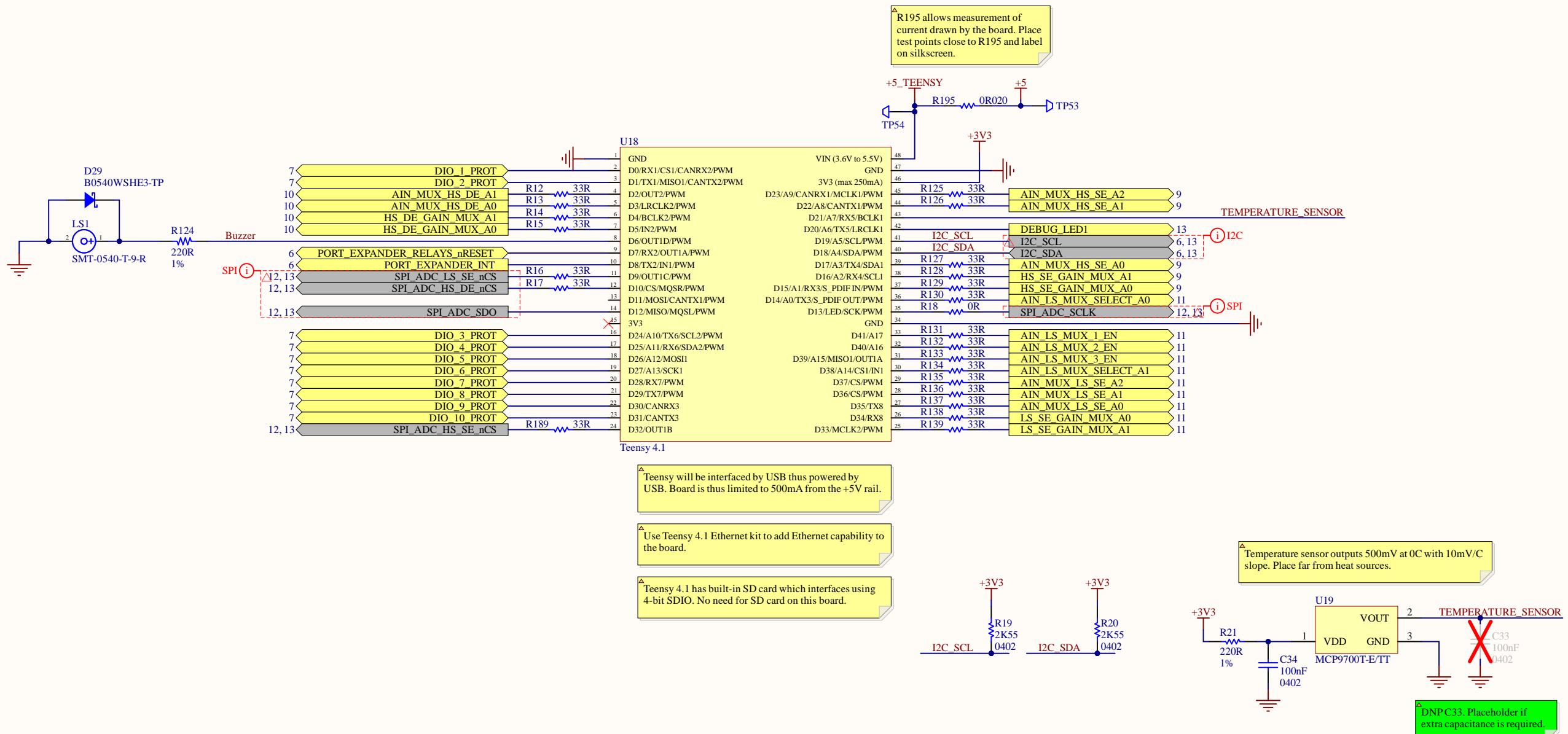
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Montreal, Quebec



Microcontroller



Title

Microcontroller

Size: B | Revision: * | Drawn By: Jasper Yun

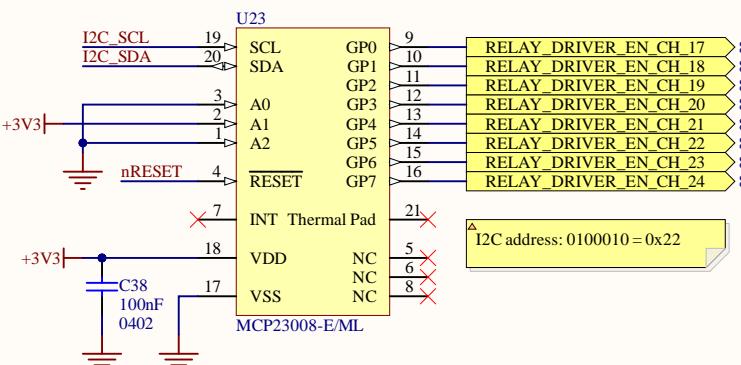
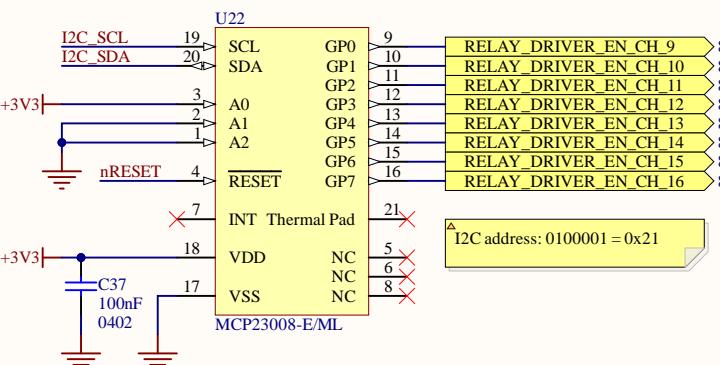
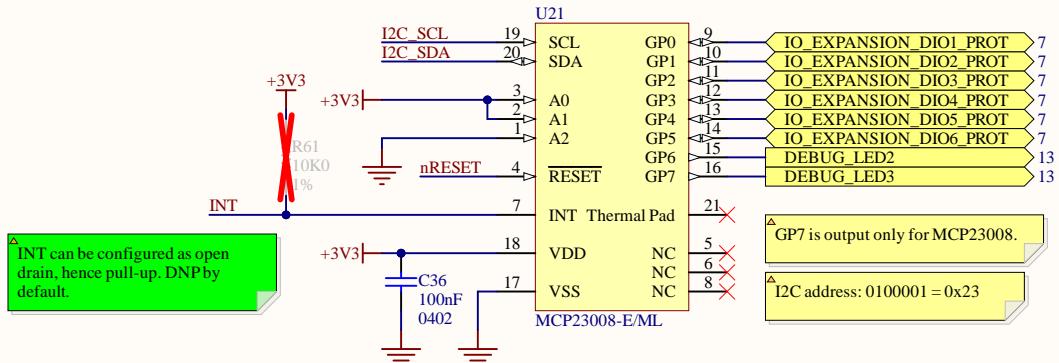
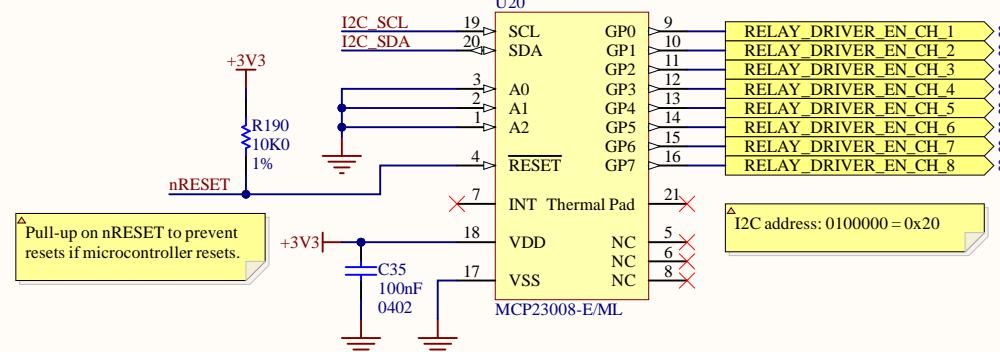
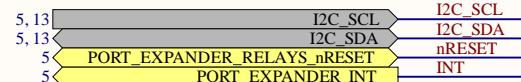
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File: C:\Users\jaspe\Desktop\ecse478_honours_thesis\1 Hardware\ECSE478 - DAQ Device\Microcontroller.SchDoc

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IO Expansion



These 24 IO expansion pins can be set as inputs or outputs. They will be configured as outputs only for relay driver control, as relay actuation does not require high speed actuation from microcontroller pins. Interrupts not needed.

GP7 is output-only on MCP23008.

I₂C address is of format: 0100 (A2) (A1) (A0)

Title

IO Expansion

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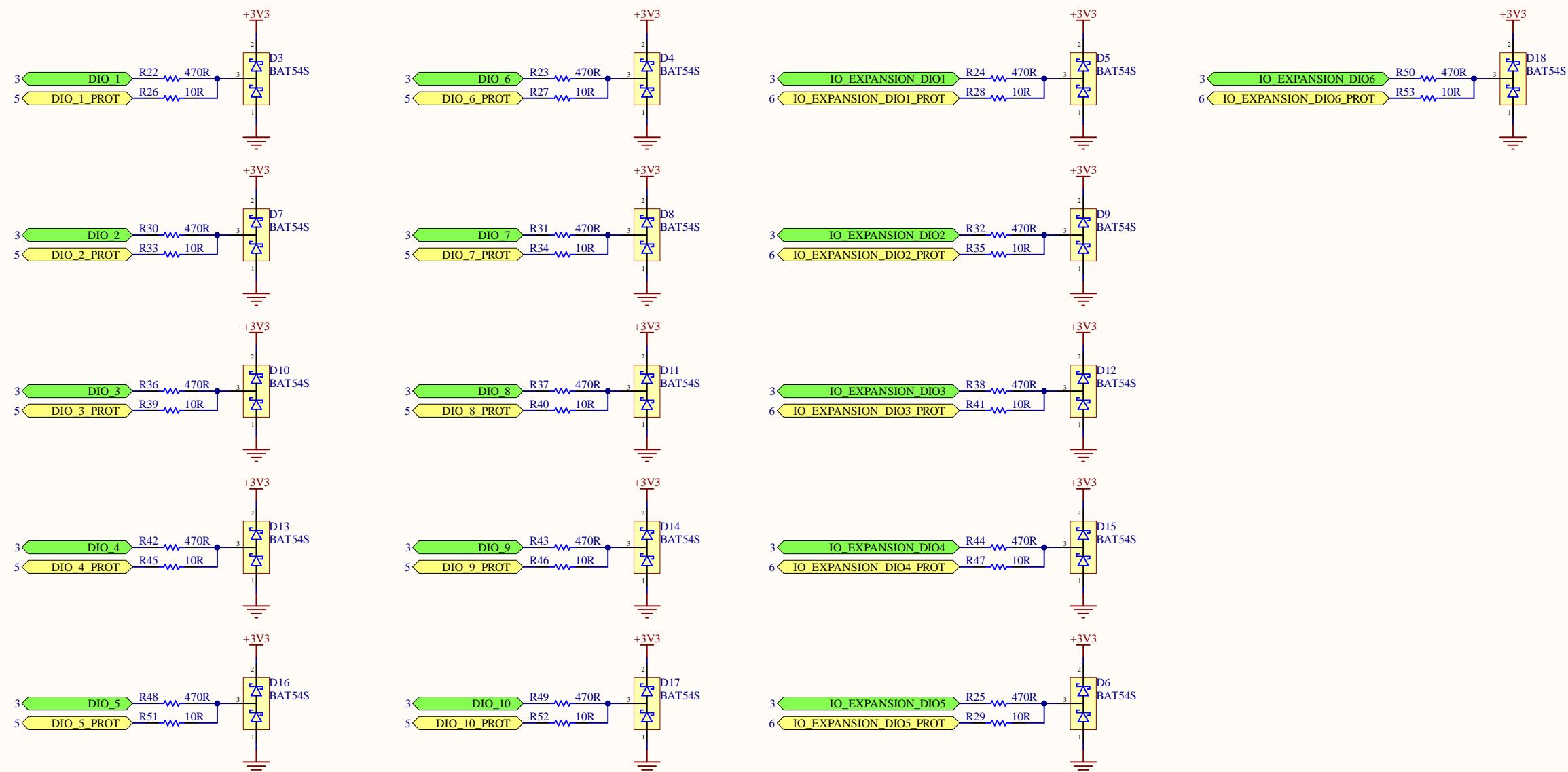
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Digital IO Protection



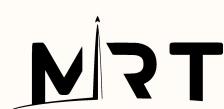
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Digital IO Protection

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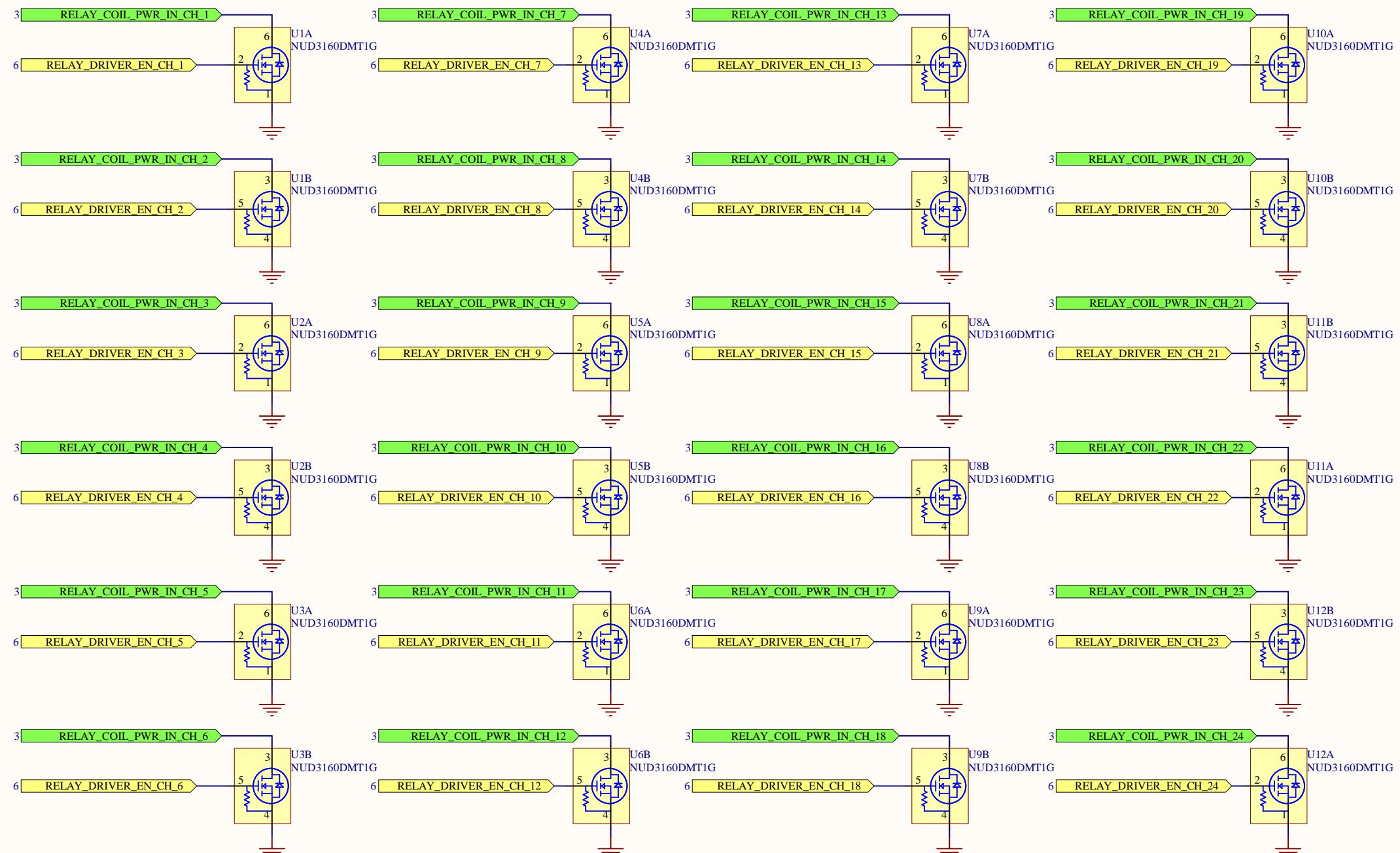
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Relay Drivers

Relay drivers are low-side nFETs which are rated to 60V drain-source. Relay coil outputs are connected to RELAY_COIL_PWR_IN_CH_XY.



Title

Relay Drivers

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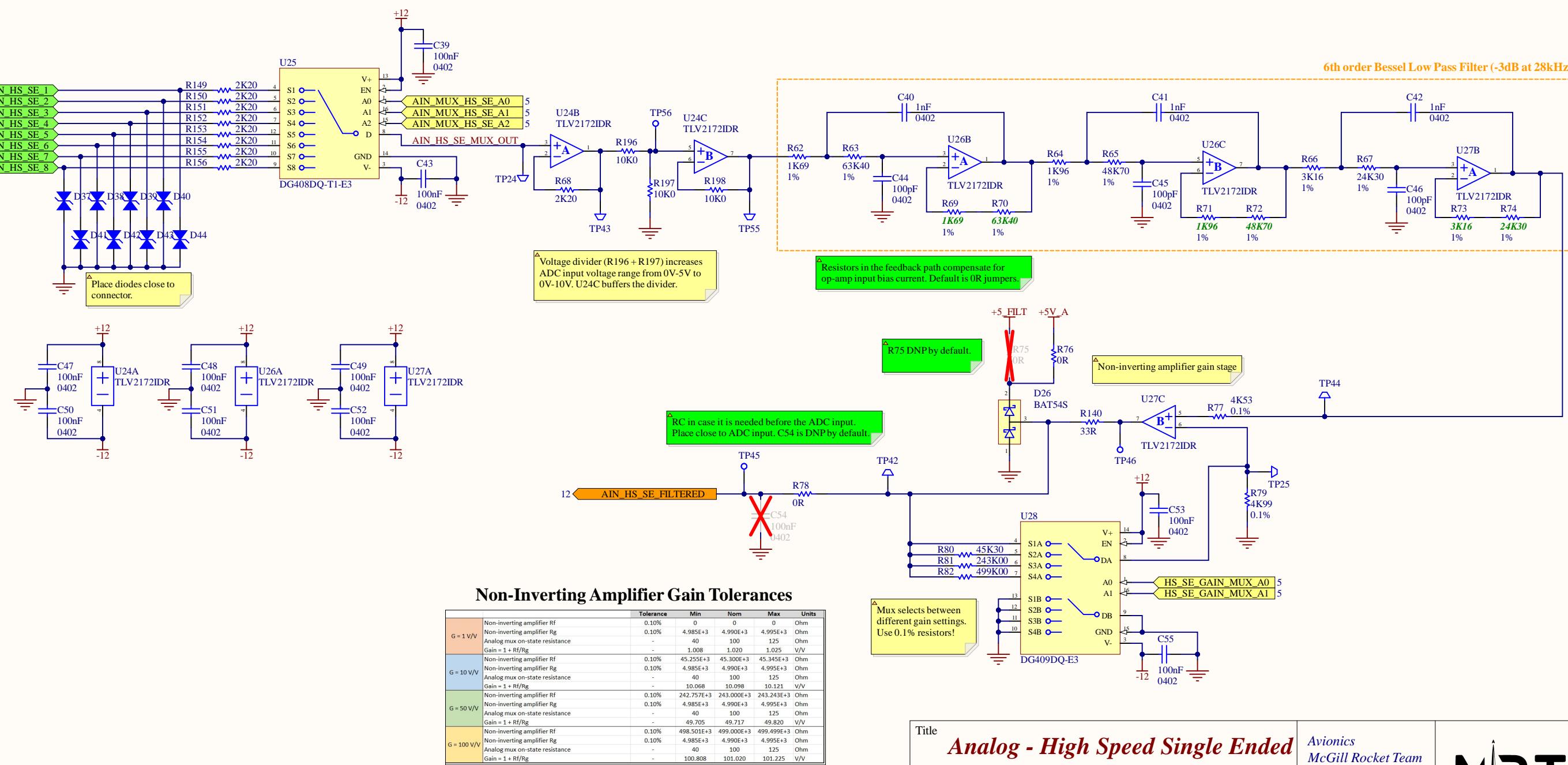
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Analog - High Speed Single Ended



Title: **Analog - High Speed Single Ended**

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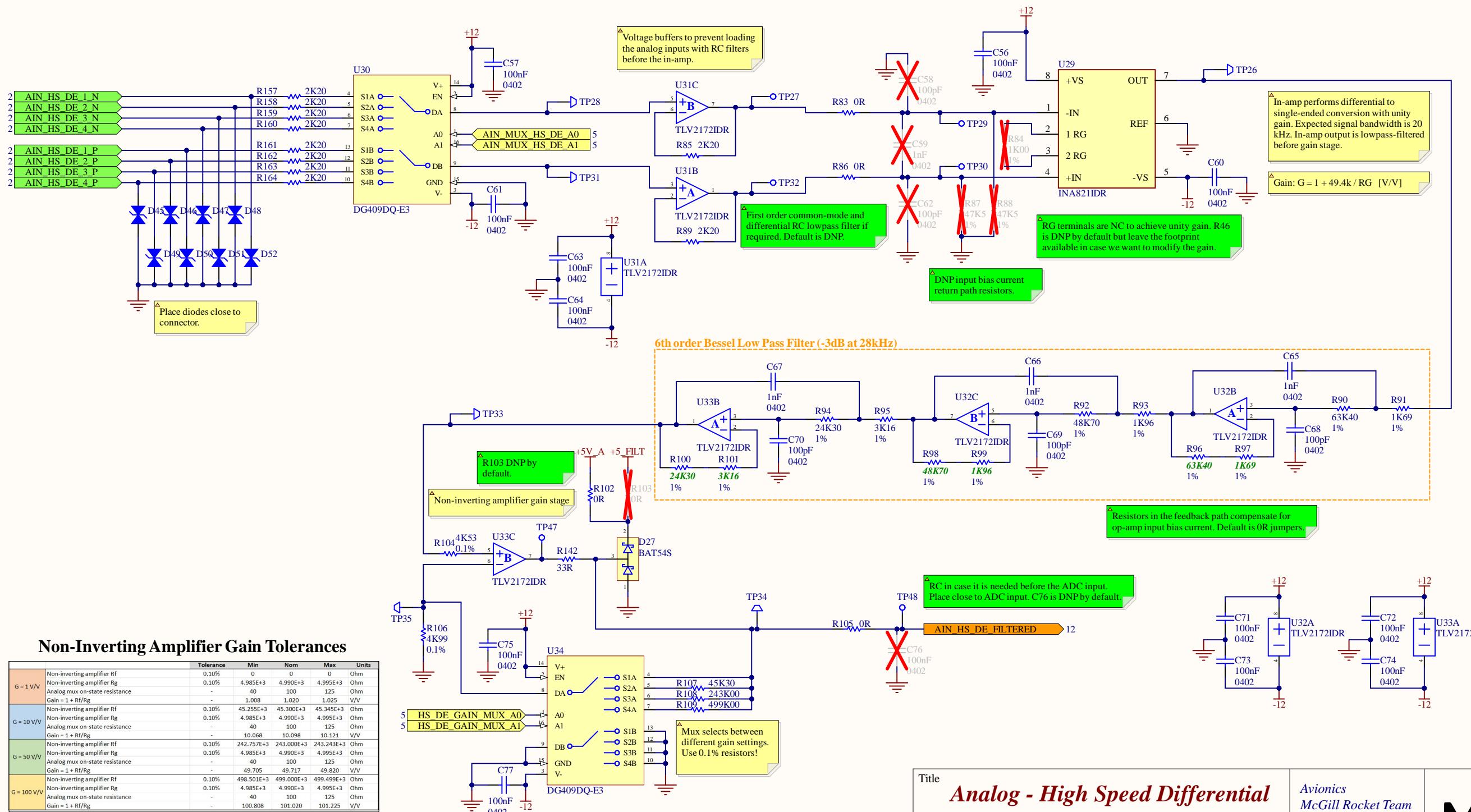
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Analog - High Speed Differential



Title **Analog - High Speed Differential**

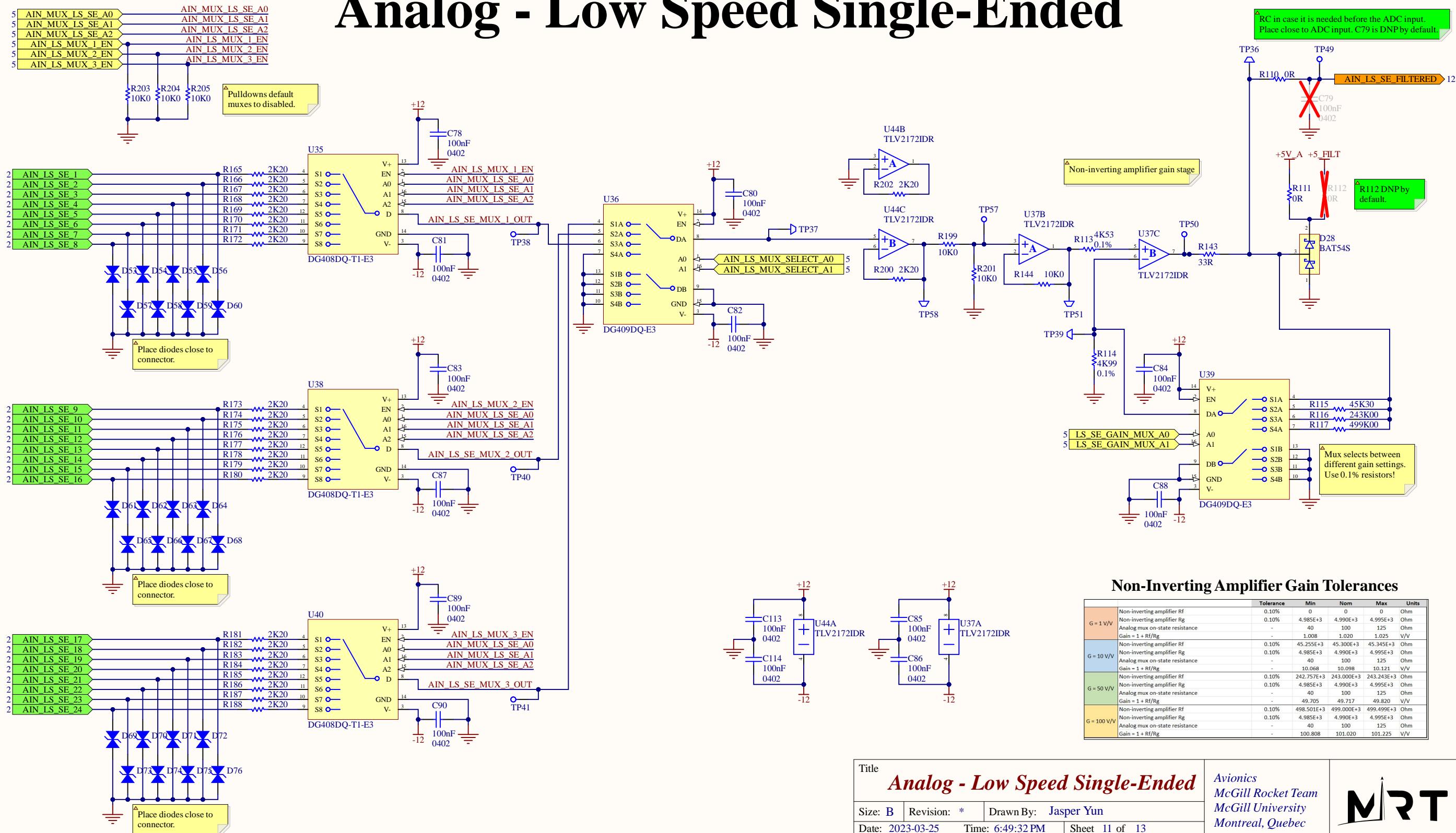
Size: B | Revision: * | Drawn By: Jasper Yun

Date: 2023-03-25 | Time: 6:49:31 PM | Sheet 10 of 13

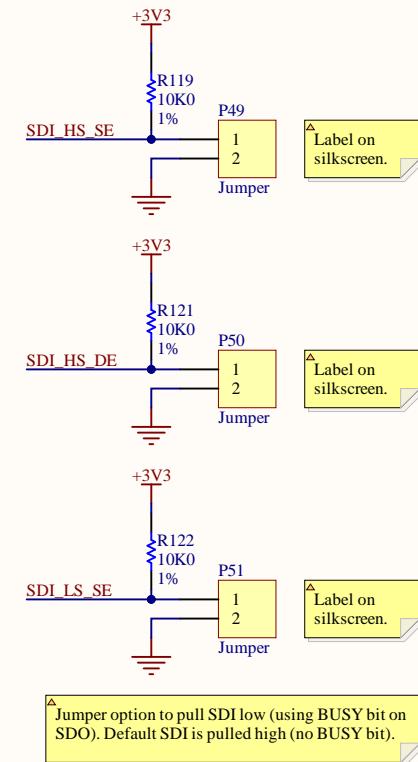
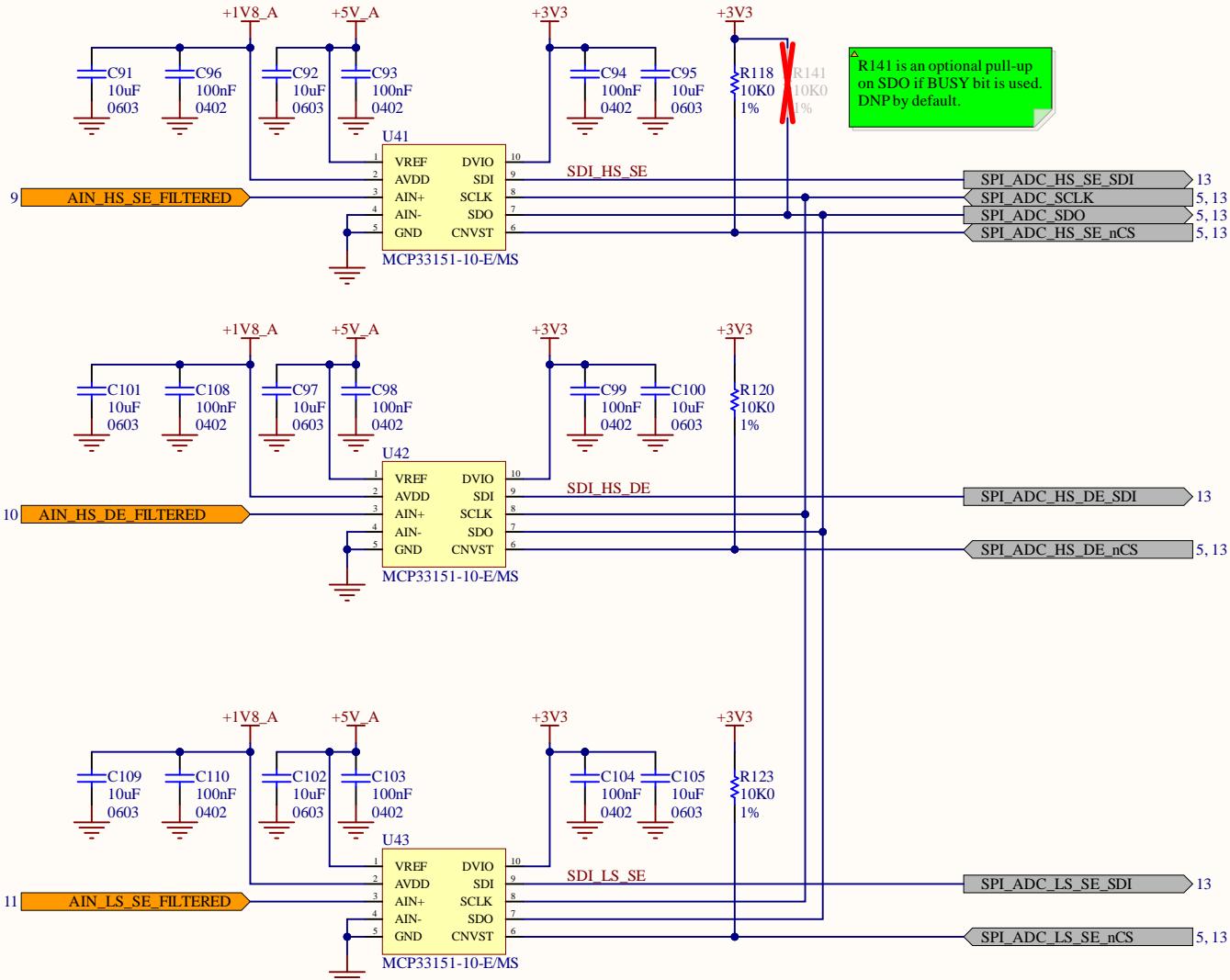
File: C:\Users\jaspe\Desktop\ecse478_honours_thesis\1 Hardware\ECSE478 - DAQ Device\Analog - High Speed DE.SchDoc



Analog - Low Speed Single-Ended



Analog to Digital Conversion



Title

Analog to Digital Conversion

Size: B Revision: * Drawn By: Jasper Yun

Date: 2023-03-25 Time: 6:49:32 PM Sheet 12 of 13

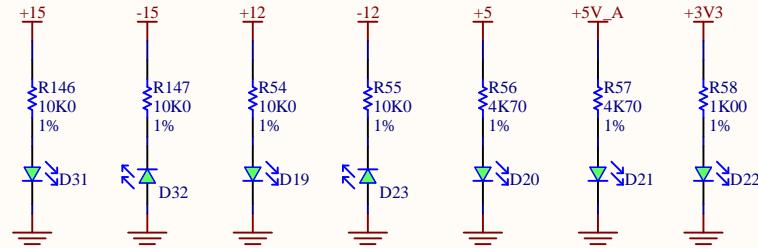
File: C:\Users\jaspe\Desktop\ecse478_honours_thesis\1 Hardware\ECSE478 - DAQ Device\ADC.SchDoc

Avionics
McGill Rocket Team
McGill University
Montreal, Quebec

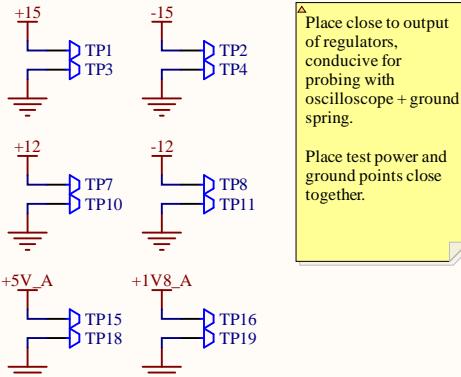


Debug

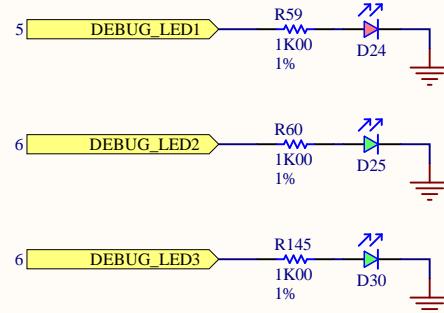
Power LEDs



Power Rails Test Points

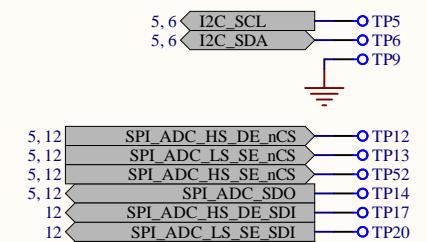


Program Debug LEDs



Analog Test Points

See analog sheets.



SMD test point pads.



A

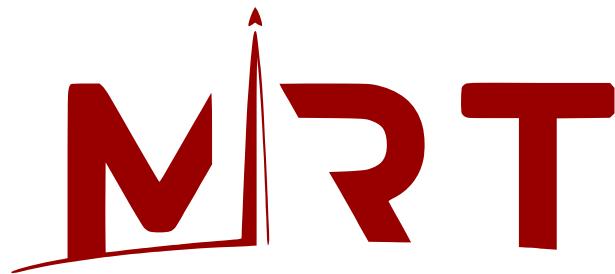
B

C

D

E

DAQ Device



Thickness: 1.6 mm

Width: 11.43cm

Length: 21.15 cm

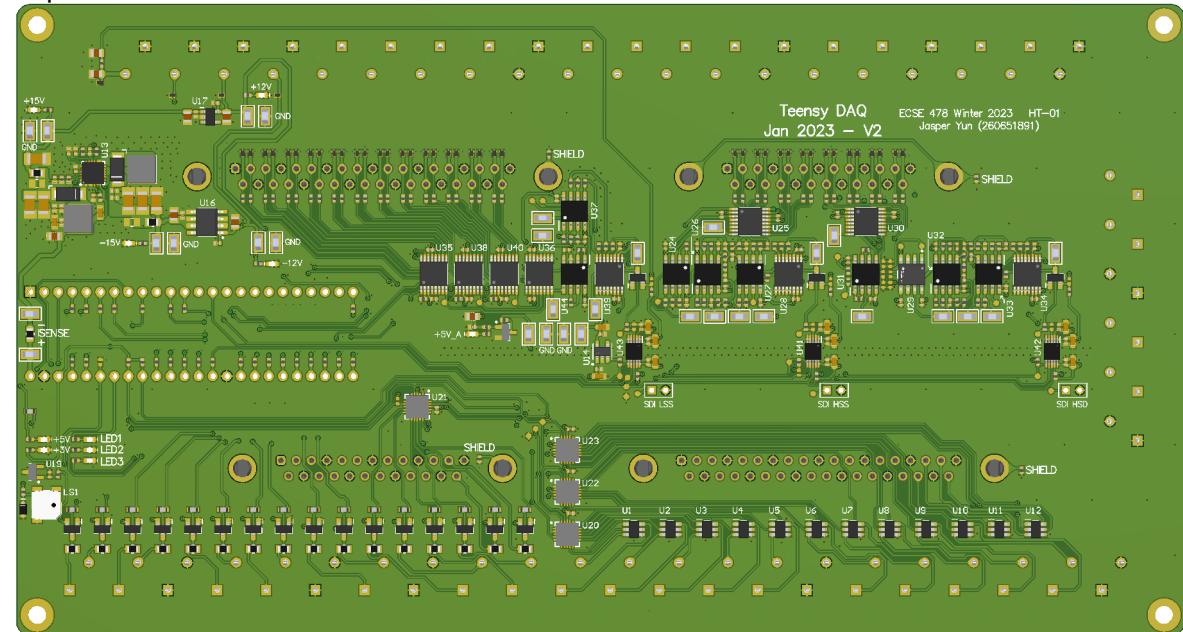
Layers: 4

ECSE 478 (Winter 2023) - HT-01
Jasper Yun (260651891)

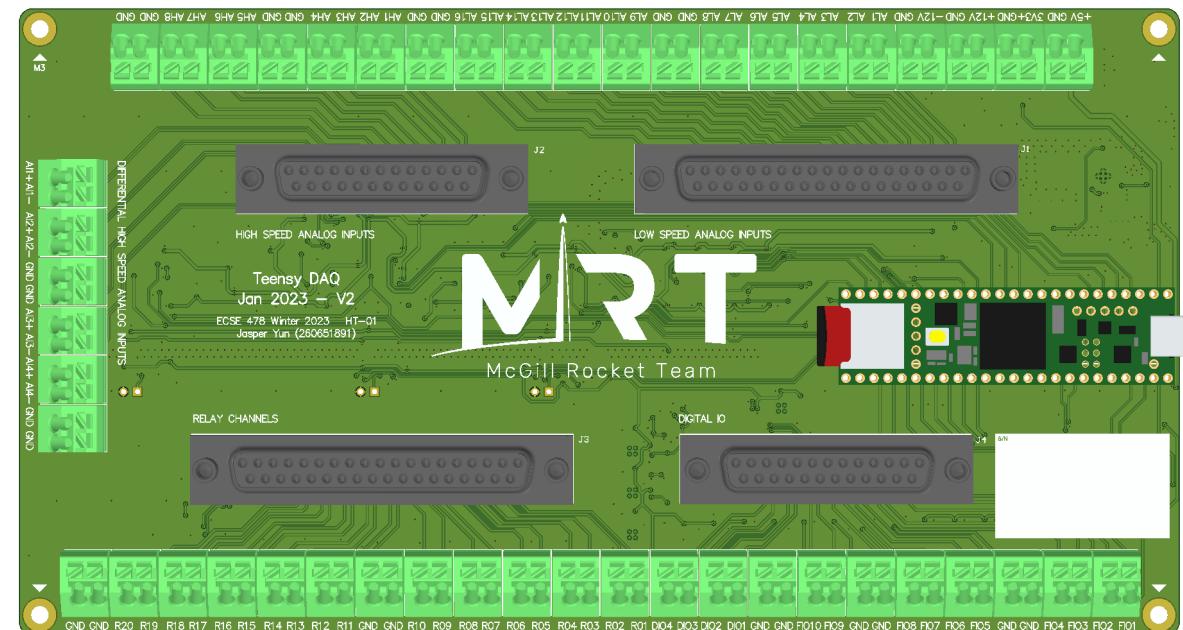
Advisor: Prof. Gordon Roberts

McGill University

Top

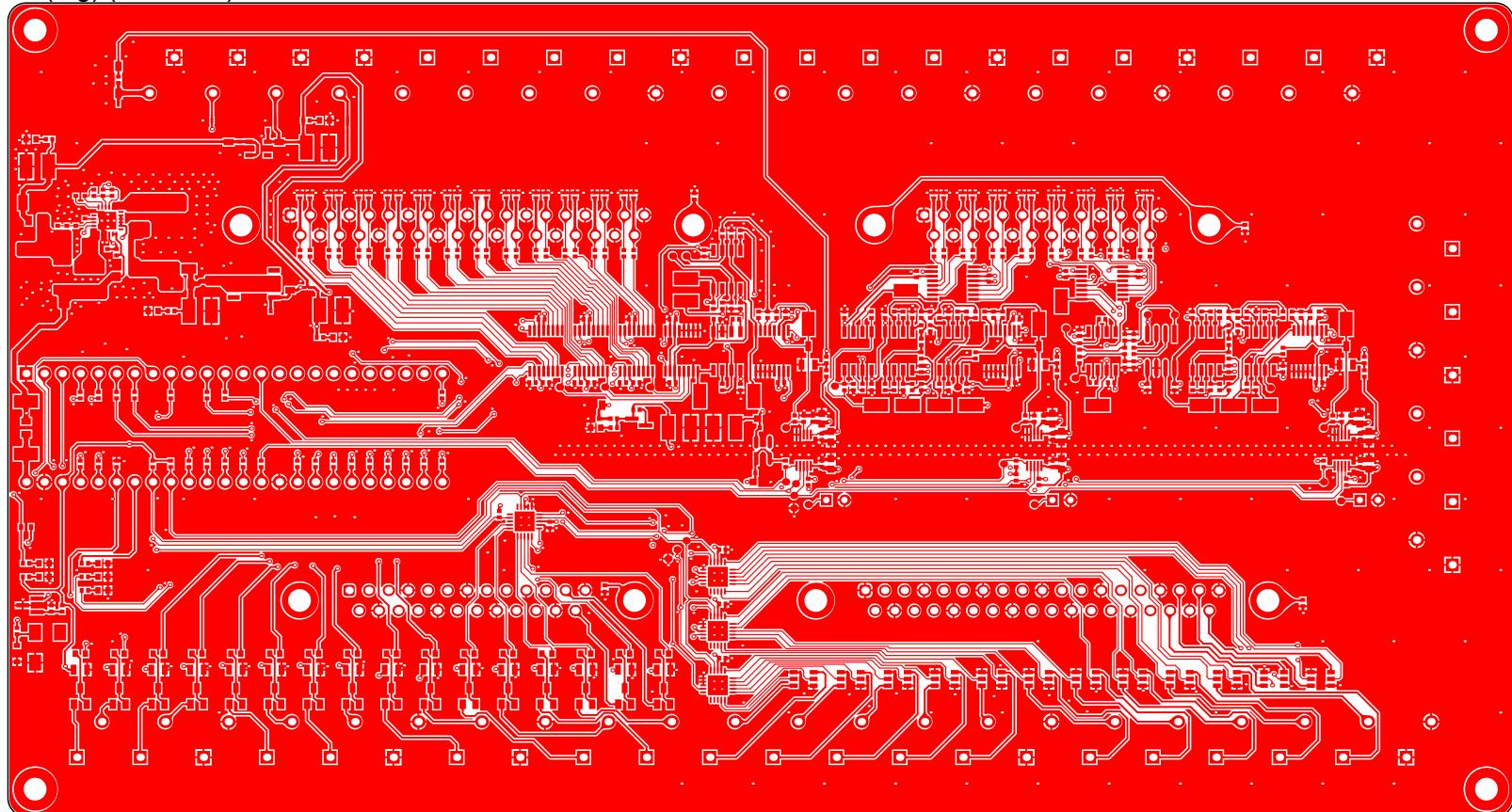


Bottom



Layer 1

L1 (Sig) (Scale 1:1)



A

B

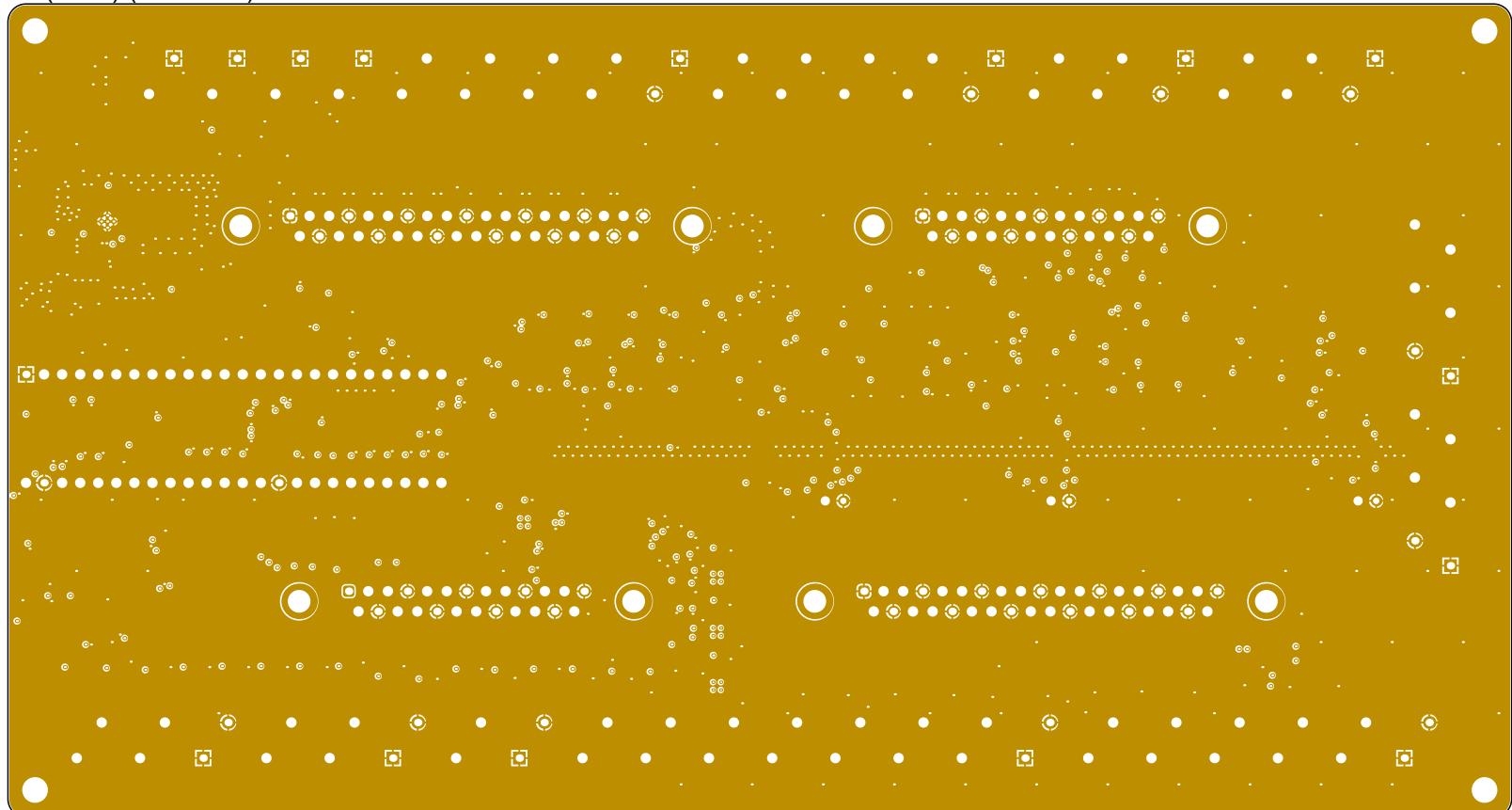
C

D

E

Layer 2

L2 (GND) (Scale 1:1)



1

1

2

2

3

3

4

4

A

B

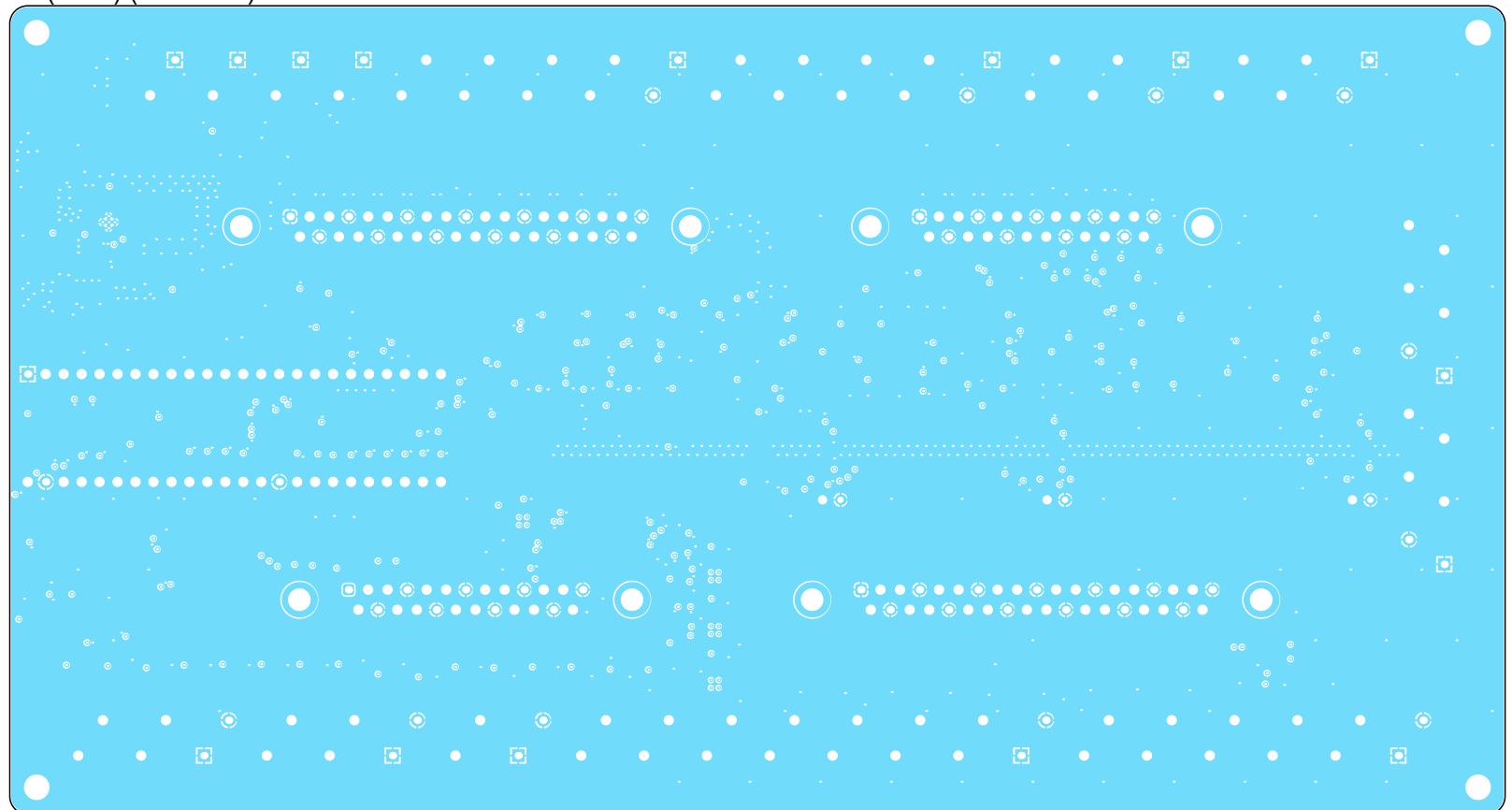
C

D

E

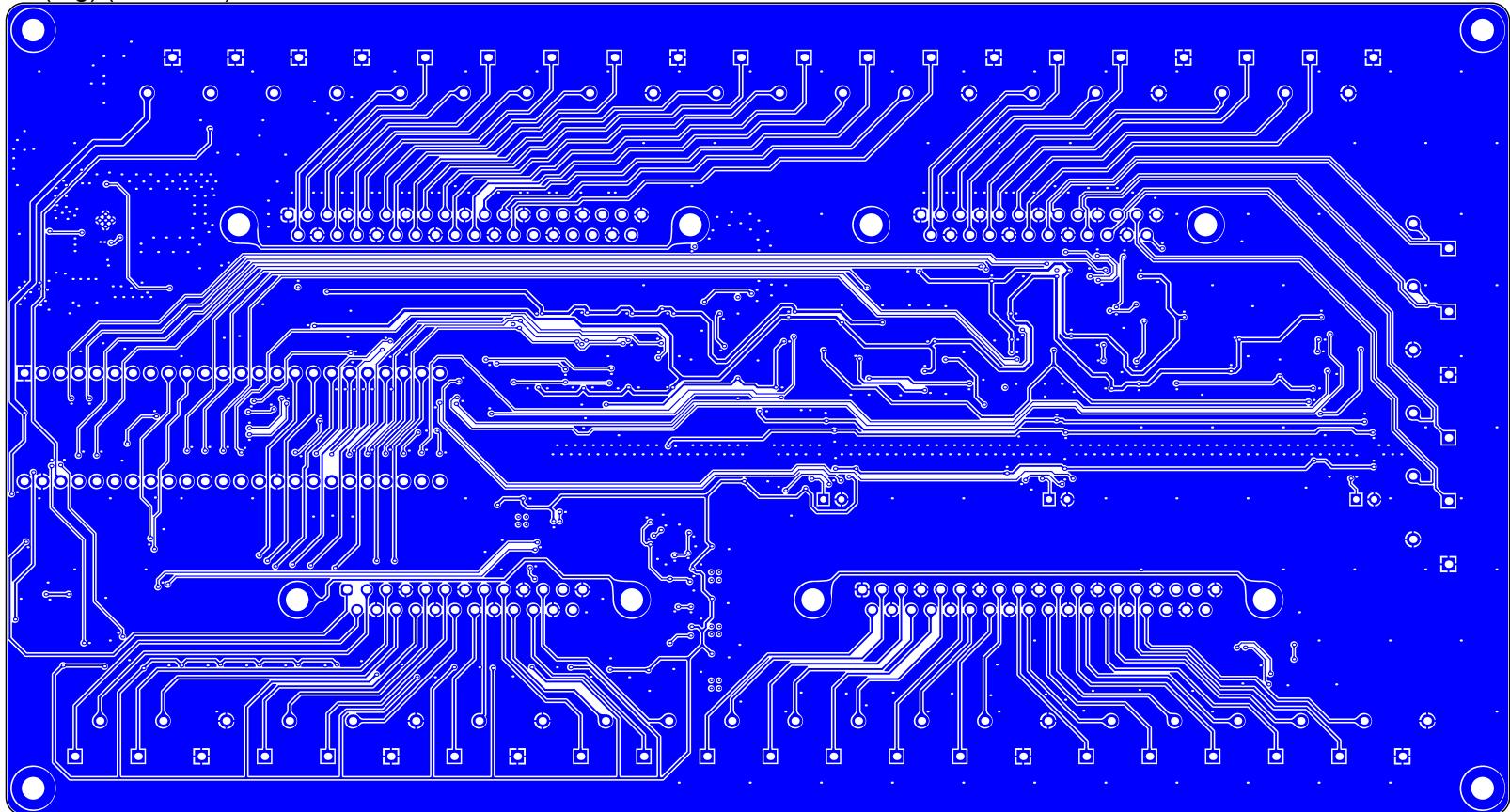
Layer 3

L3 (GND) (Scale 1:1)



Layer 4

L4 (Sig) (Scale 1:1)



Bill of Materials -- DAQ Device

Name	Description	Designator	Quantity	Footprint	Total Cost (CAD)
TLV2172IDR	2-channel, 10-MHz, low-noise, low-distortion audio op amp with high output current 8-SOIC -40 to 85	U24, U26, U27, U31, U32, U33, U37, U44	8	SOIC-8	21.60
4.7uH	4.7uH BWVS005050404R7M00	L1, L2	2	Inductor BWVS005050403R3M00	1.18
MCP23008-E/ML	8-Bit I/O Expander with Serial Interface, 20-Pin QFN, Extended Temperature	U20, U21, U22, U23	4	QFN-ML20_M	8.92
LDK320AM120R	200 mA low quiescent current and high PSRR voltage regulator	U17	1	SOT23-5	1.29
MCP33151-10-E/MS	ADC 14-bit SAR 1Msps 10-MSOP	U41, U42, U43	3	MSOP-10	12.60
D12V0L1B2LP-7B	Bidirectional Zener diode	D33, D34, D35, D36, D37, D38, D39, D40, D41, D42, D43, D44, D45, D46, D47, D48, D49, D50, D51, D52, D53, D54, D55, D56, D57, D58, D59, D60, D61, D62, D63, D64, D65, D66, D67, D68, D69, D70, D71, D72, D73, D74, D75, D76	44	DFN1006-2	12.89
100nF	Capacitor	C1, C2, C9, C12, C15, C16, C18, C19, C26, C28, C29, C31, C32, C34, C35, C36, C37, C38, C39, C43, C47, C48, C49, C50, C51, C52, C53, C55, C56, C57, C60, C61, C63, C64, C71, C72, C73, C74, C75, C77, C78, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C93, C94, C96, C98, C99, C103, C104, C108, C110, C113, C114	63	0402 CAP	2.08
22uF	Capacitor	C3, C4, C5, C20, C21, C22	6	1206 CAP	2.88
13pF	Capacitor	C6, C13	2	0402 CAP	0.20
47uF	Capacitor	C7, C111, C112	3	0805 CAP	2.73
10uF	Capacitor	C8, C11, C14, C17, C91, C92, C95, C97, C100, C101, C102, C105, C109	13	0603 CAP SAMSUNG CL10C	3.15
220nF	Capacitor	C10	1	0402 CAP	0.14
10nF	Capacitor	C23	1	0402 CAP	0.14
4.7nF	Capacitor	C24	1	0402 CAP	0.14
10uF	Capacitor	C25, C27, C30, C106, C107	5	0805 CAP	1.30
1nF	Capacitor	C40, C41, C42, C65, C66, C67	6	0402 CAP	0.20
100pF	Capacitor	C44, C45, C46, C68, C69, C70	6	0402 CAP	0.20

Bill of Materials -- DAQ Device

Name	Description	Designator	Quantity	Footprint	Total Cost (CAD)
SMT-0540-T-9-R	CMT-9648-85T Magnetic buzzer	LS1	1	Buzzer SMT-0540-T-9-R	2.27
LD25S24A4GV00LF	DB25 LD25S24A4GV00LF (Amphenol ICC)	J2, J4	2	Connector DB25 Vertical LD25S24A4GV00LF	5.26
LD37S24A4GV00LF	DB37 LD37S24A4GV00LF (Amphenol ICC)	J1, J3	2	Connector DB37 Vertical LD37S24A4GV00LF	6.98
DG408DQ-T1-E3	DG408DQ-T1-E3; Multiplexer Single 8: 1; 15 V; 18 V; 24 V; 28 V; 16-Pin TSSOP	U25, U35, U38, U40	4	TSSOP-16	19.28
DG409DQ-E3	DG409 Series 20 V 8-Ch/Dual 4-Ch High-Performance CMOS Analog Multiplexer	U28, U30, U34, U36, U39	5	TSSOP-16	30.75
MC79L12ACDR	Fixed Regulator with -14.5 to -27 V Input and -12 V Output, 0 to 125 degC, 8-Pin SOIC (D), Green (RoHS & no Sb/Br)	U16	1	D0008A_M	0.66
LED Green	Generic Green LED	D19, D20, D21, D22, D23, D25, D30, D31, D32	9	0603 LED	0.67
LED Red	Generic Red LED	D24	1	0603 LED	0.15
220R	Generic resistor	R124	1	0402 RES	0.15
CDBA140-HF	Generic Schottky Diode	D1, D2	2	Diode SMA	1.08
B0540WSHE3-TP	Generic Schottky Diode	D29	1	Diode SOD323-F	0.44
1985195	Header, 2-Pin	P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P20, P21, P22, P23, P24, P25, P26, P27, P28, P29, P30, P31, P32, P33, P34, P35, P36, P37, P38, P39, P40, P41, P42, P43, P44, P45, P46, P47, P48	48	Terminal Block 1985195 2-pos 3.5mm pitch	21.94
Jumper	Header, 2-Pin	P49, P50, P51	3	HDR1X2	0.00
NUD3160DMT1G	IC INDUCT LOAD DRVR INDUST SC74-6	U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12	12	SOT23-6	7.55
INA821IDR	IC INST AMP 1 CIRCUIT 8SOIC	U29	1	FP-D0008A-IPC_A	8.98
TPS65131RGER	IC REG BUCK BST INV ADJ DL 24QFN	U13	1	VQFN-24	4.23

Bill of Materials -- DAQ Device

Name	Description	Designator	Quantity	Footprint	Total Cost (CAD)
Test Point - Keystone 5015	Keystone 5015 Test point	TP1, TP2, TP3, TP4, TP7, TP8, TP10, TP11, TP15, TP16, TP18, TP19, TP24, TP25, TP26, TP28, TP31, TP33, TP34, TP35, TP36, TP37, TP39, TP42, TP43, TP44, TP51, TP53, TP54, TP55, TP58	31	Test Point Keystone 5015	15.13
MCP9700T-E/TT	Low-Power Linear Active Thermistor IC, 3-Pin SOT-23, Extended Temperature, Tape and Reel	U19	1	SOT-23-TT3_M	0.43
TLV74118PDBVR	None	U14	1	FP-DBV0005A-IPC_A	0.49
ADR5045BRTZ-REEL7	Precision Micropower Shunt Mode Voltage Reference, 5 V Output, Industrial, 3-pin SOT23 (RT-3), Reel	U15	1	ADI-RT-3_M	2.57
BAT54S	Rectifier Diode Small Signal Schottky 40V 0.3A 5ns 3-Pin SOT-23 T/R	D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D26, D27, D28	19	SOT23-3	5.19
15R	Resistor	R1, R8	2	0805 RES	0.30
536K0	Resistor	R3	1	0402 RES	0.15
47K50	Resistor	R4, R5	2	0402 RES	0.30
100R	Resistor	R6, R148	2	0402 RES	0.30
576K00	Resistor	R7	1	0402 RES	0.15
4K22	Resistor	R10	1	0402 RES	0.15
0R	Resistor	R11, R18, R76, R78, R83, R86, R102, R105, R110, R111, R191, R192, R193, R194	14	0402 RES	2.10
33R	Resistor	R12, R13, R14, R15, R16, R17, R125, R126, R127, R128, R129, R130, R131, R132, R133, R134, R135, R136, R137, R138, R139, R140, R142, R143, R189	25	0402 RES	3.75
2K55	Resistor	R19, R20	2	0402 RES	0.30
220R	Resistor	R21	1	0402 RES	0.15
10K0	Resistor	R54, R55, R118, R119, R120, R121, R122, R123, R144, R146, R147, R190, R196, R197, R198, R199, R201, R203, R204, R205	20	0402 RES	3.00
4K70	Resistor	R56, R57	2	0402 RES	0.30

Bill of Materials -- DAQ Device

Name	Description	Designator	Quantity	Footprint	Total Cost (CAD)
1K00	Resistor	R58, R59, R60, R145	4	0402 RES	0.60
1K69	Resistor	R62, R69, R91, R97	4	0402 RES	0.60
63K40	Resistor	R63, R70, R90, R96	4	0402 RES	0.60
1K96	Resistor	R64, R71, R93, R99	4	0402 RES	0.60
48K70	Resistor	R65, R72, R92, R98	4	0402 RES	0.60
3K16	Resistor	R66, R73, R95, R101	4	0402 RES	0.60
24K30	Resistor	R67, R74, R94, R100	4	0402 RES	0.60
		R68, R85, R89, R149, R150, R151, R152, R153, R154, R155, R156, R157, R158, R159, R160, R161, R162, R163, R164, R165, R166, R167, R168, R169, R170, R171, R172, R173, R174, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188,			
2K20	Resistor	R200, R202	45	0402 RES	6.75
4K53	Resistor	R77, R104, R113	3	0402 RES	1.71
4K99	Resistor	R79, R106, R114	3	0402 RES	1.71
45K30	Resistor	R80, R107, R115	3	0402 RES	1.71
243K00	Resistor	R81, R108, R116	3	0402 RES	1.98
499K00	Resistor	R82, R109, R117	3	0402 RES	1.12
0R020	Resistor	R195	1	0805 RES	0.60
470R	Resistor	R22, R23, R24, R25, R30, R31, R32, R36, R37, R38, R42, R43, R44, R48, R49, R50	16	0805 RES	2.40
10R	Resistor	R26, R27, R28, R29, R33, R34, R35, R39, R40, R41, R45, R46, R47, R51, R52, R53	16	0603 RES	2.40
Teensy 4.1	Teensy 4.1	U18	1	Teensy 4.1	59.93
PTS060315V005	Thermal Fuse	F1	1	Fuse Thermal 0603 PTS060315V005	0.26
				components total (CAD)	301.56

Components pricing data from Digi-Key as of March 25, 2023

Quantities were either exact from BOM or rounded up to satisfy volume discount (e.g. order 10 instead of 7)

PCBs cost (5 boards) (CAD) 62.75

PCB cost per board (CAD) 12.55

PCBs quoted from JLCPCB on March 25, 2023, prices converted from USD to CAD

final total (CAD) 314.11

DAQ Device Power Rail Checking

Rail Voltage (V) Without Teensy on board, power from KORAD KA3005D

+15	14.533
-15	-14.220
+12	11.958
-12	-12.214
+5V_A	4.985

1V8_A -- Teensy not populated, no 3v3 available

current consumption: around 1.1A -- there must be a hardware problem somewhere

Hot components

U27

U37

fixed by changing 33r on output of gain stage to 10k because I don't have many 100R

repeat sans teensy after changing 33R to 10k

Rail Voltage (V) Ripple (mVpp) Ripple Freq (kHz)

+15	14.485	76.8	22.73
-15	-14.183	64.8	21.28
+12	11.969	6.8	21.28 approx, hard to tell
-12	-12.267	4.4	n/a
+5V_A	5.000	10.6	3.247 approx, hard to tell
1V8_A	1.8011	7 n/a	measured after by adding Teensy so above measurements of rails may be invalid

current consumption: 0.201A

will need to redo test when power comes from USB because USB is noisier

with Teensy: current = 268mA (blinky program default)

5V usb 5.112 146 22.73 powered by xps13, with charger plugged in

High-Speed Single-Ended Analog Input Anti-Aliasing Filter Magnitude Response

Input is a sinusoid from signal generator to AH1 (2.00v offset, 2.00vpp)

Input+ sinusoid (1Vpp) (remember there is a 10k+10k v div on input)

Hardware output sinusoid

In+ Freq (Hz)	Filter In mean (oscope) (V)	Input Vpp (V)	Output mean (V)	Output freq (Hz)	Output Vpp (V)	Output / Input (V/V)	Output / Input (dB)	LTS spice sim results	
								Freq (Hz)	Mag (dB)
10		1	1.04	0.964	10	1.04	1	10	0
20		1	1.02	0.964	20	1.02	1	20	0
50		1	1.04	0.964	20	1.04	1	50	0
100		1	1.04	0.964	100	1.06	1.019230769	100	0
200		1	1.02	0.966	199.98	1.06	1.039215686	200	-0.001
500	0.994	1.03	0.98	499.99	1.06	1.029126214	0.249372811	500	-0.004
1000	0.996	1.04	0.98	1000	1.09	1.048076923	0.407863173	1000	-0.016
2000	0.996	1.04	0.98	2000	1.13	1.086538462	0.720902084	2000	-0.039
5000	0.996	1.04	0.98	5000	1.18	1.134615385	1.09697336	5000	-0.576
10000	0.994	1.02	0.988	10000	1.14	1.117647059	0.966093591	10000	-0.883
12000	0.997	1.02	0.974	12000	1.12	1.098039216	0.812357018	12000	-1.556
15000	0.997	1.02	0.974	15000	1.08	1.058823529	0.496471675	15000	-2.413
20000	0.994	1.02	0.988	20000	1	0.980392157	-0.172003435	20000	-3.467
22000	0.996	1.02	0.976	22000	0.968	0.949019608	-0.454496289	22000	-4.517
25000	0.995	1.02	0.988	25000	0.912	0.894117647	-0.972106669	25000	-5.575
28000	0.993	1.02	0.995		0.856	0.839215686	-1.522528142	28000	-6.633
30000	0.998	1.02	0.978	30000	0.808	0.792156863	-2.02377622	30000	-7.691
50000	0.995	1.02	0.988	50000	0.424	0.415686275	-7.624686303	50000	-10.2
75000	0.997	1.02	0.99	75000	0.12	0.117647059	-18.58837851	75000	-22.903
100000	0.995	1.02 x		100000	0.0304	0.029803922	-30.51453176	100000	-36.157
150000	0.996	1.02 x			0.0052	0.005098039	-45.85193656	150000	-54.75
200000	0.993	1.02 x			0.0036	0.003529412	-49.04595342	200000	-68.852

both inputs bw-lim to 20MHz

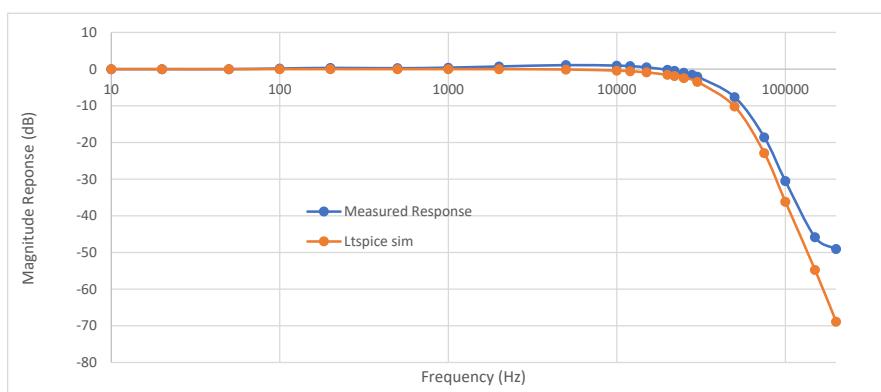
10x probes

acquisition in averaging (1024 samples)

input on TP55

output on TP44

designators according to rev 1



High-Speed Single-Ended Analog Input Full Signal Chain Tests

Input at term block, output at TP42 (output of gain stage)

Goal is to measure gain and offset of full signal chain

oscilloscope: Siglent SDS 1202x-e

10x inputs, DC coupled, averaging 1024 samples, input sine wave at 1kHz for all tests

Note: this test done after full chain test (on left) but same setup, same day, same sig gen settings

Test op amp gain stage only -- input probe on op amp input TP44, output probe on TP42

G = 1V/V config

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	Gain (V/V)
2	0.72	0.97071	0.38	0.527777778
2	1.02	0.97033	0.54	0.529411765
1.97	2.5	0.95638	1.32	0.528
2.51	0.7	1.23	0.38	0.542857143
2.51	1.02	1.23	0.54	0.529411765
2.49	2.5	1.22	1.32	0.528

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	Gain (V/V)
1	0.368	0.98664	0.376	Gain (V/V)
1	0.528	0.98625	0.536	Gain (V/V)
0.99352	1.24	0.95822	1.32	Gain (V/V)
1.25	0.352	1.24	0.368	1.045454545
1.25	0.512	1.24	0.544	1.0625
1.25	1.26	1.22	1.32	1.047619048
		average		1.051857864

G = 10V/V config

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	Gain (V/V)
0.09035	0.132	0.42598	0.696	5.272727273
0.09075	0.104	0.42873	0.528	5.076923077
0.08787	0.076	0.43067	0.384	5.052631579
0.17921	0.134	0.88767	0.696	5.194029851
0.17971	0.104	0.89071	0.536	5.153846154
0.18001	0.074	0.89244	0.384	5.189189189

G = 10V/V config

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	PP gain (V)
0.04296	0.0672	0.43685	0.688	10.23809524 changed input probe to 1x to reduce noise
0.04324	0.052	0.43917	0.536	10.30769231
0.04337	0.0376	0.44074	0.384	10.21276596
0.07987	0.068	0.80074	0.68	10
0.08021	0.052	0.80345	0.54	10.38461538
0.08027	0.038	0.80585	0.38	10
		average		10.19052815

G = 50V/V config

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	Gain (V/V)
0.08907	0.124	2.18	3.16	25.48387097
0.08987	0.104	2.2	2.64	25.38461538
0.09027	0.084	2.21	2.12	25.23809524
0.12665	0.126	3.1	3.16	25.07936508
0.12709	0.104	3.11	2.64	25.38461538
0.12778	0.084	3.12	2.16	25.71428571

G = 50V/V config

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	PP gain (V)
0.04329	0.062	2.21	3.08	49.67741935
0.04343	0.052	2.23	2.56	49.23076923
0.04367	0.042	2.24	2.08	49.52380952
0.06166	0.062	3.11	3.12	50.32258065
0.06192	0.052	3.12	2.56	49.23076923
0.06202	0.042	3.13	2.08	49.52380952
		average		49.58485958

G = 100V/V config

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	Gain (V/V)
0.06148	0.084	3.11	4.28	50.95238095
0.06211	0.0528	3.14	2.68	50.75757576
0.06172	0.0232	3.13	1.08	46.55172414
0.04289	0.0848	2.18	4.28	50.47169811
0.04342	0.0536	2.2	2.68	50
0.04321	0.0224	2.19	1.08	48.21428571

G = 100V/V config

Input mean (V)	Input Vpp (V)	Output mean (V)	Output Vpp (V)	PP gain (V)
0.03019	0.0424	3.13	4.28	100.9433962
0.03024	0.0266	3.15	2.64	99.2481203 very noisy input
0.03034	0.011	3.14	1.1	100
0.02071	0.0424	2.17	4.28	100.9433962
0.02099	0.0268	2.2	2.64	98.50746269 very noisy input
0.0211	0.01096	2.19	1.08	98.54014599
		average		99.6970869