```
1   LIBRARY IEEE;
2   USE IEEE.std_logic_1164.ALL;
3   USE WORK.ALL;
4   ENTITY state_machine3_test IS
5   END state_machine3_test;
6   ARCHITECTURE state_machine3_test_bench OF state_machine3_test
    IS
7       COMPONENT state_machine3
8       PORT(x0, x1 : IN std_logic;
9       clock : IN std_logic;
10      reset : IN std_logic;
11      y0, y1 : OUT std_logic);
12      END COMPONENT;
13      SIGNAL clock, reset, x0, x1, y0, y1 : std_logic;
14  BEGIN
15      sm1: state_machine3 PORT MAP(x0 => x0, x1 => x1, clock =>
    clock, reset => reset, y0 => y0, y1 => y1);
16      PROCESS
17      BEGIN
18          clock <= '0';
19          WAIT FOR 50 ns;
20          clock <= '1';
21          WAIT FOR 50 ns;
22      END PROCESS;
23      PROCESS
24      BEGIN
25          reset <= '1';
26          WAIT FOR 25 ns;
27          reset <= '0';
28          WAIT;
29      END PROCESS;
30
31      process
32      begin
33          x0 <= '0'; x1 <= '0';
34          wait for 75 ns;
35          x0 <= '0'; x1 <= '1';
36          wait for 100 ns;
37          x0 <= '0'; x1 <= '0';
38          wait for 100 ns;
39          x0 <= '1'; x1 <= '0';
40          wait for 100 ns;
41          x0 <= '0'; x1 <= '1';
42          wait for 100 ns;
43          x0 <= '1'; x1 <= '1';
44          wait for 100 ns;
45          x0 <= '1'; x1 <= '1';
46          wait for 100 ns;
47          x0 <= '1'; x1 <= '0';
48          wait for 100 ns;
49          x0 <= '0'; x1 <= '1';
50          wait for 100 ns;
51          wait;
52      end process;
53  END state_machine3_test_bench;
54
55  CONFIGURATION state_machine3_test_conf OF state_machine3_test
    IS
56      FOR state_machine3_test_bench
57      END for;
58  END state_machine3_test_conf;
59
```