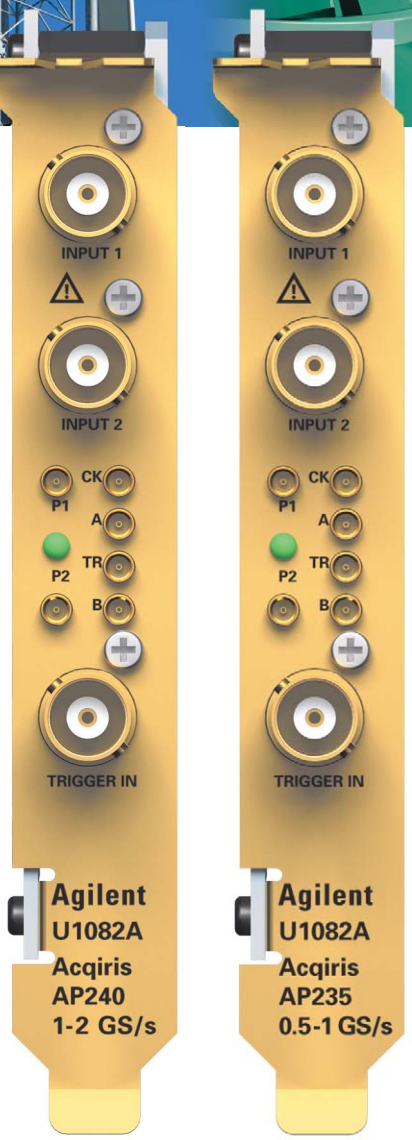
Agilent U1082A

Acqiris High-Speed PCI Data Converters
AP240: 8-bit, 2 ch, 1 GHz, 1-2 GS/s
AP235: 8-bit, 2 ch, 500 MHz, 0.5-1 GS/s

with Firmware for Sustained Sequence Recording, Averaging, or Peak Analysis

Agilent Technologies



Ctrl I/O

Main Features

- Up to 2 GS/s sampling rate
- Dual- and single-channel modes
- On-board reconfigurable FPGA for real-time data processing
- Three firmware options that maximize measurement throughput
- Fully-featured, 50 Ω, front-end mezzanine with up to 1 GHz analog bandwidth, internal calibration, and input protection
- Multi-purpose I/O connectors for trigger, clock, reference, and control signals
- Device drivers for Windows®, VxWorks, LabViewRT, and Linux, with application code examples for MATLAB®, C/C++, Visual Basic, LabVIEW, and LabWindows/CVI

Acqiris High-Speed Data Converters

The proprietary ADC chipsets in Agilent Technologies Acqiris high-speed digitizers are designed for the specific purpose of optimizing high-speed ADC performance. The analog front-end technology provides signal conditioning, amplification, and interleaving functions essential for achieving high-speed data acquisition at GS/s rates. The digital data handling components provide vital clock and synchronization signals to capture and memorize acquired data with maximum data throughput. Together these ASICS make low-power, high-fidelity data acquisition much more accessible and provide maximum data throughput to the host PC or processor to reduce the time and cost of measurement.

The Acqiris product line provides a range of high-speed digitizer cards[1] with 8-, 10-, and 12-bit resolution, wide bandwidth, and large acquisition memory. These products, in PCI, PXI, cPCI, and VME formats, are used in research, and in ATE and OEM applications in industries such as biotechnology, semiconductors, aerospace, physics, and astronomy.

High-Speed Digitizers with Real-Time Analysis

The Agilent Acqiris U1082A high-speed data converters are dual-channel, 8-bit PCI digitizer cards with an on-board, high-speed, field programmable gate array component for real-time data processing tasks. The FPGA offers the following features:

- More than 28,672 logic cells
- Up to 1.7 Mbits of on-board RAM
- 96 dedicated 18-bit x 18-bit multipliers with 36-bit results
- Ability to execute multiplications in less than 8.5 ns

Agilent firmware options can be used to implement on-the-fly data processing algorithms. These options allow the analyzer platforms to perform specific post-processing tasks, and are easily uploaded into the FPGA under program control.

The firmware options redefine the way in which data acquisition can be performed. They make the analyzer platforms extremely flexible and easy to reconfigure. A variety of on-board signal processing tasks can be performed on the digitized data.

Dual-Channel Performance and Front-Panel Processing Control

Based on high-performance digitizers, the U1082A signal analyzer platform benefits from full front-end signal conditioning (with calibrated gain and offset ranges), and delivers genuine synchronous dual-channel data acquisition and analysis in a compact card that plugs directly into a desktop PC.

Two front-panel digital I/O connectors for real-time processing control are available to easily interact with the on-board FPGA dedicated to real-time signal processing.

The U1082A-001 model represents the top of the range. Each channel has a front end with 1 GHz bandwidth, 1 GS/s ADC, and a standard 6 MB memory (optional 24 MB). Alternatively, the U1082A-002 platform offers a more cost-effective solution for lower-frequency applications. The unit's front-end bandwidth is 500 MHz and it has a sampling rate up to 500 MS/s on each channel. For single-channel applications both platforms can interleave their two channels, doubling the available memory and maximum sampling rate up to 1 GS/s (U1082A-002) or 2 GS/s (U1082A-001) while improving overall timing resolution.

Easily Integrated

Agilent Acqiris high-speed digitizers are supplied with software drivers for Windows, Linux, LabVIEW RT and VxWorks, and application code examples for MATLAB, C/C++, VisualBasic, LabVIEW, and LabWindows/CVI. These code examples provide digitizer setup and basic acquisition functionality, and are easily modified, so that the card can be quickly integrated into a measurement system. The flexibility of the driver means that, with minimum software adjustments, any Agilent Acqiris digitizer can be swapped out, replaced, or upgraded with the latest high-speed Agilent Acqiris digitizer.

1) 500 MS/s, 1 GS/s, 2 GS/s, 4 GS/s and 8 GS/s high-speed digitizer cards

High-Speed Digitizer with On-Board Signal Processing

GHz BW front end with 50 mV – 5 V FS
The platforms' channel inputs have programmable front-end electronics with a complete set of input voltage ranging from 50 mV to 5 V and variable voltage offset. The 50 Ω input impedance front-end is fully protected against overvoltage signals. The amplifiers feature internal calibration (no need to disconnect input signals) and very fast recovery from out-of-range signals. The input buffer and amplifier are mounted on a removable mezzanine card so that, in the event of accidental damage or as components fatigue over time (e.g., relays in high-duty-cycle automated testing applications), replacement is fast and efficient.

Dual-channel performance with interleave
Dual-channel synchronicity for I/Q acquisitions with up to 1 GS/s sample rate (up to 500 MS/s with the U1082A-002). Interleaved, single-channel mode with up to 2 GS/s sample rate on either input; software selectable (up to 1 GS/s with the U1082A-002).

Real-time FPGA control
Two front-panel digital I/O MMCX-type connectors (I/O P1 and P2) are dedicated to the direct control of the FPGA. For example, with averager firmware installed, one of the front-panel digital lines can be used to choose between the average add and subtract functions. This is an aid when performing automatic baseline subtraction.

Multipurpose I/O ports

Ctrl I/O

Control over the trigger and time base is made even more flexible by the addition of high-density, high-frequency, front-panel connectors. The four MMCX-type front-panel connectors can support an external clock (up to 2 GHz for the U1082A-001 and 1 GHz for the U1082A-002) or reference signal (10 MHz), a trigger output, and two additional I/O digital control lines (I/O A and B). The latter can be used for monitoring or modifying the platforms' status and configuration.
Examples of the controls available are trigger gating and acquisition states. Furthermore, the I/O outputs can be used as a 10 MHz, built-in source for autonomous board test purposes.

Precision time base
The crystal-controlled precision time base drives the data conversion on both channels. Sample rates can be selected in a 1, 2, 2.5, 4, 5 sequence, from 100 MS/s to 2 GS/s (1 GS/s with the U1082A-002). The sample rate can also be generated externally, using the dedicated MMCX CLK IN connector for applications where the sample rate must be synchronized with the device generating the signal.

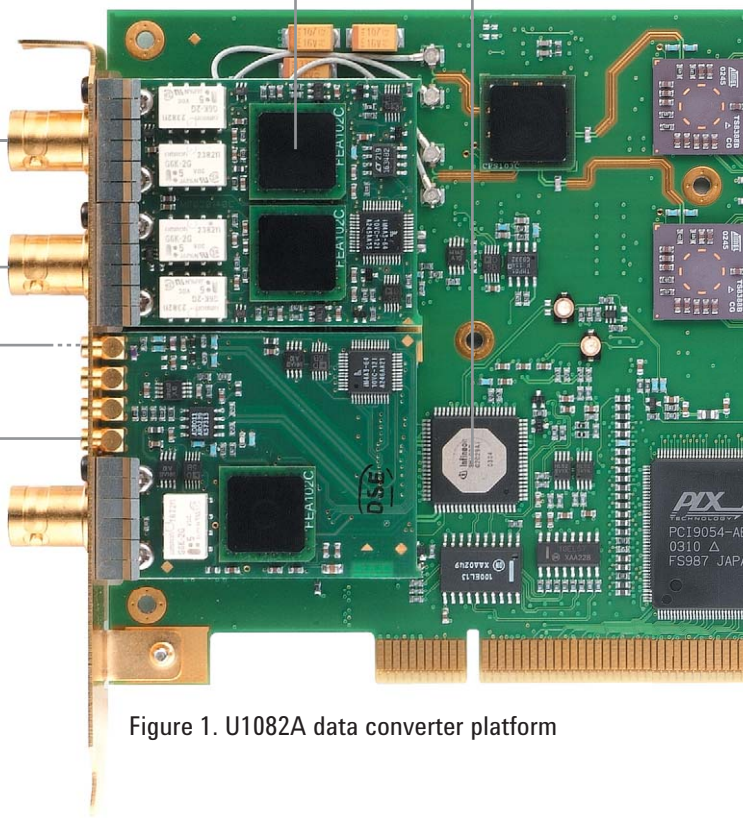
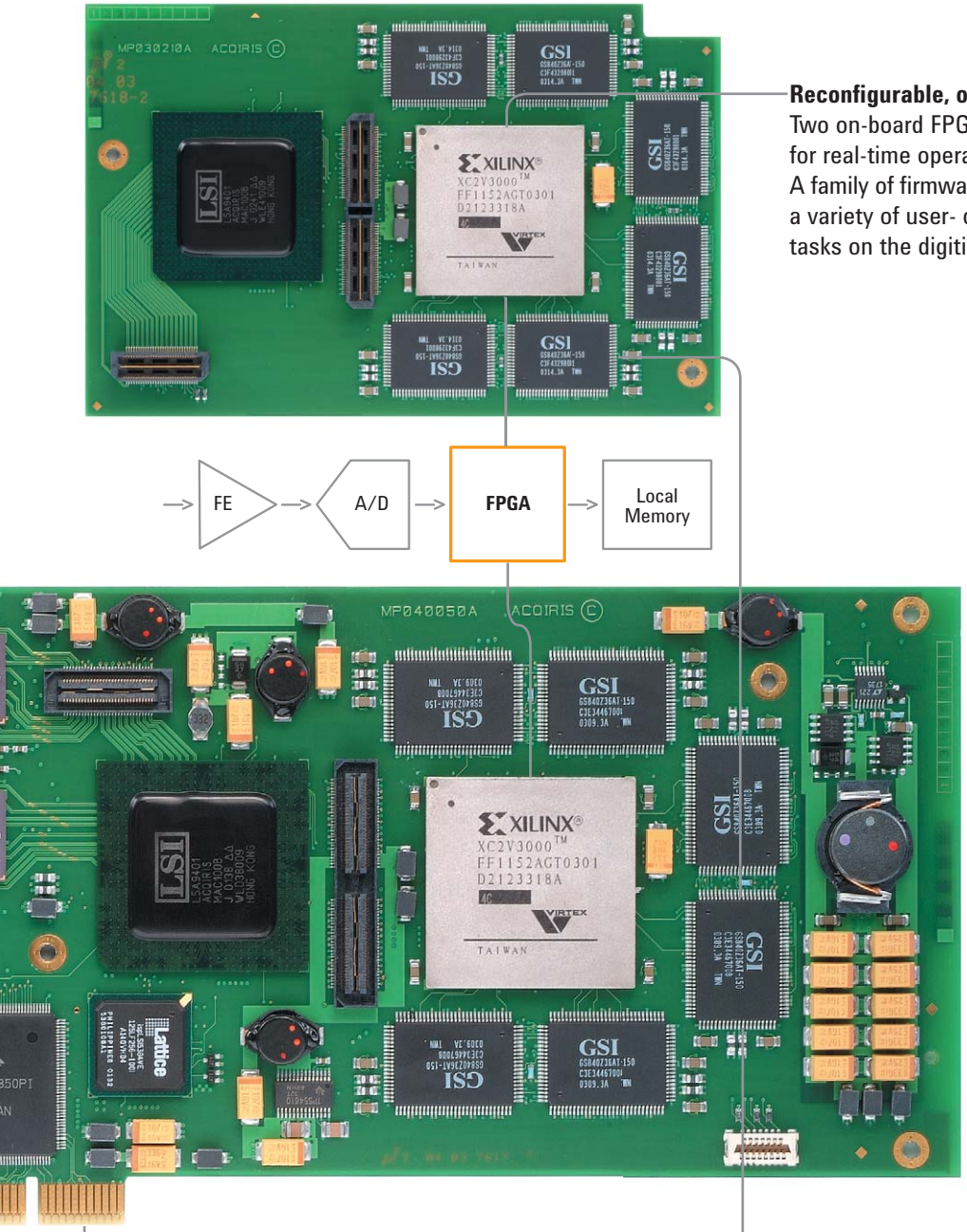


Figure 1. U1082A data converter platform



Reconfigurable, on-the-fly processing
Two on-board FPGA's (Xilinx Virtex-2®) are reconfigurable for real-time operations.
A family of firmware options enables the platform to perform a variety of user- or factory-defined on-the-fly processing tasks on the digitized data.

High data throughput
The analyzer platforms can be easily integrated into any standard PC with one long PCI slot. The platforms are designed to take advantage of the high-speed PCI bus connection. Processed digitized data can be transferred, in DMA mode, directly to the host PC over the bus at sustained rates of up to 100 MB/s.

Large processing memory
Standard processing memory, 6 MB/ch or long processing memory (optional), 24 MB/ch.

Virtex-2 is U.S. registered trademark of Xilinx Inc.

Acqiris High-Speed PCI Data Converter Platforms

Model AP240

Dual-channel, 8-bit, 2 GS/s, 1 GHz bandwidth

Model AP235

Dual-channel, 8-bit, 1 GS/s, 500 MHz bandwidth

Signal input

Channels
U1082A-001: Dual at 1 GS/s, Single at 2 GS/s
U1082A-002: Dual at 500 MS/s, Single at 1 GS/s

Bandwidth (-3 dB)
-001: DC to 1 GHz
-002: DC to 500 MHz

Bandwidth limit filter
-001: 700 MHz, 200 MHz, and 20 MHz
-002: 200 MHz and 20 MHz

Full scale (FS)
50 mV, 100 mV, 200 mV, 500 mV, 1 V, 2 V, and 5 V

Offset range
±2 V for 50 mV to 500 mV FS
±5 V for 1 V to 5 V FS

Maximum input voltage
±5 V DC

Coupling
AC, DC

Impedance
50 Ω ± 1%

Connectors
BNC or SMA, gold plated

Digital conversion

Sample rate
-001: 100 S/s to 2 GS/s
-002: 100 S/s to 1 GS/s
in 1, 2, 2.5, 4, 5 sequence

Resolution
8 bits

DNL
±0.9 LSB

Time base

Clock accuracy
Better than ±2 ppm

Sampling jitter
< 10 ps rms for 20 µs with internal clock and reference

Internal and external trigger

External trigger input
Threshold adjust range: (FS/2, -FS/2) for FS = 500 mV, 1 V, 2 V, and 5 V
Impedance: 50 Ω
Maximum input voltage: ±5 V DC
Amplitude range: > 10% FS

Coupling
DC, AC LF reject (50 Hz cutoff) and HF reject (50 kHz cutoff)

Modes
Edge, positive and negative
Window
HF: divide by 4

Control I/O (MMCX)

Ctrl I/O A and B signals
TTL & CMOS compatible (3.3 V)

Ctrl I/O A and B output
10 MHz reference clock out with 50 Ω impedance
Acquisition active
Acquisition skipping to next segment
Trigger ready

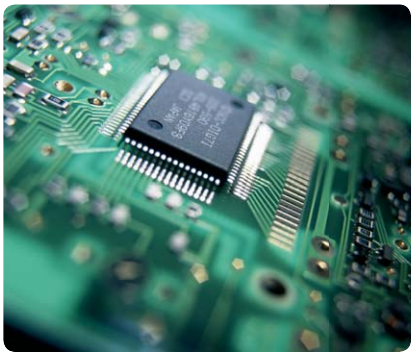
Ctrl I/O A and B input
Trigger enable

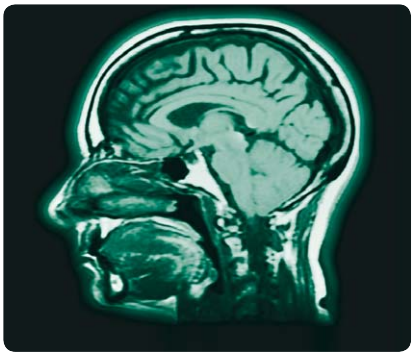
Trigger OUT
Offset: ± 2.5 V (no load)
Amplitude: ± 0.8 V (no load), ±15 mA max
Rise/fall time: 2.5 ns into 50 Ω
Coupling: DC
Output impedance: 50 Ω

CLK IN ext. clock/ref
Amplitude: > 1 V pk-pk into 50 Ω
Threshold: variable between -2 V and +2 V
Maximum input voltage: ±5 V DC

CLK IN ext. clock input
-001: 20 MHz to 2 GHz
-002: 20 MHz to 1 GHz

CLK IN ext. reference frequency
9 MHz to 10.2 MHz





System performance

DC accuracy
±2.0% of FS for ≥ 100 mV FS
±2.5% of FS for 50 mV FS

Effective bits (max. SR) typ.
7.0 at 10.7 MHz, 200 MHz BWL
6.4 at 99.5 MHz, 200 MHz BWL
5.6 at 407 MHz, 700 MHz BWL

INL
< ±1% FS

SFDR typ.
> 55 dB at 10.7 MHz
> 40 dB at 407 MHz

General

Host computer and operating system
PC compatible (x86) systems running Microsoft Windows XP, Windows 2003 Server, Windows 2000, Wind River VxWorks, National Instruments LabVIEW RT, or Linux. PowerPC systems running Wind River VxWorks.
For more information on which specific processors and operating system versions are supported, please contact us.

Transfer speed
High-speed PCI bus transfers data at sustained rates to host computer: Up to 100 Mbytes/s for 32-bit/33 MHz operation

Warranty

1 year

Environmental and physical

Operating temperature
0° to 40°C

Relative humidity
5 to 95% (non-condensing)

Dimensions
PCI long-length standard

Safety
Complies with EN61010-1

EMC immunity
Complies with EN61326-1
Industrial Environment

EMC emissions
Complies with EN61326-1 Class A for radiated emissions

Power consumption
See firmware option specifications

Firmware for Sustained Sequential Recording

- **Dual-bank memory system with on-board automatic switching allowing sustained sequential recording (SSR) to host PC in sequence mode at high sustained trigger and data rates**
- **1 GHz bandwidth with synchronous start-on-trigger dual-channel sampling at rates up to 1 GS/s (2 GS/s in single-channel mode)**
- **Minimum dead time between successive acquisitions allowing recording in sequence mode with sustained trigger rate of up to 100 kHz**
- **Smart data gating readout mode using user or threshold-defined gates for effective data reduction and improved event transfer rate**
- **Efficient burst-style acquisitions with trigger rates within the burst of up to 500 kHz, for sequences of 1 µs-long waveforms at GS/s sample rates**
- **Continuous acquisitions and transfer to host PC of digitized data at 100 MS/s sample rate with 99.995% live time in single-segment mode**

Dual-bank memory with automatic switching

With the -SSR firmware option the embedded FPGA present on the U1082A Agilent Acqiris data converter platforms can be programmed to store digitized waveforms in an automatic "ping-pong" fashion in a dual-bank memory system. The "ping-pong" mode allows one memory bank to store a waveform, or sequence of waveforms, while the other memory bank is being read out over the card's fast PCI bus at rates of up to 100 MB/s. The analyzer platforms can digitize and store waveforms at sampling rates of up to 2 GS/s, 1 GS/s with the -002 option.

Minimum bank switching dead time for remarkable sustained rates

The sustained sequential recording (SSR) firmware uses a semaphore-based technique to automatically switch and redirect the digitized data to the second bank once the first one has been filled. Rapid switching combined with state-of-the-art trigger circuitry dramatically reduces dead time between successive acquisitions, and allows automatic sequential waveform recording at remarkably high sustained trigger rates. For example, successive waveforms digitized at 1 GS/s for 1 µs each in sequences of 1,000 segments per memory bank can be continuously acquired and transferred to a PC at sustained rates of up to 100,000 times per second (50,000 if sampling at 2 GS/s).

Trigger rate	Segment length	Segment	Sample rate
100 kHz	1,000 pts	1,000	1 GS/s
50 kHz	2,000 pts	1,000	2 GS/s

Table 1. GS/s acquisitions at high sustained trigger rates

Data gating readout for smart data reduction

The -SSR firmware provides smart "data gating" readout to further maximize the event transfer rate, perform easy and effective data reduction, and reject unwanted information. This enhances the maximum trigger rate possible with the platform. On readout, the user can select "predefined gates" to transfer data points within a user-defined timing range, or "threshold-defined gates" to transfer data points above or below a user-defined threshold.
For sequences of acquisitions at 1 GS/s sample rate, with 1,000 segments of 1,000 points each, the sustained trigger rate can rise above 300 kHz if a data reduction factor of 3 or more is applied.

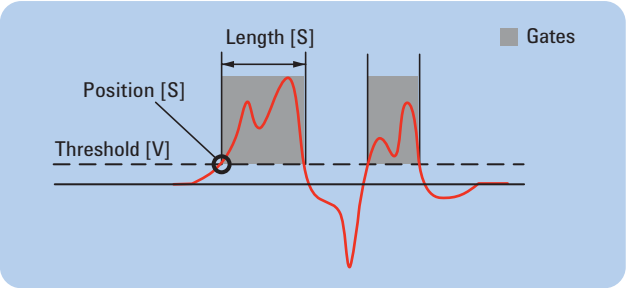


Figure 2. Data rejection with "threshold data gating"

Sequence mode to record burst-style sequence of waveforms

The U1082A analyzer platforms with SSR firmware are ideal for situations where fast sequential or burst-style repetitive signals (or pulses) are being acquired and recorded. Applications include signal intelligence, synthetic aperture radar, ultrasound, radar, and lidar. The SSR firmware also enables burst-style sequential acquisition and recording in sequence mode with trigger rates within the burst of up to 500 kHz for sequences of 1 µs-long waveforms digitized at GS/s sample rates. In particular, taking advantage of the platform's long processing memory option (U1082A-M24), up to 8,191 segments of 1,000 points each can be acquired in a single burst on each memory bank.

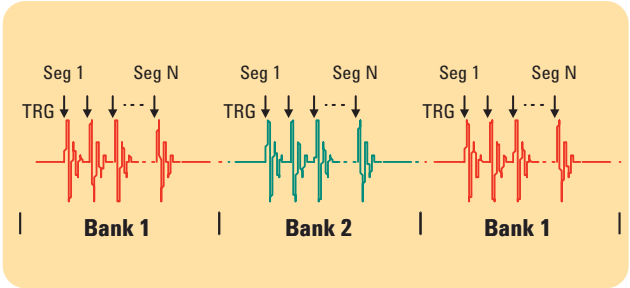


Figure 3. Sequences of burst-style waveforms

Acqiris High-Speed PCI Data Converter Firmware U1082A-SSR

Sustained sequential recording firmware running on U1082A platform

Acquisition capabilities

Acquisition memory bank size
2-4 MSamples of 8 bits
8-16 MSamples of 8 bits (with -M24 option)

Memory bank segmentation
Programmable from 1 to 8,191

Continuous acquisition
At 100 MS/s sample rate with 99.995% live time in single-segment acquisition mode
At 1 or 2 GS/s sample rates if data reduction of factor of 10 or 20 is applied

Segment length
Programmable from 16 to
2-8 MSamples in steps of 16 samples in dual-channel mode
Programmable from 32 to
4-16 MSamples in steps of 32 samples in single-channel mode

Time base and trigger

Acquisition modes
Single segment
Sequence (multiple segments)
< 1.5 µs dead time between successive triggers during an acquisition (within a memory bank)

Pretrigger
Not available

Posttrigger delay (in samples)
Programmable from 0 to 16 MSamples in steps of 16 samples in dual-channel mode
Programmable from 0 to 32 MSamples in steps of 32 samples in single-channel mode

Sustained trigger rate [1]
Up to 100 kHz in sequence mode
Up to 330 kHz using data gating readout mode if data reduction factor of 3 or more is applied

Burst trigger rate [2]
Up to 400 kHz within the burst

Clock synchronization to trigger input
At 2 GS/s or 1 GS/s dual-channel
±200 ps (synchronized)
±500 ps (nonsynchronized)

At 1 GS/s single-channel
±325 ps (synchronized)
±1 ns (nonsynchronized)

Trigger output synchronization
< ±100 ps with respect to sampling clock

Acquisition trigger timestamps
The time of trigger is recorded using the 10 MHz reference clock. It can be reset with a hardware signal on the FPGA control line.

System performance

Readout modes
Raw data

Data gating, definable for each channel:
Predefined gates
Threshold-defined gates (including pre- and post-threshold samples)

On-board automatic switch
Dual-bank memory architecture with automatic switching
On-board automatic switching dead time between successive acquisitions (within memory banks): < 2µs

1) In sequence mode, with 1,000 segments per memory bank, each one of 1,000 samples at 1 GS/s

2) In sequence mode, with 1 µs-long waveforms and posttrigger delay set to zero sample rates over 1 GS/s

General

Power consumption typ.
37 W
At maximum sampling rate

Current requirements typ.

	U1082A	Fan
+12 V	< 0.84 A	-
+5 V	< 2.0 A	< 0.16 A
+3.3 V	< 5.0 A	-
-12 V	< 0.03 A	-

Firmware for Real-Time Sampling and Averaging

- **Synchronous, dual-channel real-time sampling and averaging with a maximum trigger rate of over 333 kHz**
- **Averaging from 1 to 65,536 triggers per segment**
- **Control of 2 to 8 MSamples per channel averaging memory**
- **Round robin and standard segment averaging**
- **Start-on-trigger mode with front-panel add/subtract control**
- **Trigger and clock synchronization modes for improved accuracy**
- **Noise Suppressed Accumulation (NSA)**
- **ADC dithering achieving 12-bit dynamic range**
- **Embedded TDC histogram mode, showing signal peak distribution in the time domain**

Synchronous dual-channel fast averaging

With the -AVG firmware option for U1082A Agilent Acqiris data converter platforms, the embedded FPGA on the platform is programmed to perform the retrieve, add, and store functions necessary to average signals in real time at the card's maximum sampling rate.

Signal averaging reduces random noise effects, thus improving the signal-to-noise ratio, as well as increasing resolution and dynamic range.

Ultrafast summing capabilities of up to 1 GS/s real-time sampling rate can be reached simultaneously on the two channels (2 GS/s real-time in single-channel mode, on either input), with exceptionally high data transfer rates to the host PC.

Segment accumulation and round robin

In time-resolved applications where multiple averaged waveforms must be acquired with very low dead time, the averaging memory can also be segmented. This allows the user to store from 1 up to 8,191 separate accumulations of summed data. The segment length is user-programmable.

In standard segment accumulation mode the user selects the desired number of triggers per segment, N. The next segment will be started after the previous N triggers have been processed.

A round robin segment accumulation is also available. In this mode consecutive triggers are accumulated in different segments. In particular, for stimulus-response experiments, one segment could be the averaged stimulus and another could be the averaged response.

Add/subtract feature

The Averaging firmware also uses the real-time processing control I/O connectors present on the host platform to choose, at the instant the trigger arrives, whether the data of the new trace will be added to or subtracted from the accumulated sum. This gives the user control over how background noise is taken into account in the accumulated sum.

16-bit data readout

A 16-bit fast readout capability is available for applications in which the full 24-bit precision of the accumulated sum data is not desired.

Improved timing

In order to provide superior timing accuracy for successively summed triggers, the Averager firmware supports two sampling modes (Synchronized and Nonsynchronized) with respect to the input trigger. In Non-synchronized Mode, the trigger signal starts the digitizing clock. The trigger is not synchronized with respect to the internal sampling clock and the jitter, when adding one acquisition to another, is within the range of ± one half of the sampling period (in dual-channel mode). The Synchronized Mode is the preferred method for applications where the jitter between the traces being summed must be minimized. Upon receipt of the trigger signal, the digitizing clock starts. Then internal timing circuitry is used to synchronize the sampling clock with the trigger to within ±200 ps (when sampling at 2 GS/s). This mode has the additional benefit of minimizing the overall loss of system bandwidth that would otherwise be associated with the averaged signal.

Noise suppressed accumulation (NSA)

In some applications, such as time of flight spectroscopy, the signal is a rare event sitting on top of a noisy baseline and the averaging process reduces the random noise. However, to enhance the averager's ability to detect such signals in the presence of synchronous noise, the -AVG firmware allows the user to set a threshold that must to be exceeded for each data value to be entered into the sum.

Furthermore, as an aid to the user, or in order to avoid overflow in the summed data, a fixed number, the noise base, can be subtracted from each data value before the summation is done. A similar capability is implemented for negative-going signals.

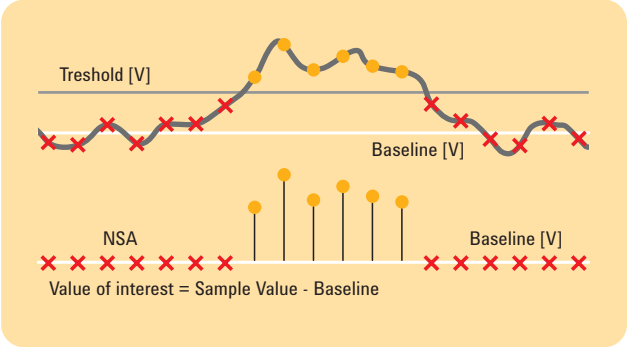


Figure 4. Signal detection using noise suppressed accumulation

Acqiris High-Speed PCI Data Converter Firmware U1082A-AVG

Real-time sampling and averaging firmware running on U1082A platform

Acquisition capabilities

Acquisition memory size
2 MSamples/channel of 24 bits
8 MSamples/channel of 24 bits (with –M24 option)

Memory segmentation
Programmable from 1 to 8,191

Dithering
Adjustable in range from 0 to 12% FS

Triggers per segment
Programmable from 1 to 65,536

FPGA control (I/O P1 & P2)
Real-time, trigger-to-trigger control of whether to add data to or subtract from the accumulated sum

TDC histogram
Bin width equal to sampling period
Programmable increment

Segment length
Programmable from 16 to 2-8 MSamples in steps of 16 Samples in dual-channel mode
Programmable from 32 to 2-8 MSamples in steps of 32 Samples in single-channel mode

NSA
Vthres, Vbase programmable in 0.4% FS steps

Time base and trigger

Range
-001: Up to 1 ms at 2 GS/s, optionally 4 ms (with –M24 option)
-002: Up to 2 ms at 1 GS/s, optionally 8 ms (with –M24 option)

Clock synchronization to trigger input
At 2 GS/s or 1 GS/s dual-channel
±200 ps (synchronized)
±500 ps (nonsynchronized)

At 1 GS/s single-channel
±325 ps (synchronized)
±1 ns (nonsynchronized)

Pretrigger
Not available

Trigger output synchronization
< ±100 ps with respect to sampling clock

Posttrigger delay (in samples)
Programmable from 0 to 16 MSamples in steps of 16 Samples in dual-channel mode
Programmable from 0 to 32 MSamples in steps of 32 Samples in single-channel mode

Acquisition trigger timestamps
The time of trigger is recorded using the 10 MHz reference clock. It can be reset with a hardware signal on the FPGA control line.

Acquisition modes
Single segment accumulation
Standard segment accumulation
Round robin segment accumulation
3 µs dead time between successive triggers:

System performance

Averaging resolution
24 bits

Transfer to PCI
Up to 25 MSamples/s with 24-bit data readout
Up to 50 MSamples/s with 16-bit data readout

Coherent noise (typical)
With background subtract:
0.005 LSB RMS (85 dB SNR)
Full BW and long-term stability

Without background subtract:
0.025 LSB RMS (71 dB SNR)

Conditions: 65,536 accumulated triggers, 10k samples, no input signal, ext. TRG, 500 mV FS, zero offset, dithering

Effective bits (typical at 1 GS/s)
9.0 at 10 MHz
8.5 at 100 MHz
6.2 at 400 MHz

Conditions: 65,536 accumulated triggers, 10k samples, signal amplitude ±40% at 500 mV FS, dithering

General

Power consumption typ.
43 W
At maximum sampling rate

Current requirements typ.

	U1082A	Fan
+12 V	< 0.84 A	-
+5 V	< 2.0 A	< 0.16 A
+3.3 V	< 7.0 A	-
-12 V	< 0.03 A	-

Firmware for Time-to-Digital Conversion and Peak Analysis

- **Synchronous, dual-channel real-time sampling and processing at up to 1 GS/s**
- **Interleaved single-channel sampling and processing on either input, at up to 2 GS/s**
- **Effective acquisition memory of 2 or 8 MSamples per channel**
- **Multi-peak detection with advanced hysteresis algorithm**
- **12-bit peak interpolation with time resolution down to 1/16th of the sampling period**
- **Dual-bank (ping-pong) memory and post acquisition processing maintains high data throughput**
- **Raw, peak region, or peak data output to PC**
- **Data reduction to peak amplitude and time**
- **Programmable on-board TDC histogram creation with up to 4 billion counts per bin, peak count or summed amplitude**

Advanced peak detection and localization

Ideal for time-of-flight measurements such as ultrasound, lidar, and time-of-flight spectrometry, U1082A-TDC Time-to-Digital Converter and Peak Analysis firmware allows the embedded FPGA present on the Agilent Acqiris AP240 and AP235 analyzer platforms to be programmed to perform advanced peak identification and localization at up to 2 GS/s (1 GS/s AP235).

Hysteresis algorithm for multi-peak detection

The firmware finds peaks, using an advanced algorithm that uses hysteresis for peak qualification.

First, during the acquisition, gate regions are defined. Then, after the data are acquired, the algorithm begins looking for peaks. After the signal has increased from its minimum by some programmable start delta the algorithm searches for the peak value in the digitized data stream. After the signal level drops below the current maximum by the valid delta value, the maximum value in the block of data is validated as a peak. The algorithm then continues looking for another rising start delta. Using this method, multiple peaks can be defined within a large zone of interest, even when densely packed in the waveform data. The firmware can also be used to find negative going peaks.

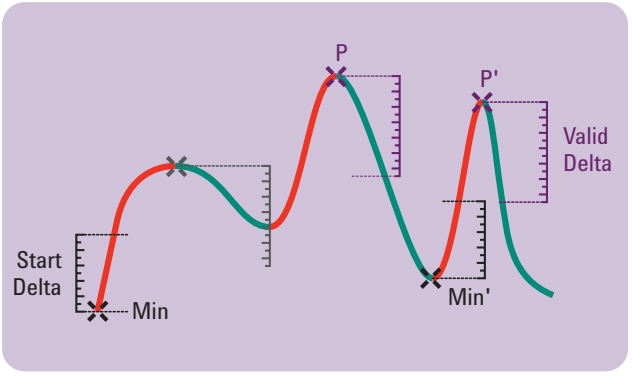


Figure 5. Peak localization using hysteresis algorithm

Peak interpolation

To improve the measurement, peak time and amplitude are determined using an interpolation routine. Fitting a 12-bit quadratic spline to the 3 points around the extrema found by the hysteresis algorithm, the position of a peak maximum is found and defined by its time (Tmax) and amplitude (Vmax). This provides improved time resolution, encoded to 1/16th of the sampling period (31.3 ps AP240, 62.5 ps AP235) and 1/16th of the ADC resolution. This is particularly useful when creating a histogram (or average) from a series of very similar waveforms.

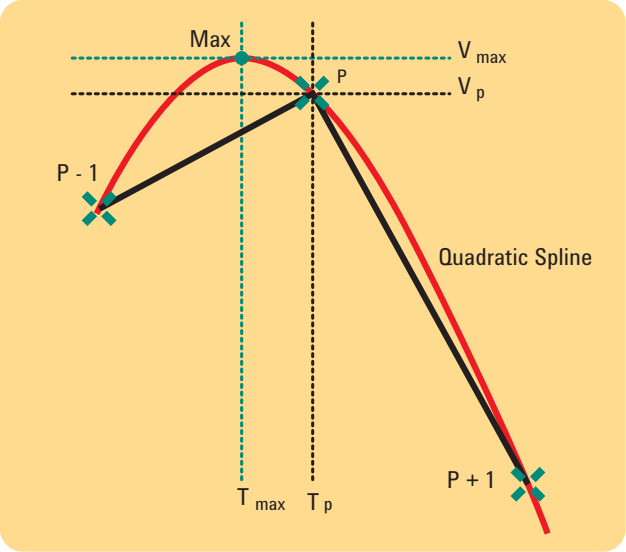


Figure 6. Peak interpolation with quadratic spline

Programmable data output modes

The firmware provides flexible data output while maintaining maximum data throughput through to the host PC.

In “Data Gating” mode the acquired data is dealt with in a simple sustained sequential recording (SSR) fashion. This “ping-pong” memory mode allows one memory bank to be filled while the other, with no post-acquisition processing, is being read out over the analyzer cards’ fast PCI bus at rates of up to 100 MB/s.

Using “Peak Region” mode the validated maximum point and 7 or 15 of its adjacent neighbors are provided so that the user can implement any alternative interpolation routine.

In “Peak Data” mode, the amplitude and position of all of the peaks can be sent to the host for subsequent treatment.

In “Histogram” mode, a TDC histogram is created onboard from the peak timing and amplitude data. With a time resolution as fine as 31 ps per data bin, and allowing for over 4 billion counts per bin, the applied increments, associated with identified peaks, are programmable as counts or as peak amplitudes.

Acqiris High-Speed PCI Data Converter Firmware U1082A-TDC

Time-to-digital conversion and peak analysis firmware running on U1082A platform

Acquisition capabilities

Acquisition memory bank size
2-4 MSamples of 8 bits
8-16 MSamples of 8 bits (with -M24 option)

Memory bank segmentation
Programmable from 1 to 8,191

Segment length
Programmable from 16 to 2-8 MSamples in steps of 16 samples in dual-channel mode
Programmable from 32 to 4-16 MSamples in steps of 32 samples in single-channel mode

Time base and trigger

Acquisition modes
Single segment
Sequence (multiple segments)
< 1.5 µs dead time between successive triggers during an acquisition (within a memory bank):

Pretrigger
Not available

Posttrigger delay (in samples)
Programmable from 0 to 16 MSamples in steps of 16 samples in dual-channel mode
Programmable from 0 to 32 MSamples in steps of 32 samples in single-channel mode

Sustained trigger rate [1]
Up to 100 kHz in sequence mode
Up to 330 kHz using data gating readout mode if data reduction factor of 3 or more is applied

Burst trigger rate [2]
Up to 500 kHz within the burst

Clock synchronization to trigger input
At 2 GS/s or 1 GS/s dual-channel
±200 ps (synchronized)
±500 ps (nonsynchronized)

At 1 GS/s single-channel
±325 ps (synchronized)
±1 ns (nonsynchronized)

Trigger output synchronization
< ±100 ps with respect to sampling clock

Acquisition trigger timestamps
The time of trigger is recorded using the 10 MHz reference clock. It can be reset with a hardware signal on the FPGA control line.

System performance

Readout modes
Peak region data, or peak data for each event
Histogram of peak data over many acquisitions

Data gating, definable for each channel:
Predefined gates
Threshold-defined gates (including pre- and post-threshold samples)

On-board automatic switch
Dual-bank memory architecture with automatic switching
On-board automatic switching dead time between successive acquisitions (within memory banks): < 2µs

1) In sequence mode, with 1,000 segments per memory bank, each one of 1,000 samples at 1 GS/s

2) In sequence mode, with 1 µs-long waveforms and posttrigger delay set to zero sample rates over 1 GS/s

General

Power consumption typ.
47 W
56 W maximum

Current requirements max.

	U1082A	Fan
+12 V	< 1.1 A	-
+5 V	< 2.8 A	< 0.16 A
+3.3 V	< 8.4 A	-
-12 V	< 0.04 A	-

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Contacts

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Ordering Information

Model	Description
U1082A	Acqiris AP240 and AP235 high-speed 8-bit PCI data converter platforms
U1082A-001	1 GHz, 1-2 GS/s, AP240
U1082A-002	500 MHz, 0.5-1 GS/s, AP235
U1082A-M24	24 MB processing memory for U1082A
U1082A-SSR	Firmware for sustained sequence recording
U1082A-AVG	Firmware for real-time sampling and averaging
U1082A-TDC	Firmware for time-to-digital conversion and peak analysis

Accessories

U1082A-UK6	Calibration certificate and cal data

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For more information on the Acqiris product line, sales or services, see our website at:
www.agilent.com/find/acqiris

Product specifications and descriptions in this document subject to change without notice.

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