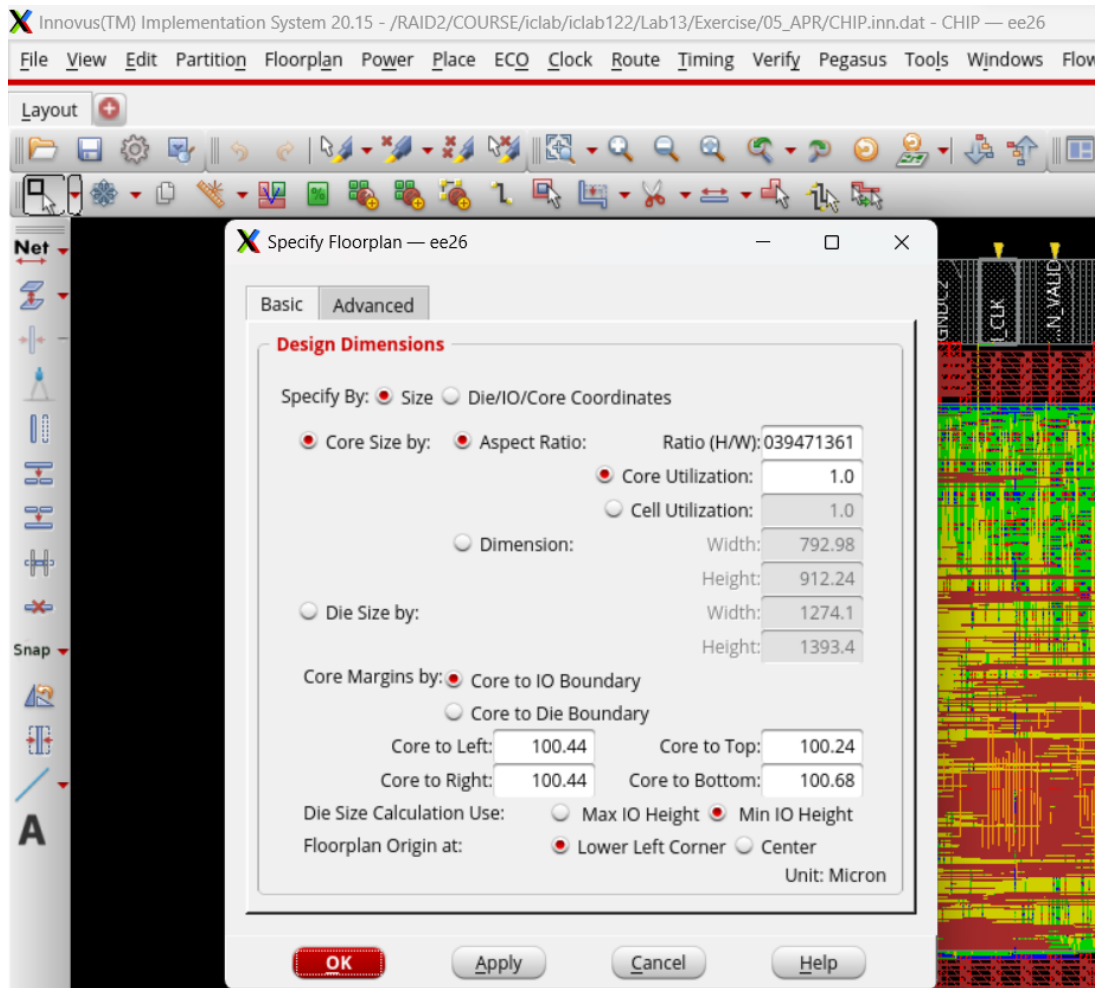
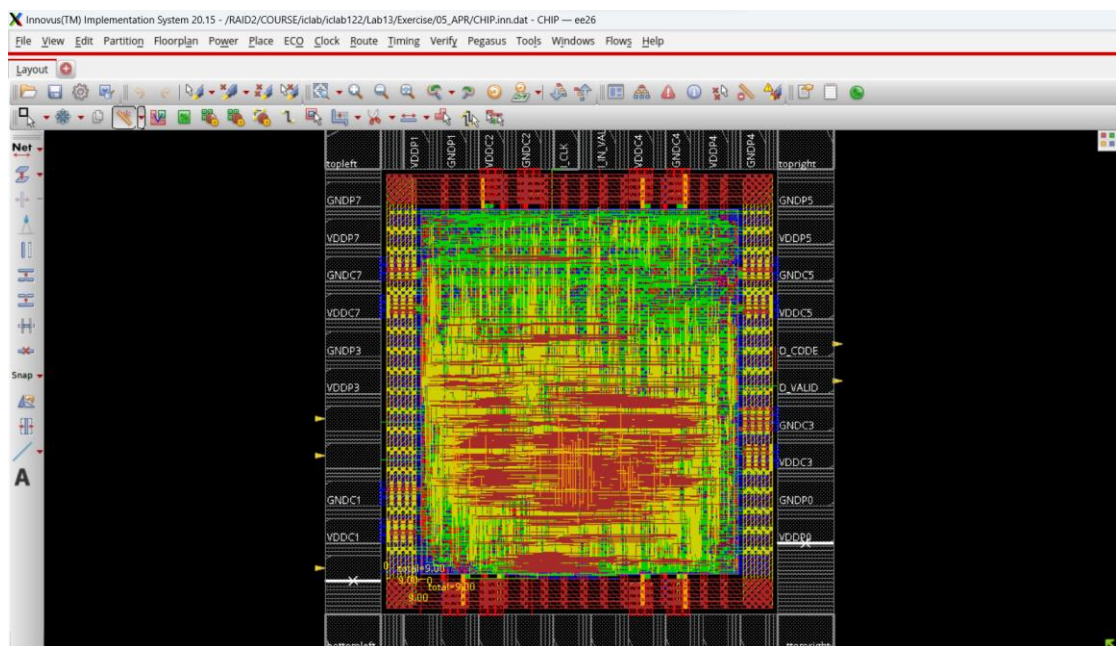


Report

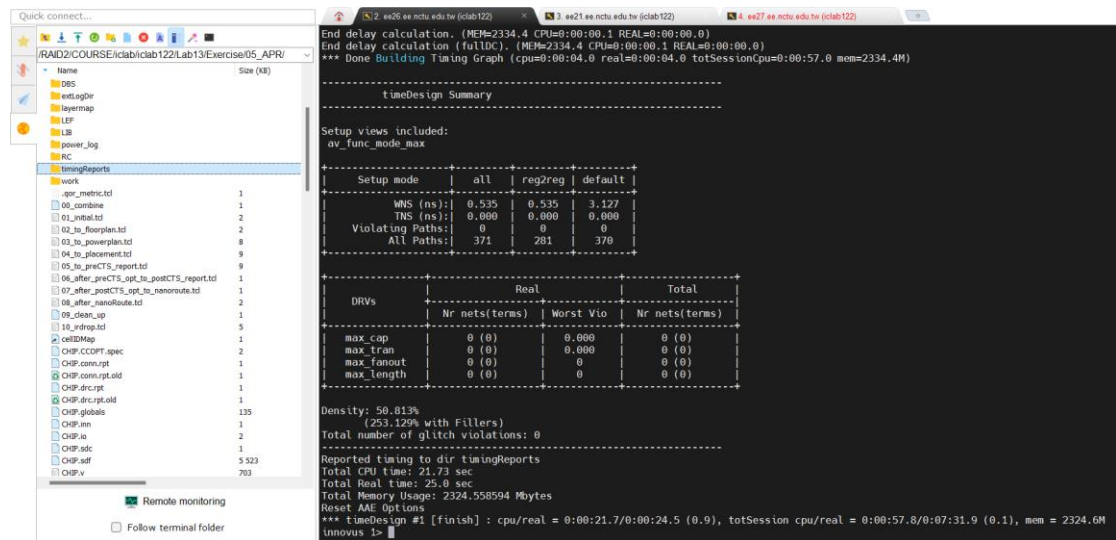
1. Core to IO boundary :



2. Core Ring :



3. Post-Route setup time analysis :



End delay calculation. (MEM=2334.4 CPU=0:00:00.1 REAL=0:00:00.0)
 End delay calculation (fullDC). (MEM=2334.4 CPU=0:00:00.1 REAL=0:00:00.0)
 *** Done Building Timing Graph (cpu=0:00:04.0 real=0:00:04.0 totSessionCpu=0:00:57.0 mem=2334.4M)

timeDesign Summary

Setup views included:
 av_func_mode_max

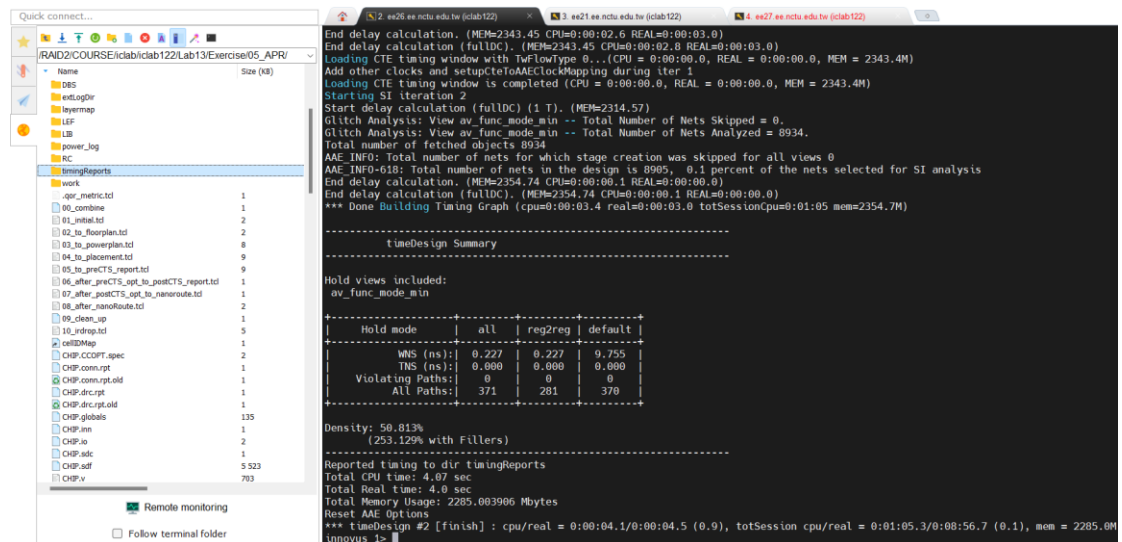
Setup mode	all	reg2reg	default
WNS (ns):	0.535	0.535	3.127
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	371	281	370

DRVs	Real		Total	
	Nr nets (terms)	Worst Vio	Nr nets (terms)	
max_cap	0 (0)	0.000	0 (0)	
max_tran	0 (0)	0.000	0 (0)	
max_fanout	0 (0)	0	0 (0)	
max_length	0 (0)	0	0 (0)	

Density: 50.813%
 (253.129% with Fillers)
 Total number of glitch violations: 0

Reported timing to dir timingReports
 Total CPU time: 21.73 sec
 Total Real time: 25.0 sec
 Total Memory Usage: 2324.558594 Mbytes
 Reset AAE Options
 *** timeDesign #1 [finish] : cpu/real = 0:00:21.7/0:00:24.5 (0.9), totSession cpu/real = 0:00:57.0/0:07:31.9 (0.1), mem = 2324.6M
 tinovus i>

4. Post-Route hold time analysis :



End delay calculation. (MEM=2343.45 CPU=0:00:02.6 REAL=0:00:03.0)
 End delay calculation (fullDC). (MEM=2343.45 CPU=0:00:02.8 REAL=0:00:03.0)
 Loading CTE timing window with TwFlowType 0... (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2343.4M)
 Add other clocks and setupCteIoAAEClockMapping during iter 1
 Loading CTE timing window is completed (CPU = 0:00:00.0, REAL = 0:00:00.0, MEM = 2343.4M)
 Starting SI iteration 2
 Start delay calculation (fullDC) (1 T). (MEM=2314.57)
 Glitch Analysis: View av_func_mode_min -- Total Number of Nets Skipped = 0
 Glitch Analysis: View av_func_mode_min -- Total Number of Nets Analyzed = 8934
 Total number of fetched objects 8934
 AAE INFO: Total number of nets for which stage creation was skipped for all views 0
 AAE INFO-618: Total number of nets in the design is 8905, 0.1 percent of the nets selected for SI analysis
 End delay calculation. (MEM=2354.74 CPU=0:00:00.1 REAL=0:00:00.0)
 End delay calculation (fullDC). (MEM=2354.74 CPU=0:00:00.1 REAL=0:00:00.0)
 *** Done Building Timing Graph (cpu=0:00:03.4 real=0:00:03.0 totSessionCpu=0:01:05 mem=2354.7M)

timeDesign Summary

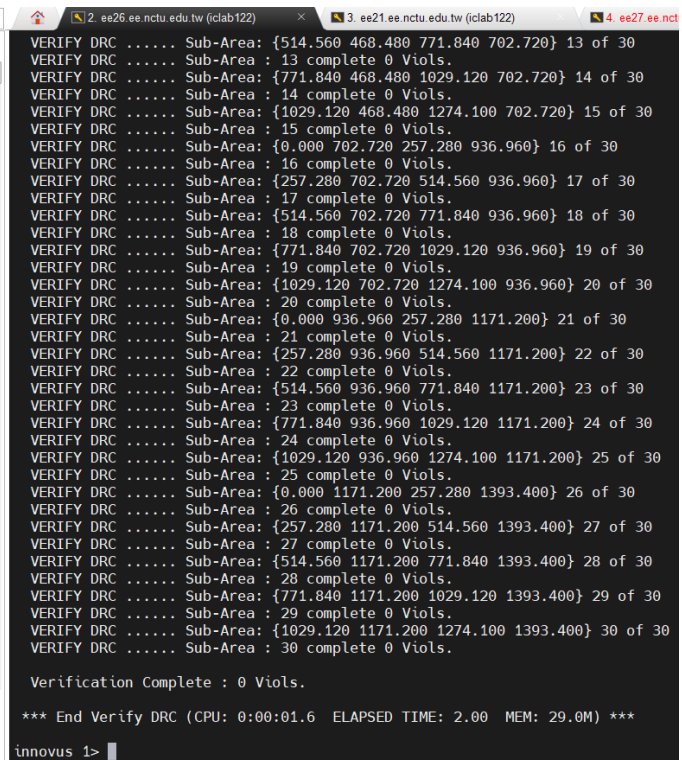
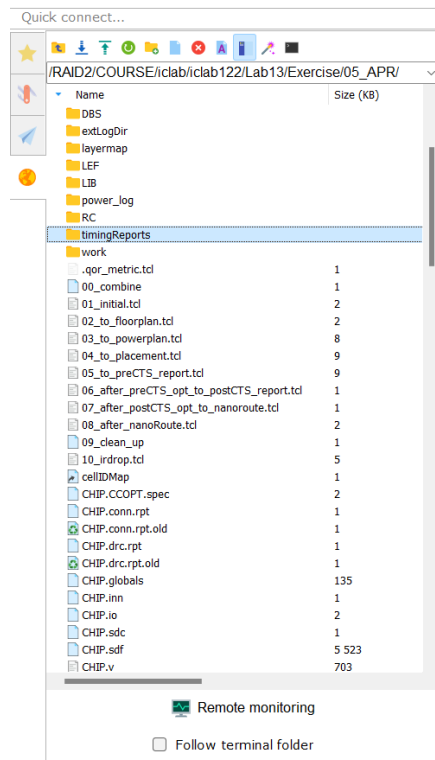
Hold views included:
 av_func_mode_min

Hold mode	all	reg2reg	default
WNS (ns):	0.227	0.227	0.755
TNS (ns):	0.000	0.000	0.000
Violating Paths:	0	0	0
All Paths:	371	281	370

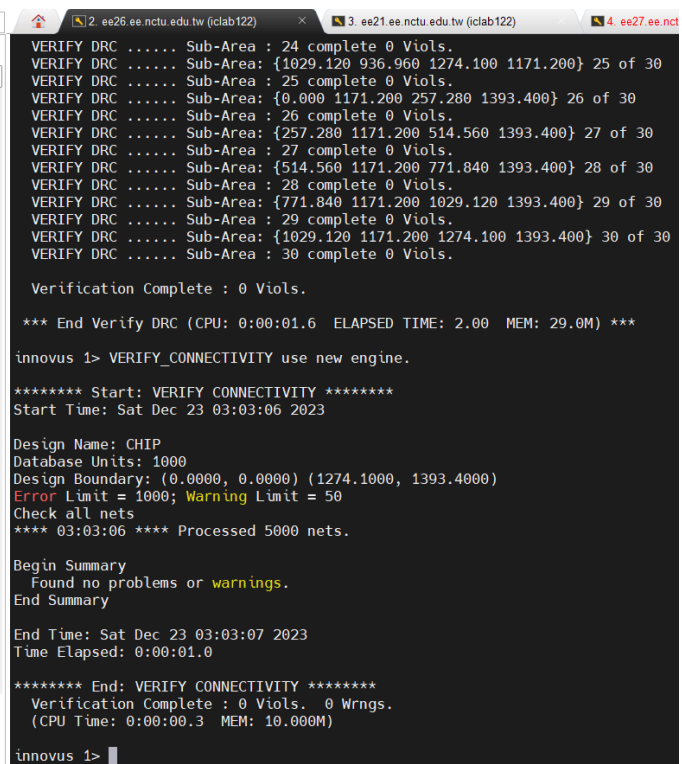
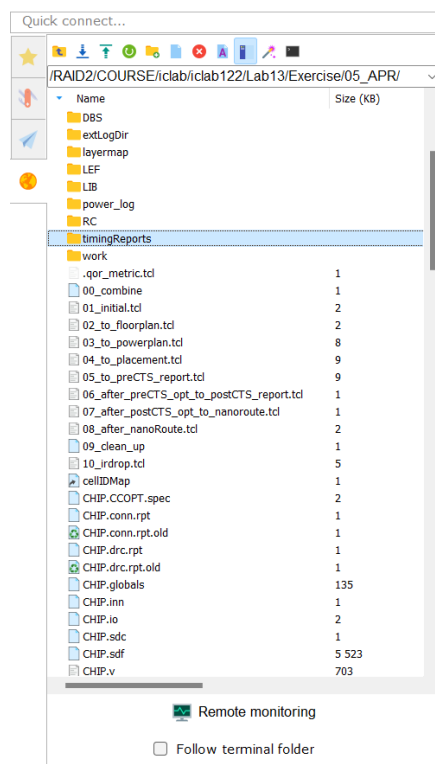
Density: 50.813%
 (253.129% with Fillers)

Reported timing to dir timingReports
 Total CPU time: 4.07 sec
 Total Real time: 4.0 sec
 Total Memory Usage: 2205.003906 Mbytes
 Reset AAE Options
 *** timeDesign #2 [finish] : cpu/real = 0:00:04.1/0:00:04.5 (0.9), totSession cpu/real = 0:01:05.3/0:08:56.7 (0.1), mem = 2285.0M
 tinovus i>

5. DRC result :



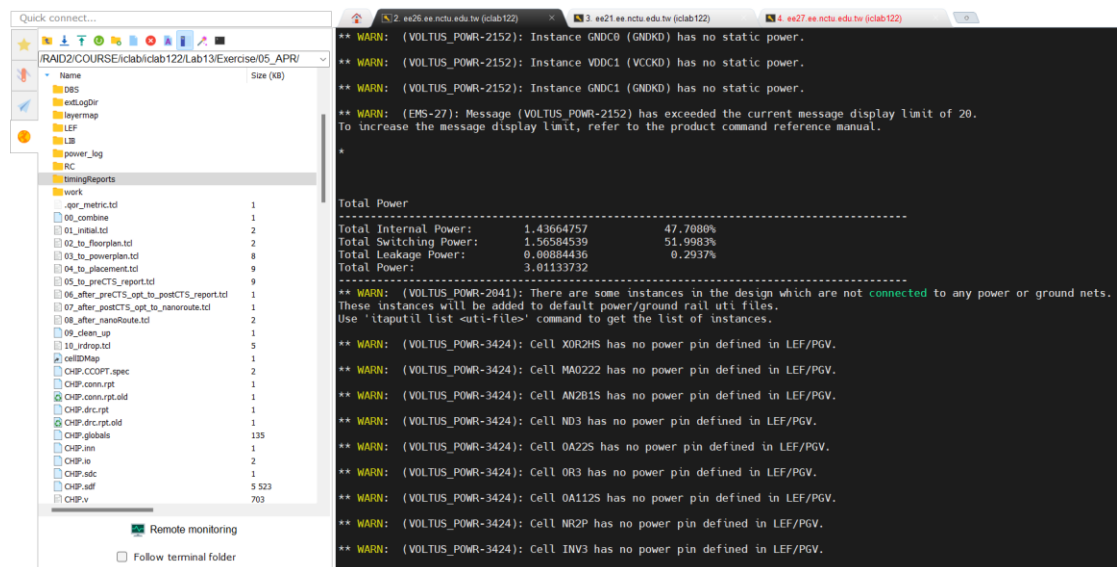
6. LVS result :



7. Post Layout simulation result :

```
PASS PATTERN NO.1983
PASS PATTERN NO.1984
PASS PATTERN NO.1985
PASS PATTERN NO.1986
PASS PATTERN NO.1987
PASS PATTERN NO.1988
PASS PATTERN NO.1989
PASS PATTERN NO.1990
PASS PATTERN NO.1991
PASS PATTERN NO.1992
PASS PATTERN NO.1993
PASS PATTERN NO.1994
PASS PATTERN NO.1995
PASS PATTERN NO.1996
PASS PATTERN NO.1997
PASS PATTERN NO.1998
PASS PATTERN NO.1999
-----
                Congratulations!
                You have passed all patterns!
                Your execution cycles = 32000 cycles
                Your clock period = 20.0 ns
                Total Latency = 640000.0 ns
-----
$finish called from file "PATTERN.v", line 36.
$finish at simulation time      1819630000
      V C S  S i m u l a t i o n   R e p o r t
Time: 1819630000 ps
CPU Time:   26.870 seconds;      Data structure size:   2.2Mb
Sat Dec 23 03:04:11 2023
CPU time: 1.686 seconds to compile + .398 seconds to elab + .604 seconds to link + 26.924 seconds in simulation
3:04 icLab122@ee21[~/Lab13/Exercise/06_POST]$
```

8. Power result :



Quick connect...

RAID2/COURSE/iclab122/Lab13/Exercise/05_APR/

DBS
ee21LogDir
IcVerMap
LEF
LIB
power_log
rc
TimingReports
work
_qor_metric.tcl 1
00_combine 1
01_init.tcl 2
02_to_floorplan.tcl 2
03_to_powerplan.tcl 8
04_to_placement.tcl 9
05_to_jreCTS_report.tcl 9
06_after_jreCTS_opt_to_postCTS_report.tcl 1
07_after_postCTS_opt_to_nanoRoute.tcl 1
08_after_nanoRoute.tcl 2
09_clean_up 1
10_ir_drop.tcl 5
2) cell2Map 1
CHIP.CCOP.spec 2
CHIP.conn.rpt 1
CHIP.conn.rpt.old 1
CHIP.drc.rpt 1
CHIP.drc.rpt.old 1
CHIP.globals 135
CHIP.inn 1
CHIP.io 2
CHIP.sdc 1
CHIP.sdf 533
CHIP.v 703

Remote monitoring
☐ Follow terminal folder

```
** WARN: (VOLTUS_POWR-2152): Instance GND00 (GNDKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance VDDC1 (VCCKD) has no static power.
** WARN: (VOLTUS_POWR-2152): Instance GNDC1 (GNDKD) has no static power.
** WARN: (EMS-27): Message (VOLTUS_POWR-2152) has exceeded the current message display limit of 20.
To increase the message display limit, refer to the product command reference manual.
*
Total Power
-----
Total Internal Power:      1.43664757      47.7880%
Total Switching Power:    1.56584539      51.9983%
Total Leakage Power:      0.00884436      0.2937%
Total Power:              3.01133732
-----
** WARN: (VOLTUS_POWR-2041): There are some instances in the design which are not connected to any power or ground nets.
These instances will be added to default power/ground rail uti files.
Use 'itaputil list <uti-file>' command to get the list of instances.
** WARN: (VOLTUS_POWR-3424): Cell XOR2HS has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell MA0222 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell AN2B1S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell N03 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell 0A22S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell 0R3 has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell 0A112S has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell NR2P has no power pin defined in LEF/PGV.
** WARN: (VOLTUS_POWR-3424): Cell INV3 has no power pin defined in LEF/PGV.
```

9. IR Drop Results :

IR drop最大值为0.10967 mV

平均分配power pad，將stripe之間的間距縮小，都可以使IR drop的最大值降低。

