ECE 385

Fall 2023

Experiment #1

Introductory Experiment

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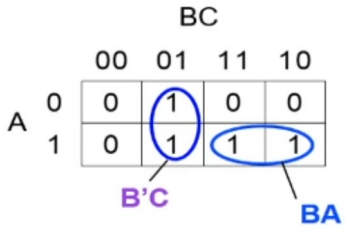
Purpose of Circuit

We want to build a 2 to 1 multiplexer using only NAND gates. The purpose of this Lab is to understand what static hazard is and try to find out a possible solution to fix the problem.

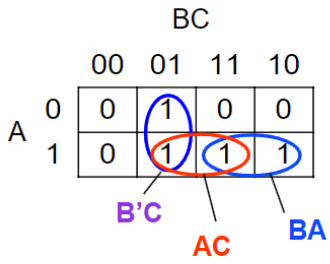
Written Description of Circuit

Part A: In this part we are using one single 7400 chip, which contains four NAND gates to perform the experiment. Inputs A and C are set to high, and we drive input B with a 1 MHz, 0-to-5-volt square wave from the pulse generator. We connect the circuit as Figure 17 from GG. Output of the circuit is connected to the oscilloscope. It acts like a 2 to1 MUX, the output will be A when B is high, and the output will be C when B is low.



$$Z = BA + B'C$$

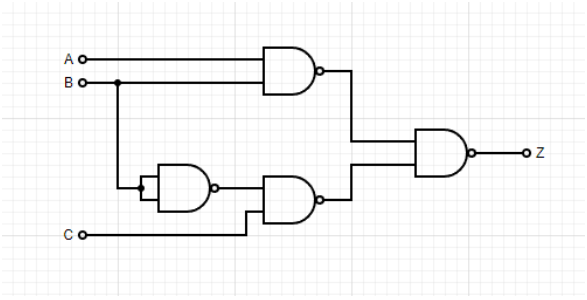
Part B: In this part of the experiment, we design a circuit base on the first part in order to avoid static hazards. Since, glitches are caused by delay of gates, we want to minimize the delays. To avoid Static-1 hazard in an AND-OR (SOP) circuit, we need to cover all adjacent min-terms in the K-map. In this example, we add the term AC. We add another 7400 chip to achieve this goal.



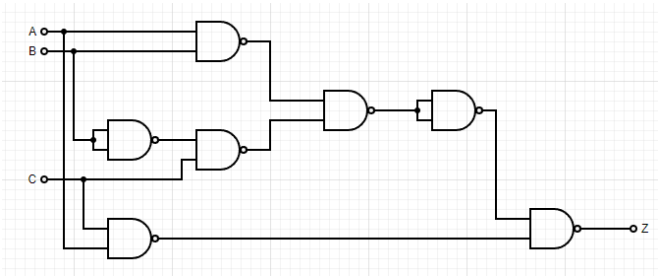
$$Z = BA + B'C + AC$$

Logic Diagrams

Part A:

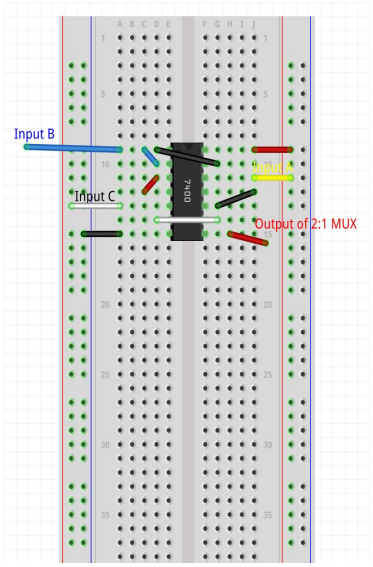


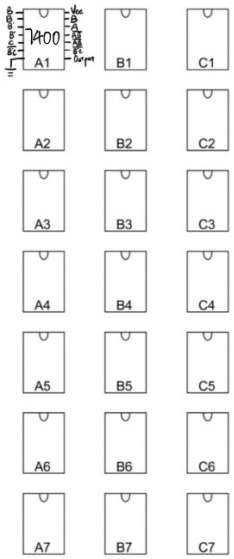
Part B:



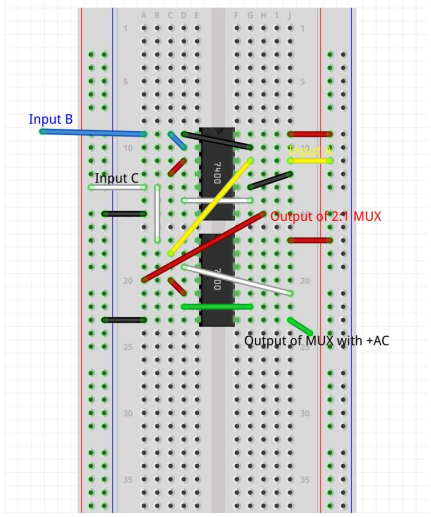
Component Layout

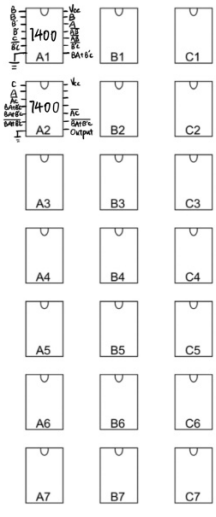
Part A:





Part B:





Answers to Pre-Lab Questions

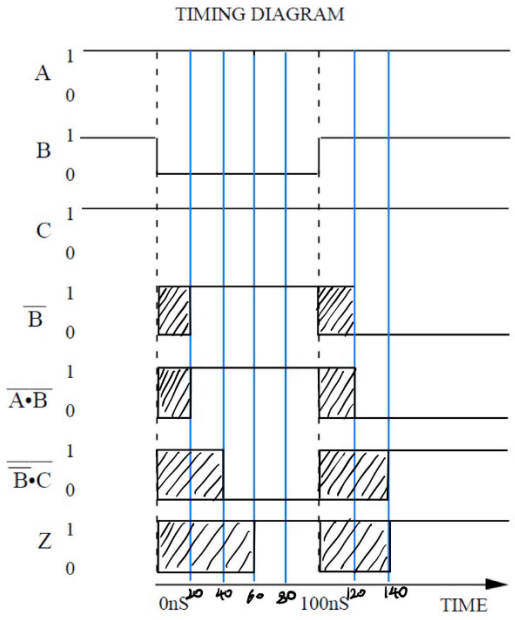
1. Why does the hazard appear when you chain an odd number of inverters together or add a small capacitor to the output of the inverter?
   Because the delay of one inverter is too minute to determine, adding more inverters will make the phenomenon more obvious.

Answers to Lab Questions

1. For the circuit of part A of the pre-lab, at which edge (rising/falling) of the input B are we more likely to observe a glitch at the output?
   For part A, we are more likely to observe a glitch at the falling edge of the input B at the output.

Answers to Post-Lab Questions

1. Complete the timing diagram below for the circuit of part A.

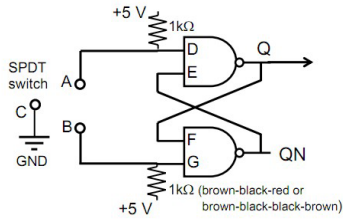


2. How long does it take the output Z to stabilize on the falling edge of B (in ns)?
   60 ns.

3. How long does it take on the rising edge (in ns)?
   60 ns.

4. Are there any potential glitches in the output, Z? If so, explain what makes these glitches occur.
   There are two possible glitches in the output. The first glitch is from 0 ns to 60 ns, and the second glitch is from 100 ns to 140 ns. Glitches occur when there is delay of gates and changes of input values.

5. Explain how and why the debouncer circuit given in General Guide (Figure 22) works. Specifically, what makes it behave like a switch and how the ill effect of mechanical contact bounces is eliminated?



1. Initial Condition: Let's assume the switch is open (not pressed) initially. In this case, Ais low (0), and we can force B to be high (1) to ensure the latch is in the RESET state. So, Q is low, indicating the button is not pressed.
2. Button Pressed: As the button gets pressed, even if there's a bounce, the very first "ON" signal will SET the latch because A becomes high momentarily. After this initial setting, any further bounces won't matter because the latch has already registered the button press and Q remains high.
3. Button Released: When the button is released, A returns to low. The latch retains its previous state, which means Q stays high. If we want Q to return to low, indicating the button is no longer pressed, we will need an external signal or mechanism to trigger the B input and reset the latch.
4. Benefit: The advantage here is that once the latch is set due to a button press, all subsequent bounces are effectively ignored. The latch output remains stable and unaffected by any bouncing of the switch.

Answers to General Guide Questions

1. The Noise Immunity of a gate is defined as the maximum amplitude of a positive-going (noise) pulse added to the nominal logic "0" voltage level or a negative-going (noise) pulse added to the logic "1" voltage level at the input of a gate which does not cause the output of that gate to change its logic value. The nominal logic "0" and "1" voltage levels can be determined by connecting several inverter gates (e.g., 7404) in series and observing the voltage levels at the output of the last inverter when the input to the first inverter is at GND and at +5v. What is the advantage of a larger noise immunity? Why is the last inverter observed rather than simply the first? Given a graph of output voltage (VOUT) vs. input voltage (VIN) for an inverter, how would you calculate the noise immunity for the inverter? (GG.7)
    1. A higher noise immunity is crucial for reliable logic gate operation, especially in noisy environments.
    2. Observing the last inverter is practical as it would show the cumulative effects of noise and signal degradation, providing a kind of worst-case analysis for the circuit's noise immunity.
    3. The smallest of the ranges X and Y determines the overall noise immunity of the device, as this represents the worst-case noise the device can tolerate without a logic level change.

4. To calculate X: Identify the input voltage that leads to the lowest logic 1 output. Then subtract half the nominal range for input logic 0. To calculate Y: You take half the nominal range for input logic 1 and subtract from it the lowest input voltage that results in a logic 0 output. Then take the minimum of X and Y to find the overall noise immunity.

2. If we have two or more LEDs to monitor several signals, why is it bad practice to share resistors? (GG.23)
    1. Forward Voltage Variation: Different LEDs, even of the same color or type, can have different forward voltage drops.
    2. Current Imbalance: Because of the variance in voltage drop, different LEDs in parallel will have different current flows through them. This could lead to uneven brightness and potential overheating of some LEDs.
    3. Unequal Brightness: The brightness of an LED is proportional to the current flowing through it. When LEDs share a resistor, the one with the lowest voltage drop will hog most of the current, making it brighter than the others.

Conclusions

What have you learned? What worked? What didn't? What can you possibility do to enhance/simplify/fix your circuit to make it better?

This lab is about static hazard. This kind of problem may happen when there are delays of gates in the circuit. We can add additional terms to cover all adjacent min-terms in K-map to eliminate static hazard. However, eliminating static hazard is not easy for most circuits.