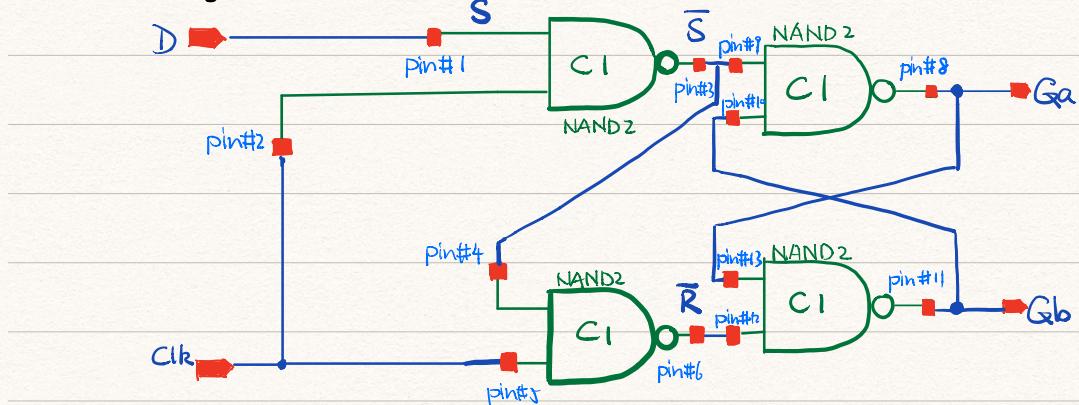


Pre-lab 4

6.1 Draw gate-level schematic for gated D-latch.



CHIPS USED :

C1 - 74LS00 (NAND2)

CONNECTED TO ALL CHIPS :

PIN #7 - Gnd

PIN #14 - Vcc

6.4 Are there any input combinations of clk and D that should NOT be the first you test ? Explain.

① $D = 0, \text{clk} = 0$

② $D = 1, \text{clk} = 0$

It will cause indeterminate outputs since we don't know what are the initial values of Q_a and Q_b .

7.1. Create a Verilog module for the simple ALU with register
with indicated specifications

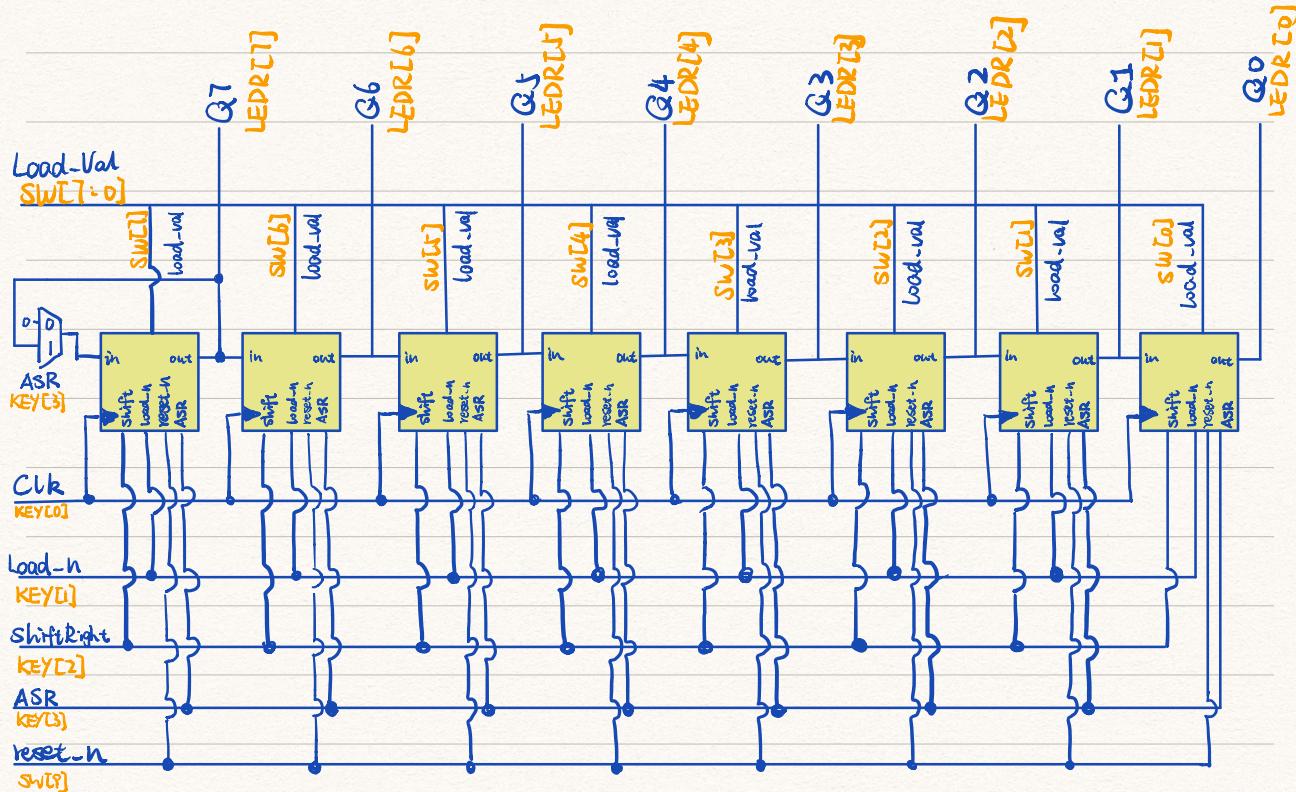
see reg-ALU.v

7.2 Simulate your code with ModelSim (Include screenshots)



8.1. When Load-n = 1 and shiftRight = 0,
the 8 bit shift register will not change
since the output of each shifter bit is
chosen and be loaded to D.

8.2 Draw a schematic for 8-bit shift register



prelab. Use SW_{7-0} as the inputs $LoadVal_{7-0}$ and SW_9 as a synchronous active low reset (reset_n). Use KEY_1 as the $Load_n$ input, KEY_2 as the $ShiftRight$ input and KEY_3 as the ASR input. Use KEY_0 as the clock (clk). The outputs Q_{7-0} should be displayed on $LEDR_{7-0}$. (PRELAB)

8.3 Use Verilog to write a one-bit shifter.
see single-shifter.v

8.4 Write Verilog code for 8-bit shift register.

see full-shifter. ✓

8.5 Simulate your code with ModelSim

