University of Chinese Academy of Sciences

Emerging I/F IP Design

SerDes Design and Simulation

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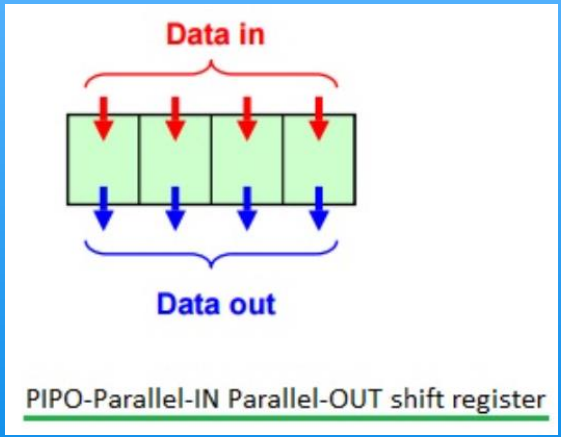
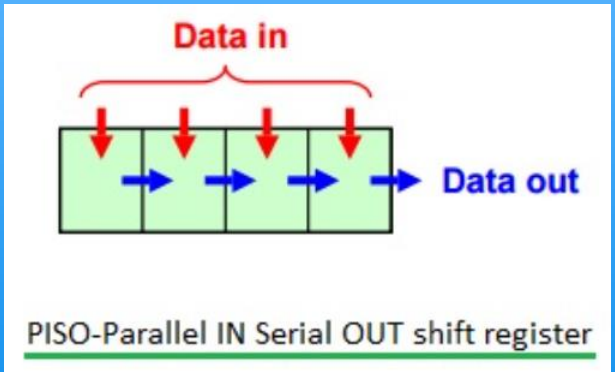
Topics

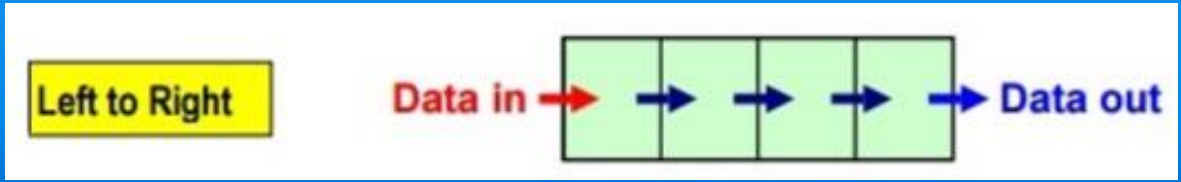
- Serial and Parallel Communication
- Components of SerDes
- Modeling of SerDes
- Implementation of SerDes
- Discussion

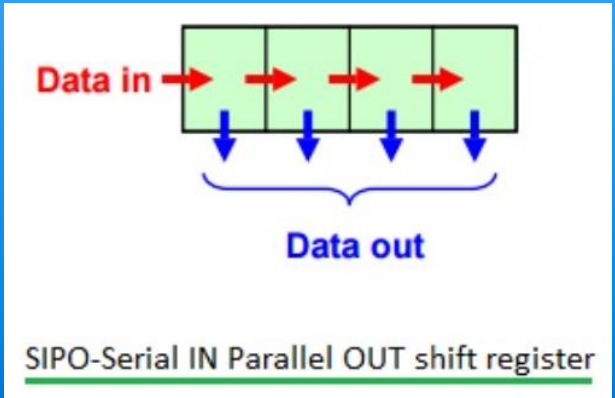
Shift Registers:

- PIPO, PISO, SISO, SIPO

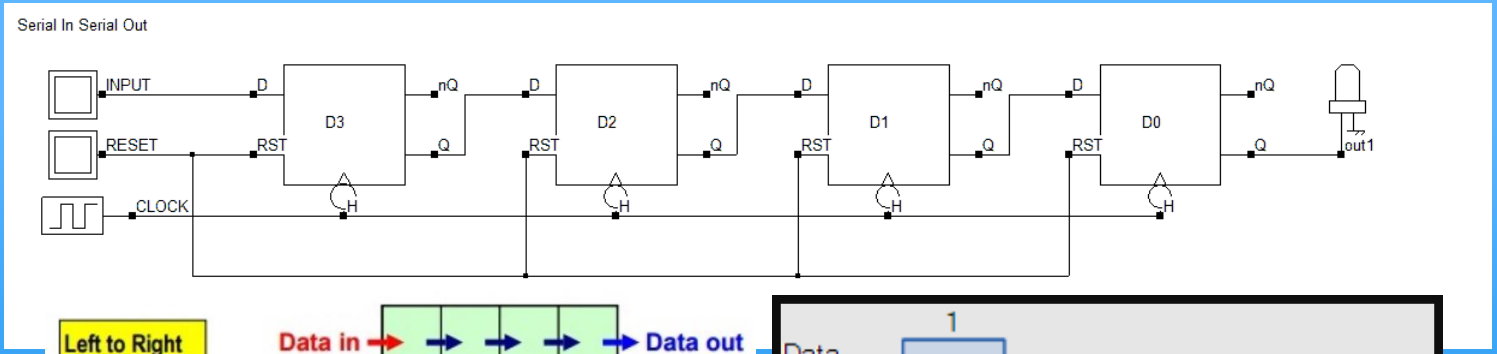


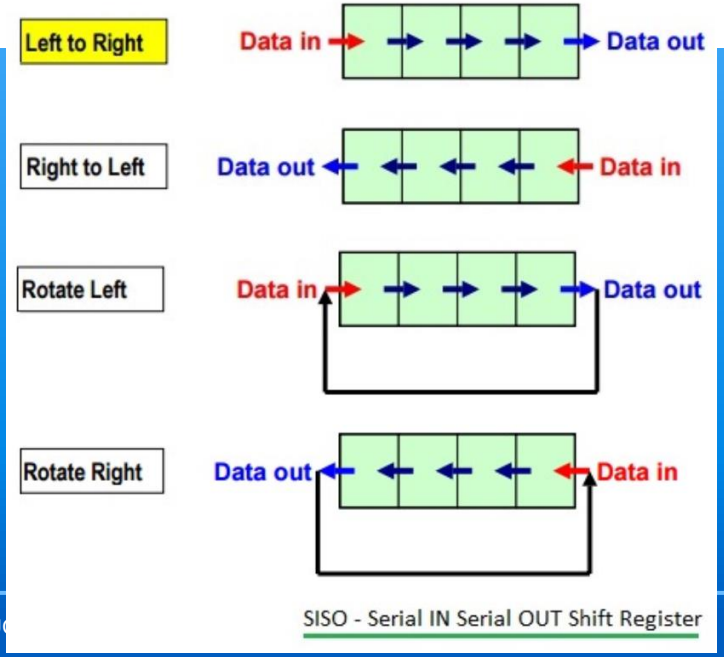


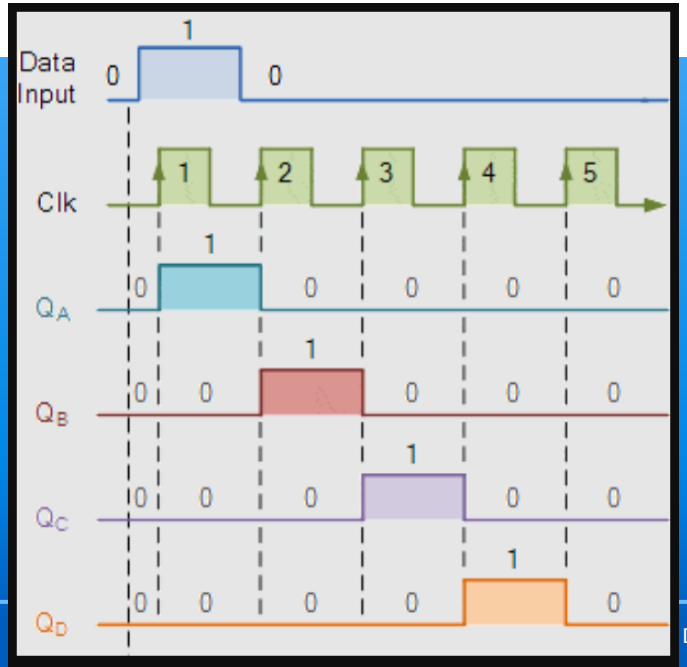




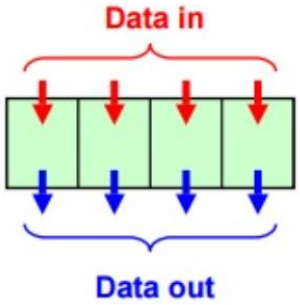
SISO


Serial In Serial Out
INPUT
RESET
CLOCK
D
RST
nQ
Q
H
D3
D2
D1
D0
out1

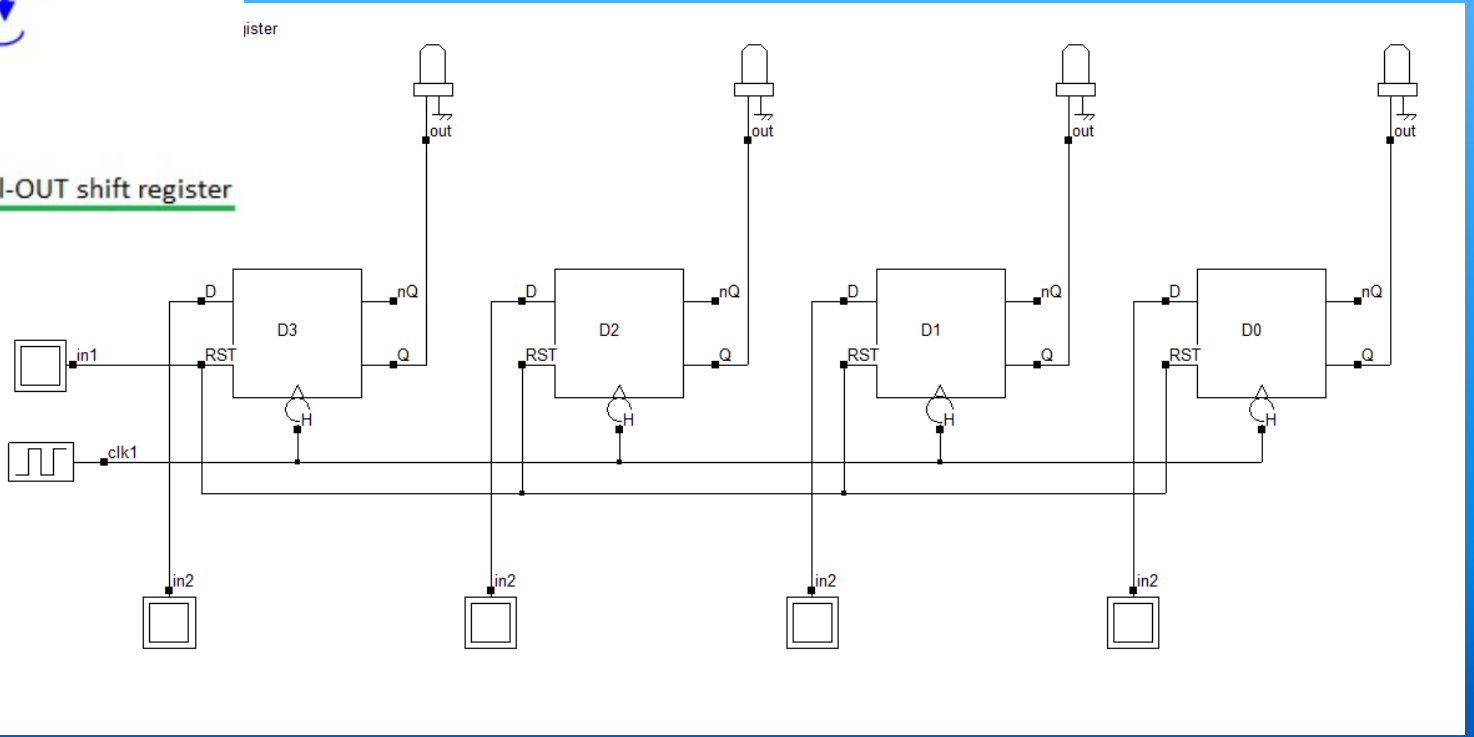

Left to Right
Data in
Data out
Right to Left
Data out
Data in
Rotate Left
Data in
Data out
Rotate Right
Data out
Data in
SISO - Serial IN Serial OUT Shift Register


Data Input
Clk
Q_A
Q_B
Q_C
Q_D

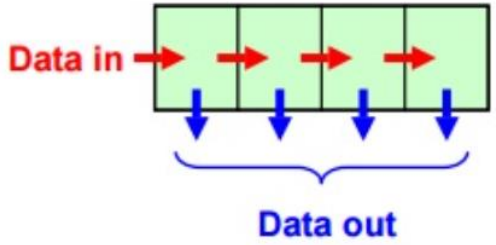
PIPO



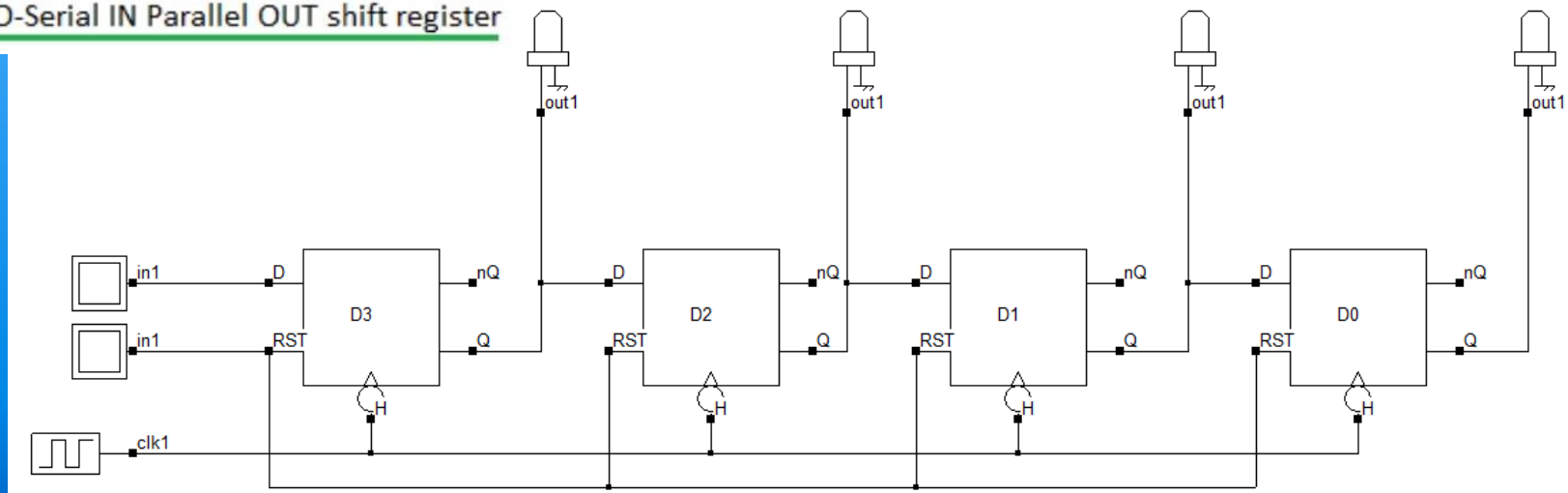
PIPO-Parallel-IN Parallel-OUT shift register



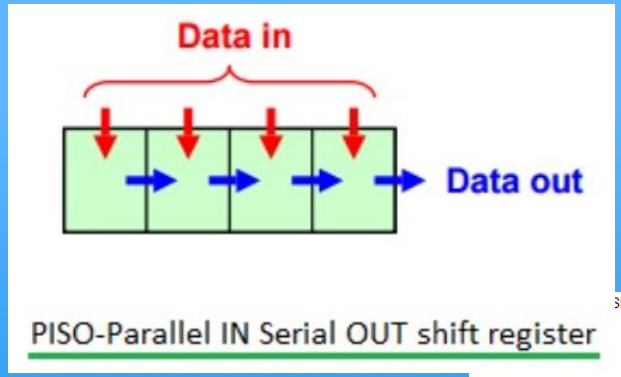
SIPO

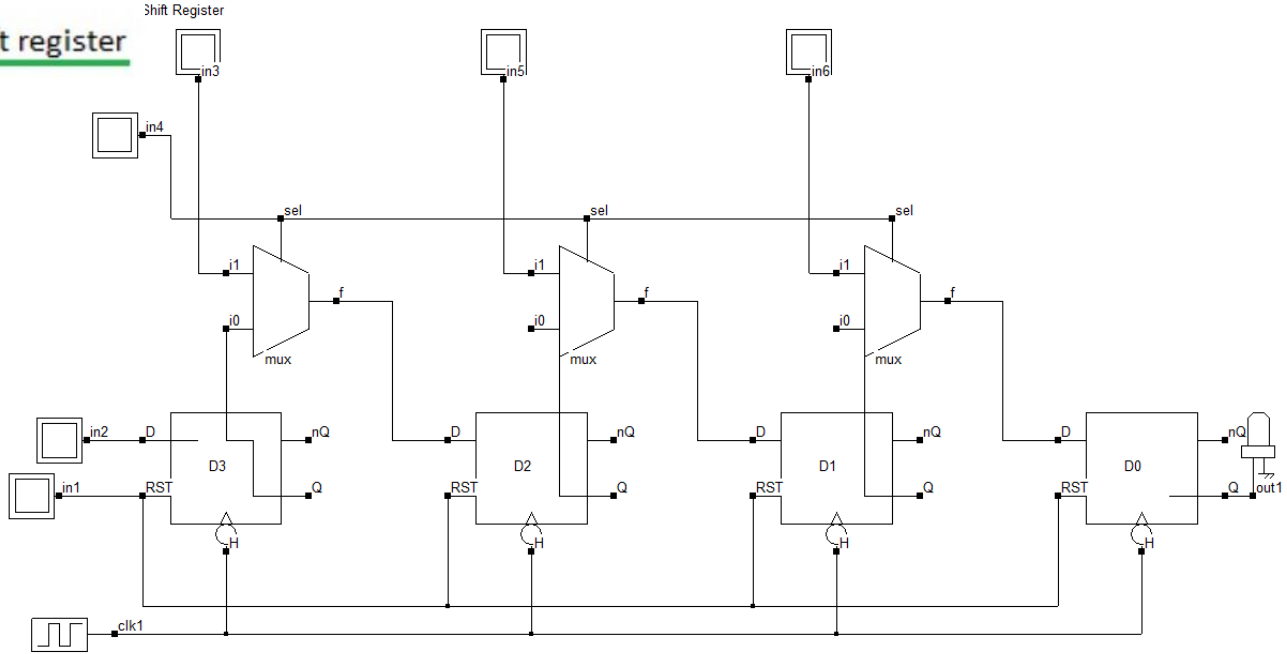


SIPO-Serial IN Parallel OUT shift register



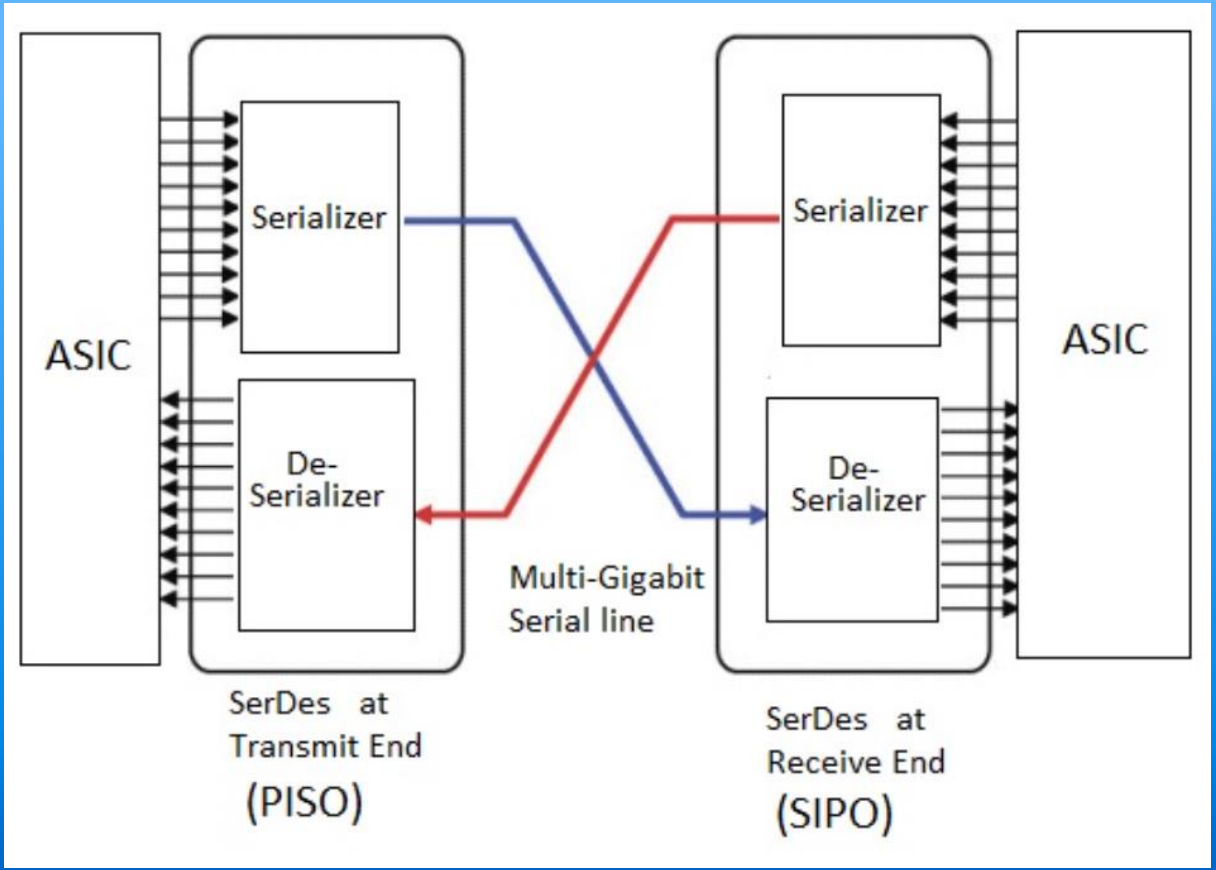
PISO


Data in
Data out
PISO-Parallel IN Serial OUT shift register


Shift Register
in3
in5
in6
in4
sel
sel
sel
i1
i0
f
mux
in2
in1
D
RST
nQ
Q
H
D3
D2
D1
D0
out1
clk1

SerDes used in between ASICs

- PISO
- SIPO

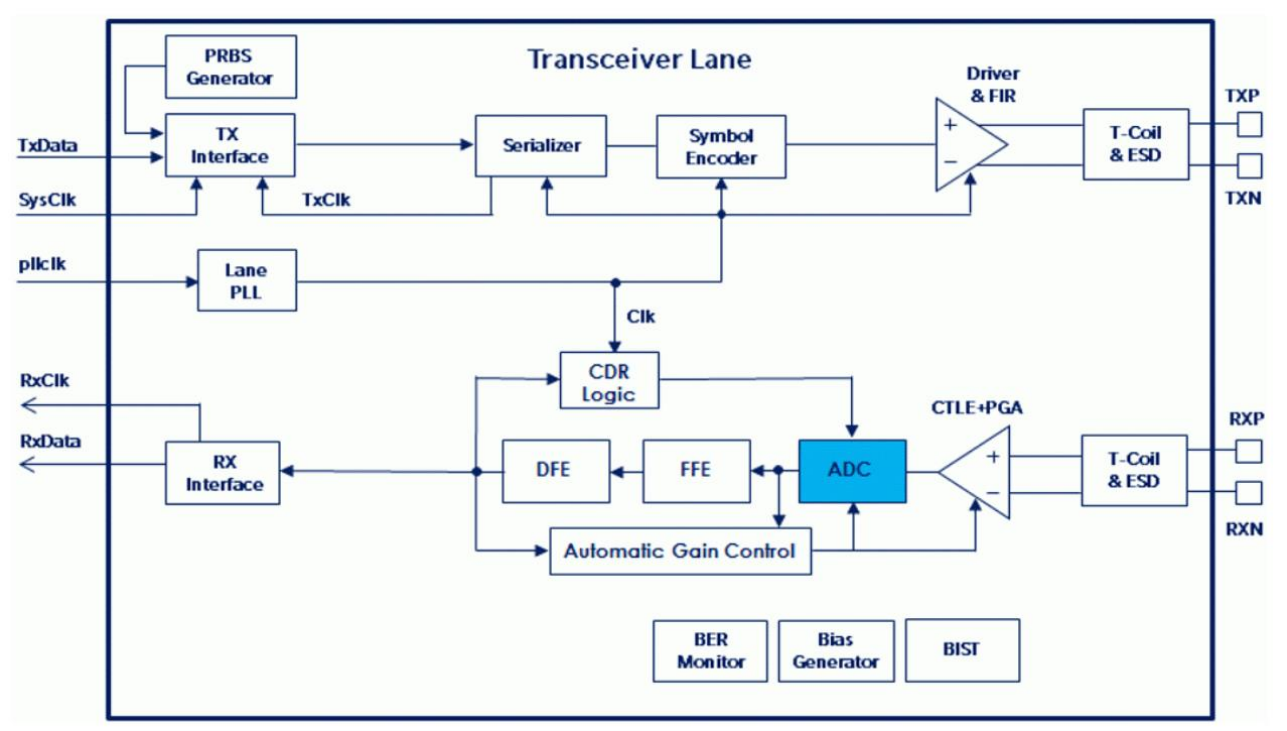


Topics

- Serial and Parallel Communication
- Components of SerDes
- Modeling of SerDes
- Implementation of SerDes
- Discussion

112-Gbps ADC/DSP Long-Reach SerDes PHY

- RAMBUS



SerDes System

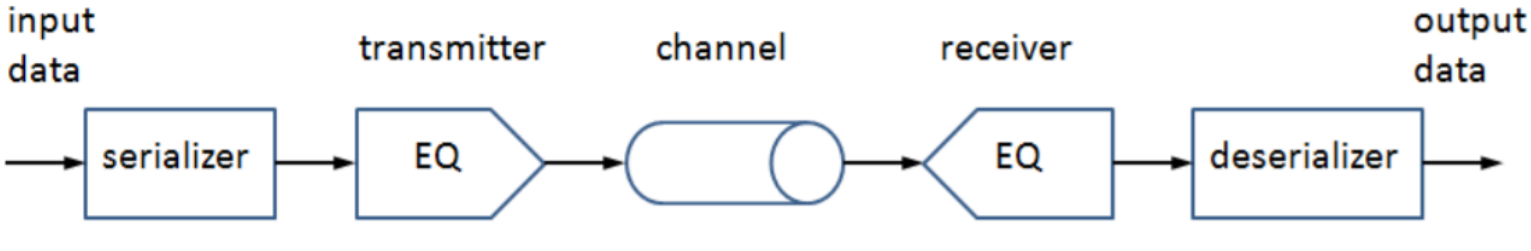
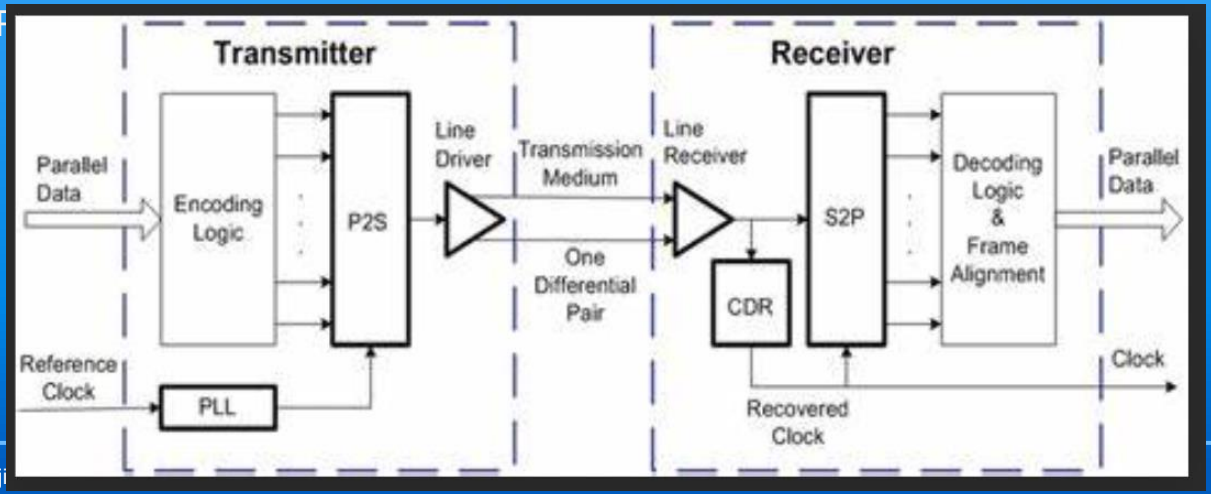


Figure 1. A general SerDes system

- PLL, TX, F

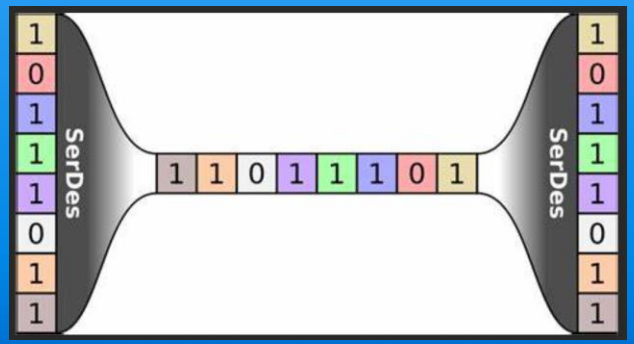


SerDes and PLL

- PLL
  - Reference, Phase comparator/detector (PD),
    Voltage Controlled Oscillator (VCO), Loop Filter;
  - frequency, jitter
- TX
- RX

Key Components in SerDes – TX, RX

- TX: Serial signal, Buffer, 8B/10B Encode/Scrambler, Serializer, Equalizer, Differential Driver
- RX: Receiver, EQ, CDR, De-serializer, 8B/10B Decode/ De-scrambler, Elastic, FIFO



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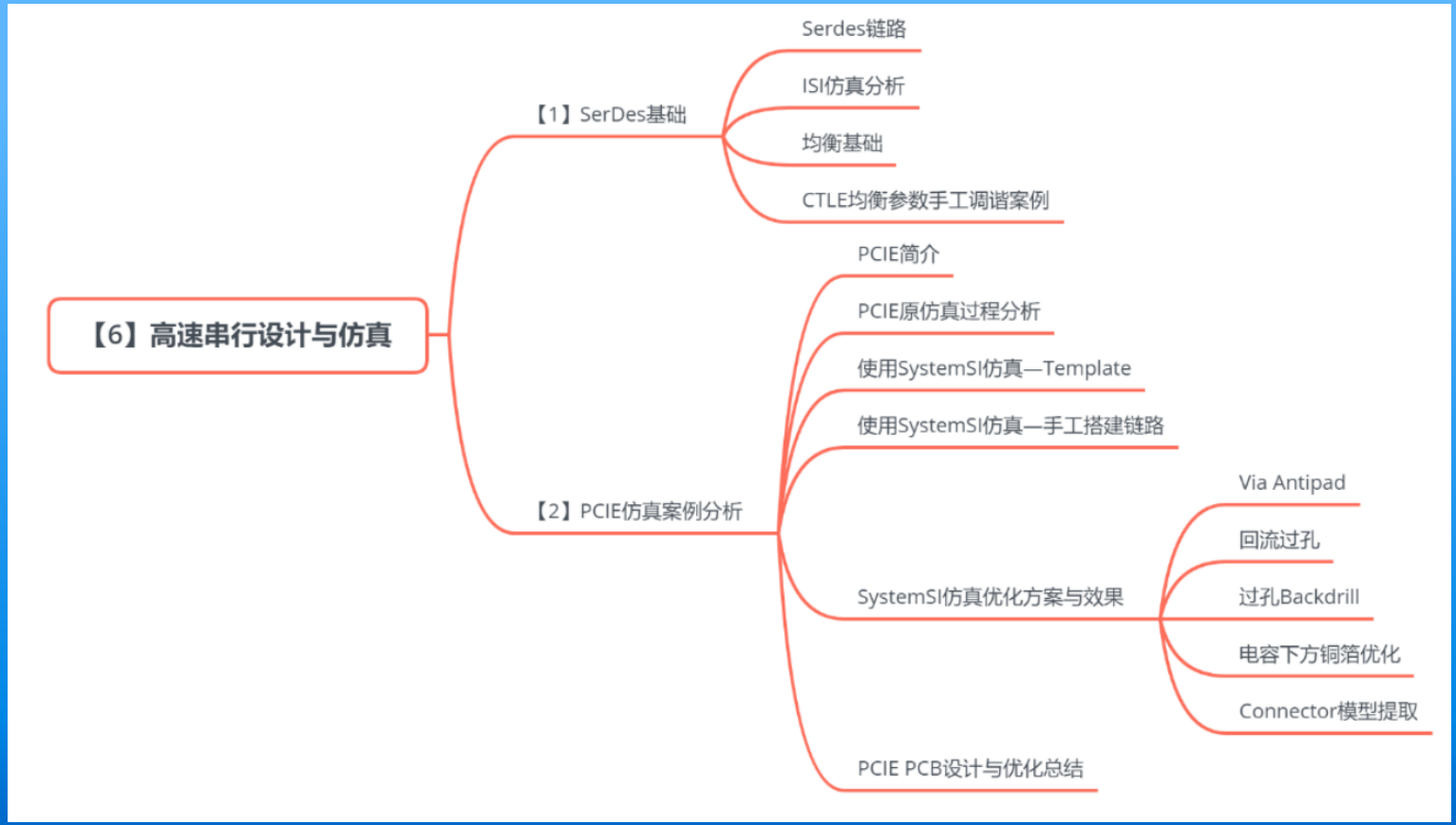
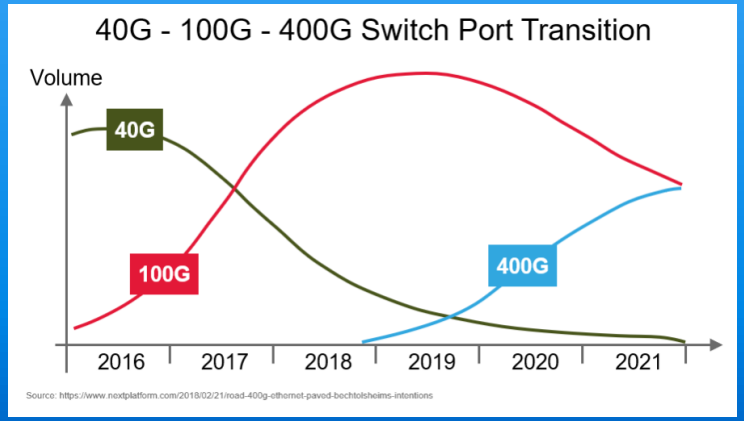
SerDes Simulation



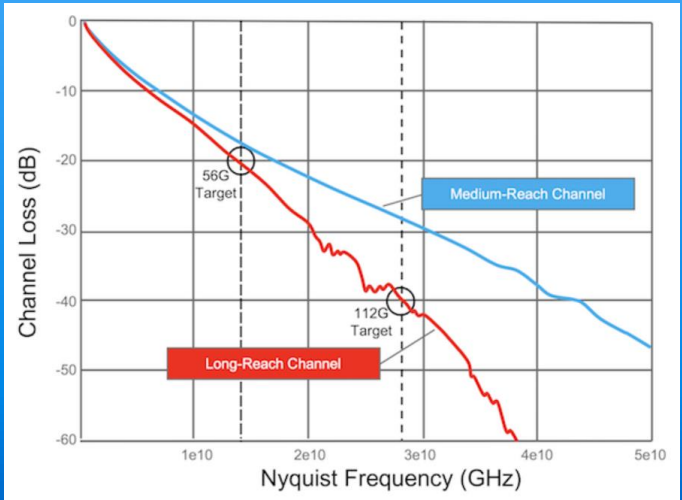
SerDes IP (1/2)

- Traditional MR and LR SerDes
  - PCIe, Ethernet
  - ***NRZ*** modulation (up to 32Gb/s)
- New XSR/USR
  - 50Gb/s – 100Gb/s
  - D2D (die-to-die) application [D2OE]
  - **PAM** (pulse amplitude modulation)



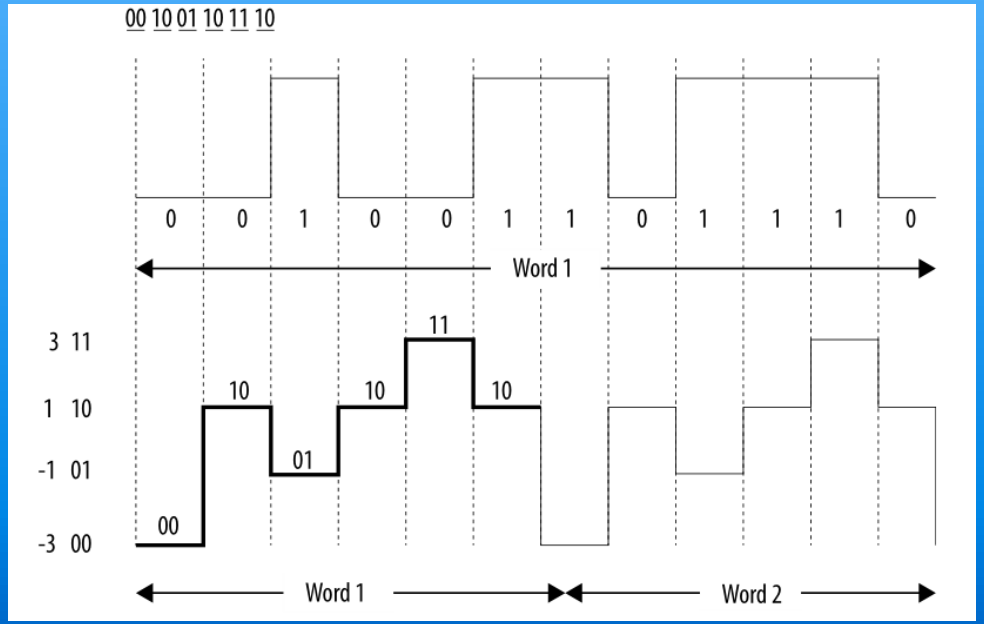
SerDes IP (2/2)

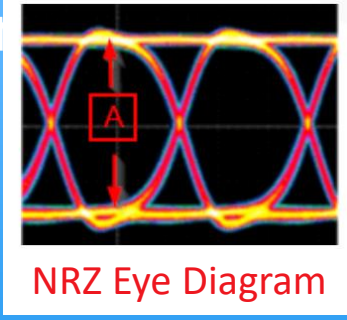
- Traditional MR and LR SerDes
  - PCIe, Ethernet
  - ***NRZ*** modulation (up to 32Gb/s)
- New XSR/USR
  - 50Gb/s – 100Gb/s
  - D2D (die-to-die) application [D2OE]
  - **PAM** (pulse amplitude modulation)



NZR (PAM2) and PAM4

- Non-Return-to-Zero (NRZ), also called Pulse Amplitude Modulation 2-level





NRZ Eye Diagram

NZR (PAM2) and PAM4

- NZR: 10, 16, 32Gbps
  - Process: 0.18um, 65, … 28nm
- PAM4: 56, 112, 224Gbps
  - Process: 16, 7, 5nm
- SNR, BER

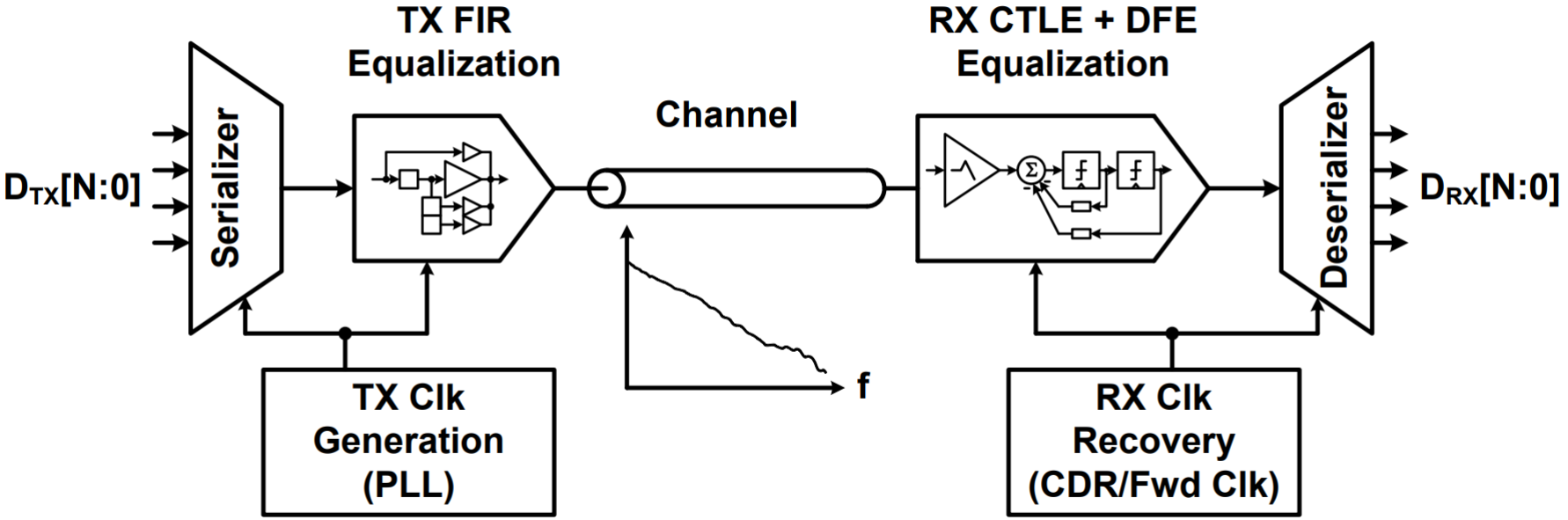
PAM4 and Interconnect Reaches

- NRZ, PAM2
- PAM4
- PAM-X

Standards using PAM4 Coding

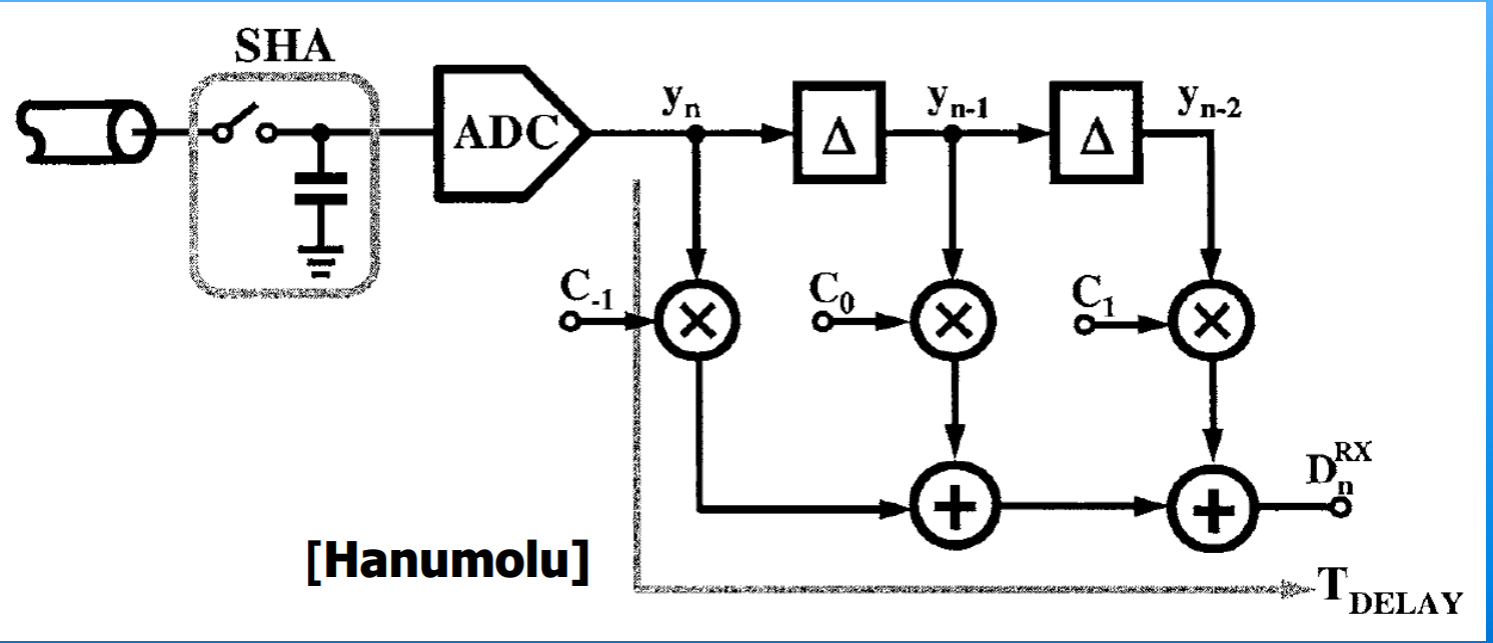
- Total data rate | Media | Number of lanes
- 10G … 400G | Cu cable/ Backplane/ Optical | 2,4,8,10

TX FIR

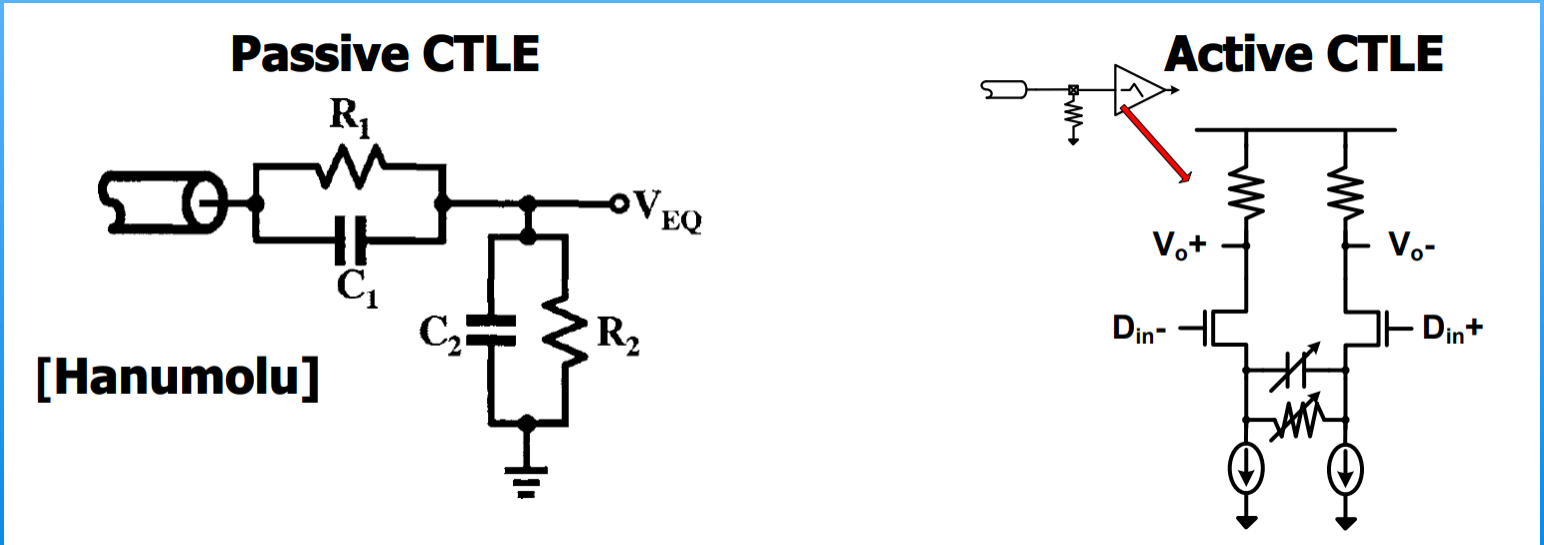

TX FIR
Equalization
RX CTLE + DFE
Equalization
Channel
D_{TX}[N:0]
Serializer
Deserializer
D_{RX}[N:0]
f
TX Clk
Generation
(PLL)
RX Clk
Recovery
(CDR/Fwd Clk)

RX FIR

- Digital RX FIR Equelizatioin



CTLE Parameter Tuning



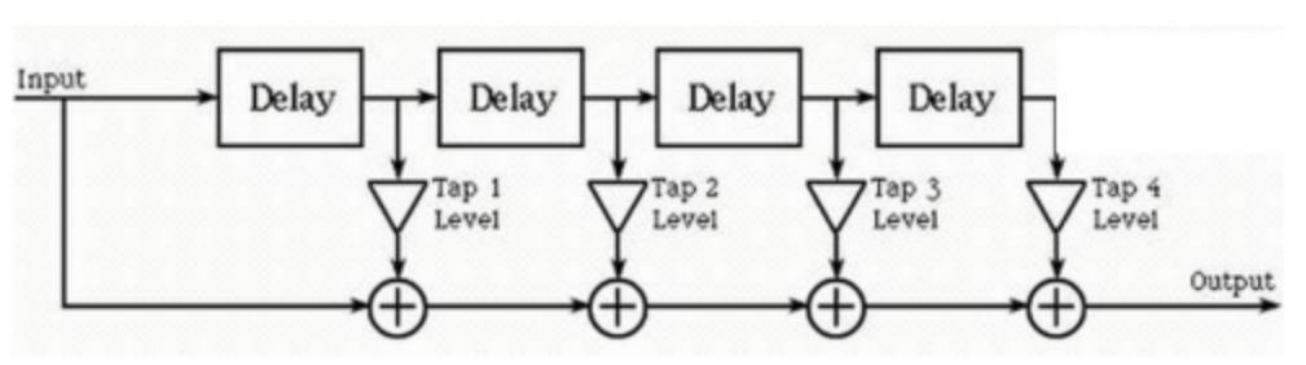
RX DFE

- Verilog-AMS, Implementation of DFE

```
//Verilog-AMS HDL for "ece546", "dfe_sampler" "verilogams"

`include "constants.vams"
`include "disciplines.vams"

module dfe_sampler (in, inbar, out, outbar, Dout, clk, rst);
input in, inbar, clk, rst;
output reg Dout;
output out, outbar;
electrical in, inbar, out, outbar;
logic clk, rst;

parameter real tap1 = 0;
parameter real tap2 = 0;
parameter real tap3 = 0;
parameter real tap4 = 0;
parameter real tap5 = 0;

reg[4:0] data_history;

analog begin
        V(out) <+ slew(V(in)+tap1*(2*data_history[0]-1)+tap2*(2*data_history[1]-1)+tap3*(2*data_history[2]-1)+tap4*
(2*data_history[3]-1)+tap5*(2*data_history[4]-1),1e11, 1e11);
        V(outbar) <+ slew(V(inbar)-tap1*(2*data_history[0]-1)-tap2*(2*data_history[1]-1)-tap3*(2*data_history[2]-1)-tap4*
(2*data_history[3]-1)-tap5*(2*data_history[4]-1),1e11, 1e11);
end

always@(posedge(clk), rst) begin

        if(rst) begin
                data_history <= 5'b00000;
                Dout <= 1'b0;
        end
        else begin
                if(V(out) - V(outbar) > 0.2)
                        Dout <= 1'b1;
                else if (V(out) - V(outbar) < -0.2)
                        Dout <= 1'b0;
                data_history[4:0] = {data_history[3:0],Dout};
        end
end

endmodule
```

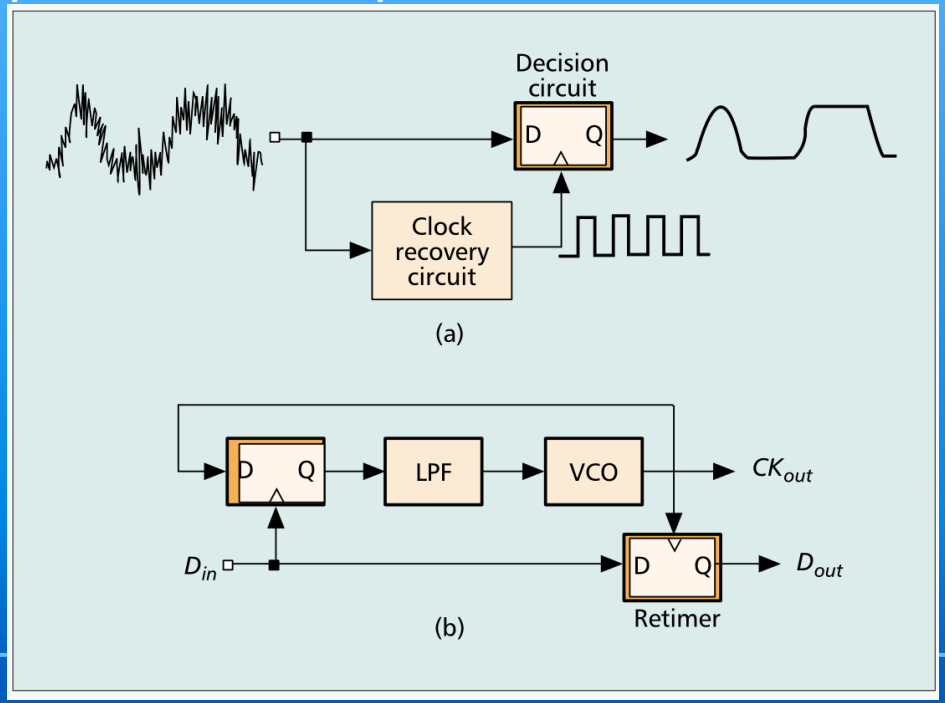
FFE

- A typical signal flow diagram for a 4-tap FFE



CDR

- a) The role of a CDR circuit in retiming data
- b) an example of CDR implementation



ADC-Based SerDes

- Intel 10nm FinFET, 112 Gbps, PAM4 ADC SerDes
- RX: LN-AFE, TI-ADC
- CDR, 7 GHz DCO
- Long reach, -35 dB Nyquist channels, FEC/EBR 1e-6

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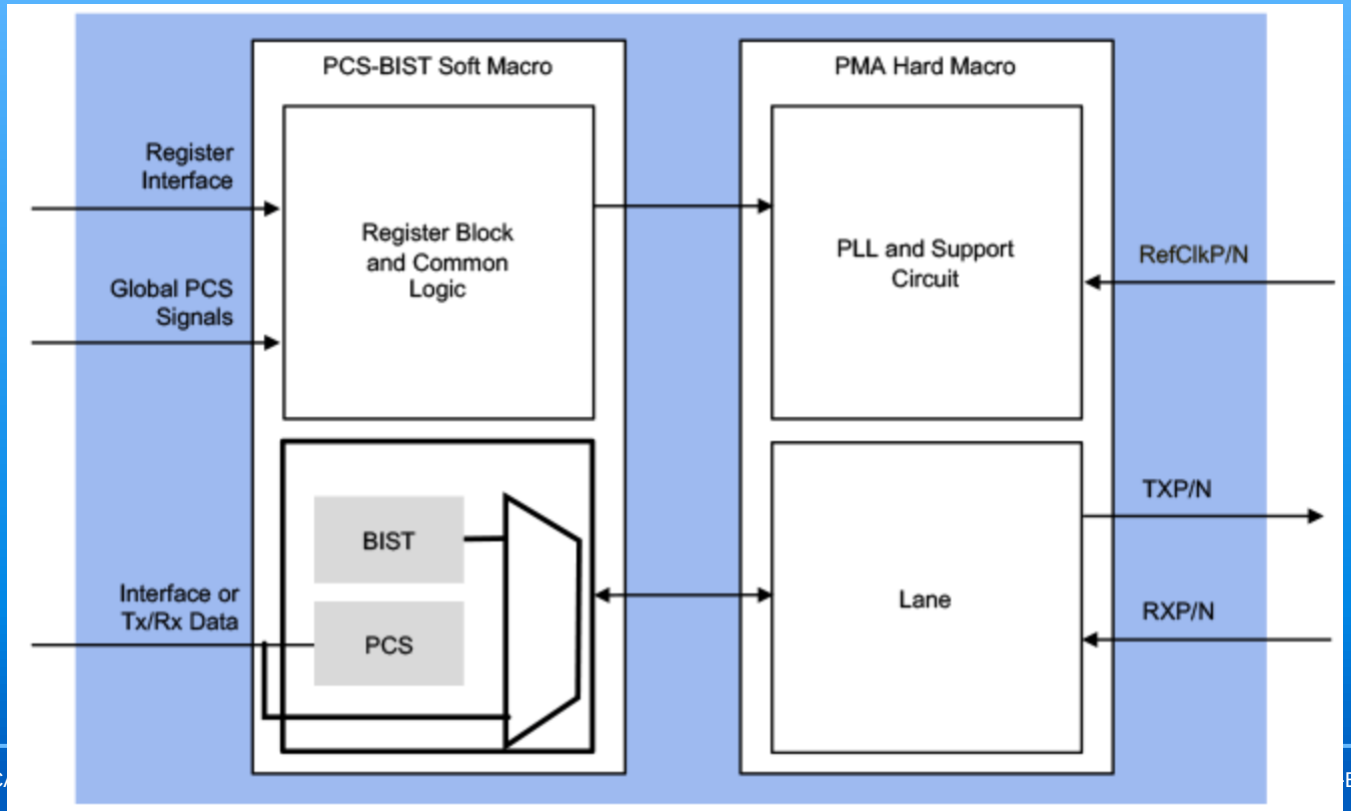
PCS of PHY, a shared IP

- PCS (TX, RX) Sublayer

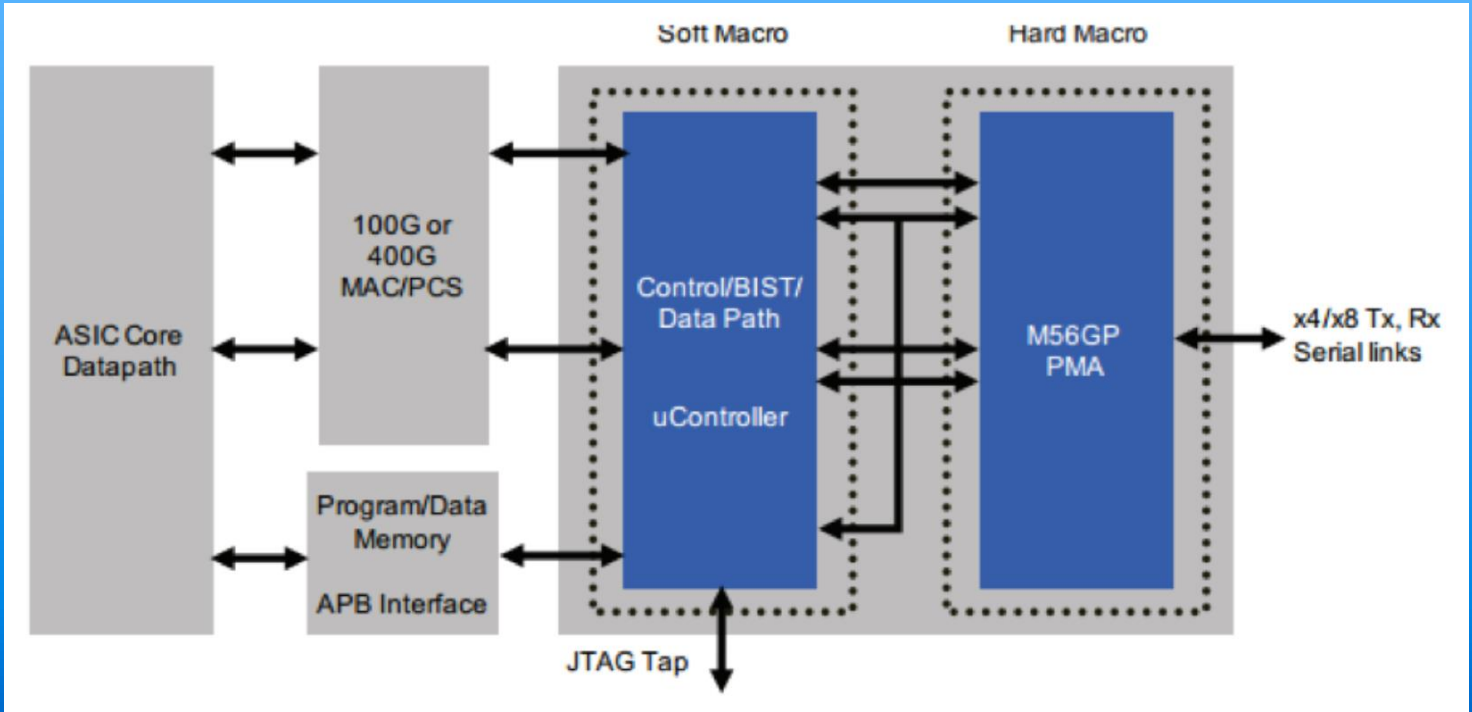
SerDes PHY

- SerDes PHY Configuration

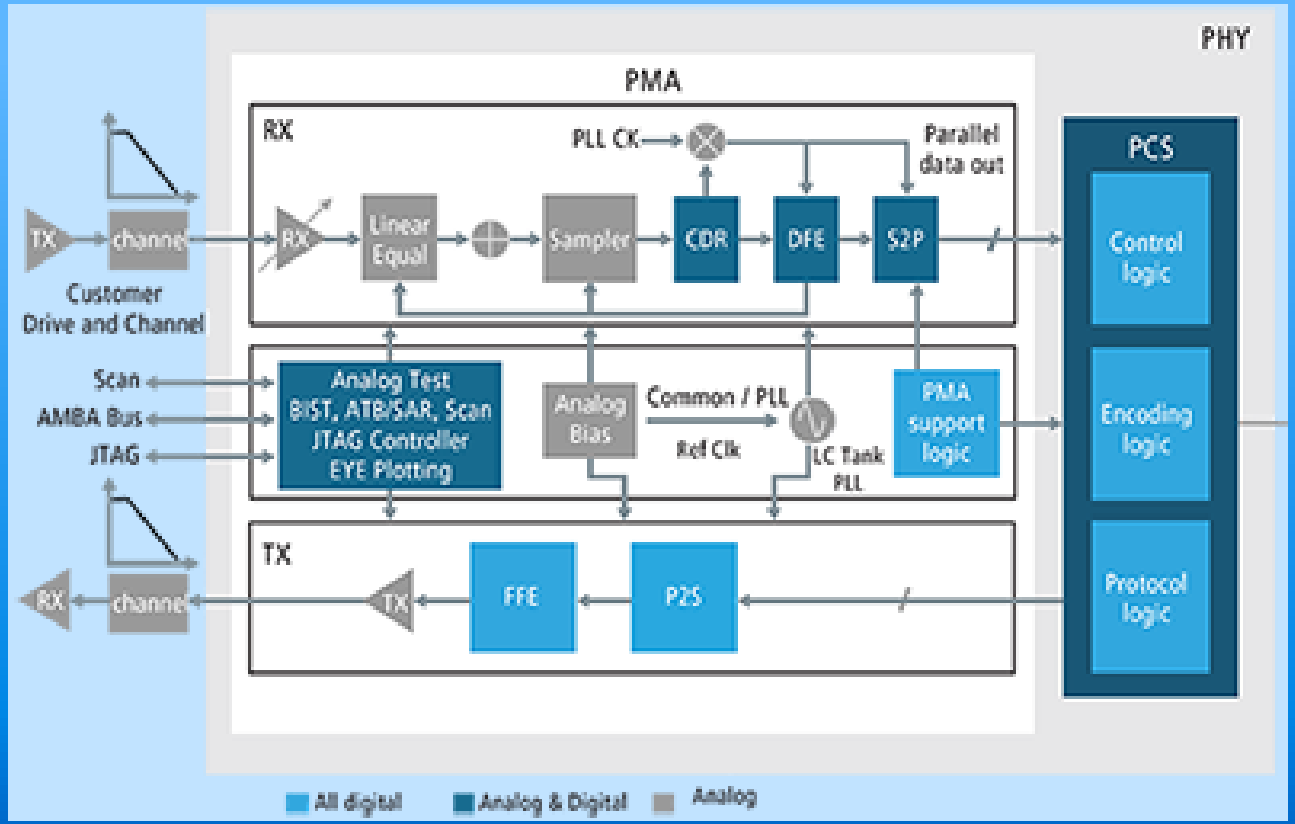


56G SerDes PHY Subsystem Example

- 56G SerDes PHY Subsystem Example



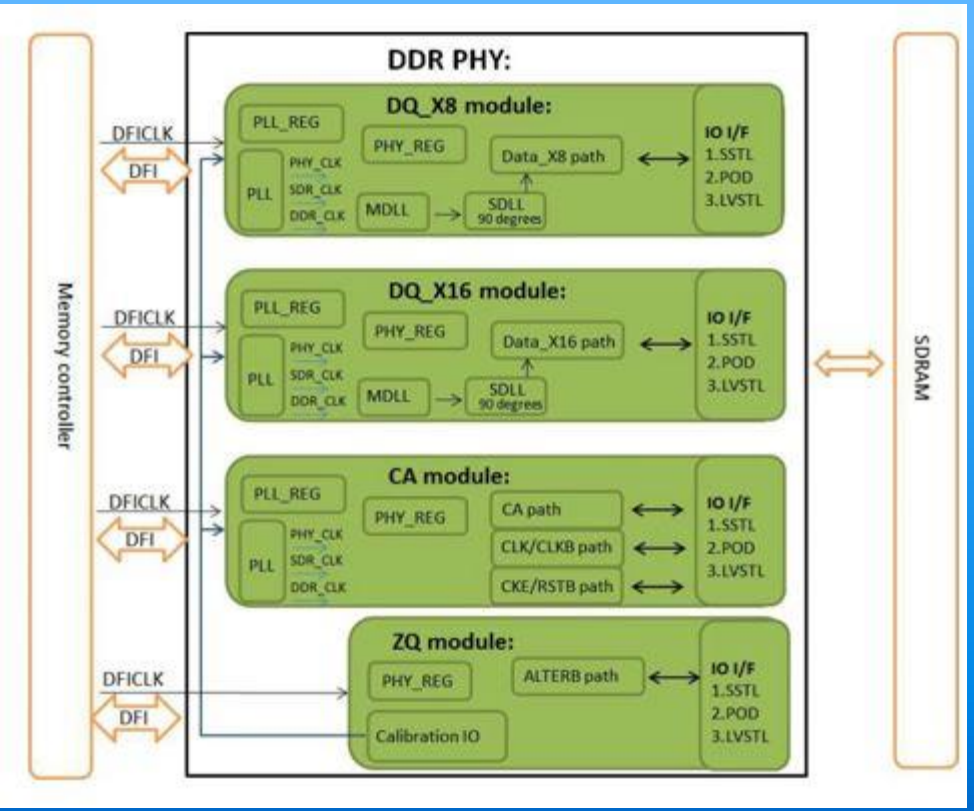
Ethernet SerDes



SerDes Designs

- Snowbush
- Alphaware 224Gbps
- CDNS, 112Gbps (w/ DFE, DSP)

DDR4/LPDDR4
Controller and PHY



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