University of Chinese Academy of Sciences

EDA in IC/IP Design

Development and Role of EDA

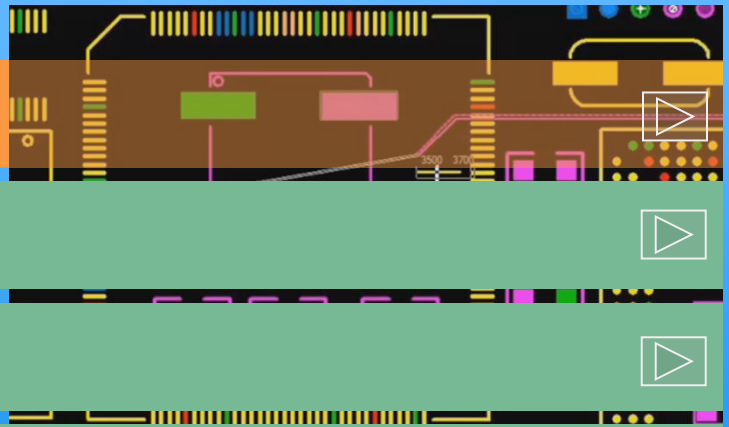
Chun-Zhang Chen, Ph.D.

June 28 – July 2, 2021

中国科学院大学2021年夏季

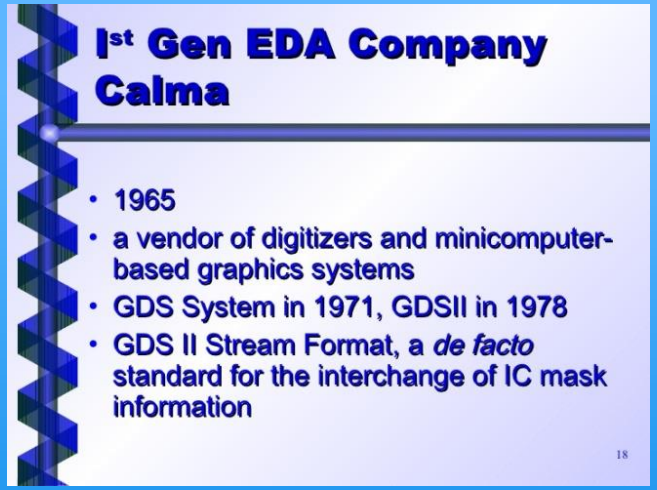
Development of EDA Industry

University of Chinese Academy of Sciences



- Invention of EDA Technology
- DAC and ICCAD
- EDA Research and Community
- Phil Kaufman Award for EDA
- Summary & Discussion

Birth of Commercial EDA



Calma (1965-1988)

- Graphics vendor, Calvin + Irma Hefte 1963/1965
- 1971 GDS, 1978 **GDS II** → UTI → GE → 1988 **Valid** → 1989 *Cadence*

EDA Ages “The Tides of EDA (2003)”

- Age of **Invention (Gods, 1964-1978)**
  - Routing, placement, STA, logic synthesis
- Age of **Implementation (Heroes, 1978-1992)**
  - Data structure, advanced algorithms
- Age of **Integration (Men, 92-03; 1992→2016)**
  - Design steps in integrated environment, cost analyzer
- *Age of **“Intelligentization” (2017-)***

Major EDA Companies

Mentor Graphics

SYNOPSYS®

cadence®

MENT

2021

In CN: 1989

(1981-)

SNPS

2021

In CN: 1995

(1986-)

CDNS

2021

In CN: 1992

(1988-)

EDA Revenue Share

Company, Yr	Market Cap	Rev 2018	Emp 2018
SNPS, 1986	$5.77B	$3.121B	12,590
CDNS, 1988	$4.46B	$2.146B	7,500
MENT, 1981	$2.33B	$1.280B	5,968
Empyrean, 2009	??	$50M	400

A Glance of EDA Industry

- Tier 1: Three Main Players
  - $6.5B, 25,000 Employees
  - Complete Design Flows
- Tier 2: Ansys, …
  - Strong in certain areas
  - Competent, 1/10 of Tier 1?
- Tier 3: Point Tools
  - Developing

EDA Ages

The tides of EDA

November 2003 · IEEE Design and Test of Computers 20(6):59 - 75

DOI: 10.1109/MDT.2003.1246165

Source · IEEE Xplore

Alberto Sangiovanni Vincentelli

- EDA Ages, **3 Eras: Gods, Heroes, Men**
  - 2003, Alberto Sangiovanni-Vincentelli: 40th EDA Keynote
- EDA for IC reviewed
  - 2006 (1st Ed.), Louis Scheffer, Luciano Lavagno and Grant Martin: "*EDA for IC Implementation, Circuit Design and Process Technology*"
- "EDA Ages" Quoted in IC Book
  - 2008, "Physical Implementation of Digital IC" (C.-Z. Chen *et al.*)
- EDA Ages of **3 I's** proposed
  - **Invention (64-78), Implementation (78-92), Integration (92-16?)**
  - 2016 (2nd Ed), Luciano Lavagno et al. Elec. Design Auto. for IC Sys.

EDA for IC Implementation, Circuit Design and Process Technology (2nd Ed., 2016)

(EDA for ICs Handbook, pp1472, CRC Press**)**

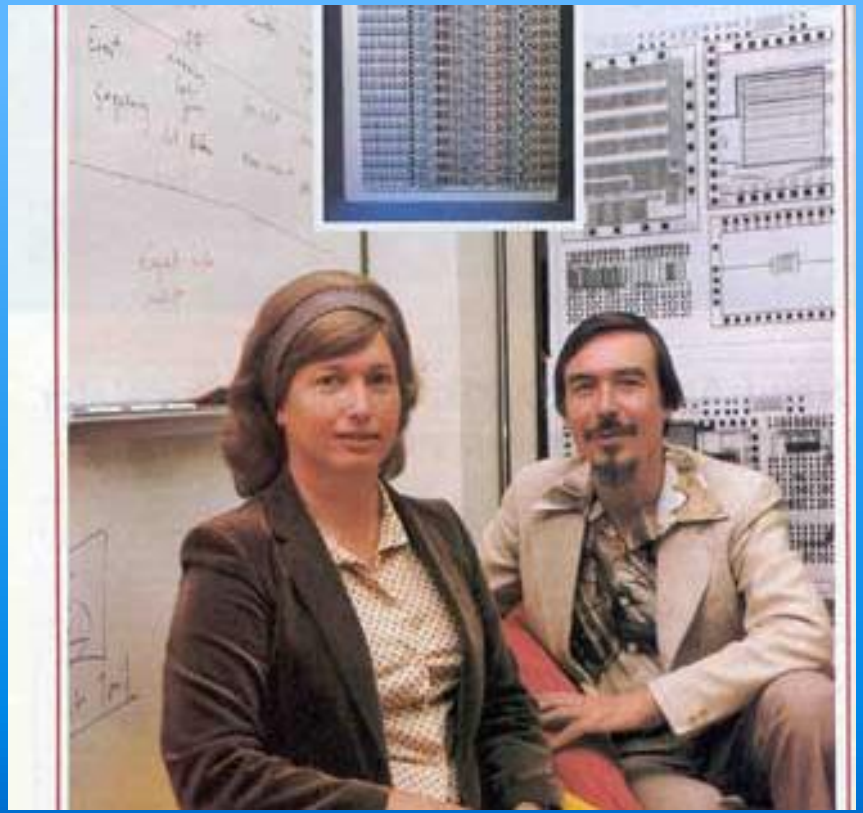
Luciano Lavagno, Grant Martin, Igor L. Markov, Louis K Scheffer

- Pt I: **RTL to GDSII**, or Synthesis, Place and Route (16 ch.)
- Pt II: Analog and Mixed-Signal Design (3 ch.)
- Pt III: Physical Verification (7 ch.)
- Pt IV: Technology Computer-Aided Design (TCAD, 3 ch.)

(*Louis K Scheffer, Luciano Lavagno, Grant Martin*, 1st Ed, 2006)

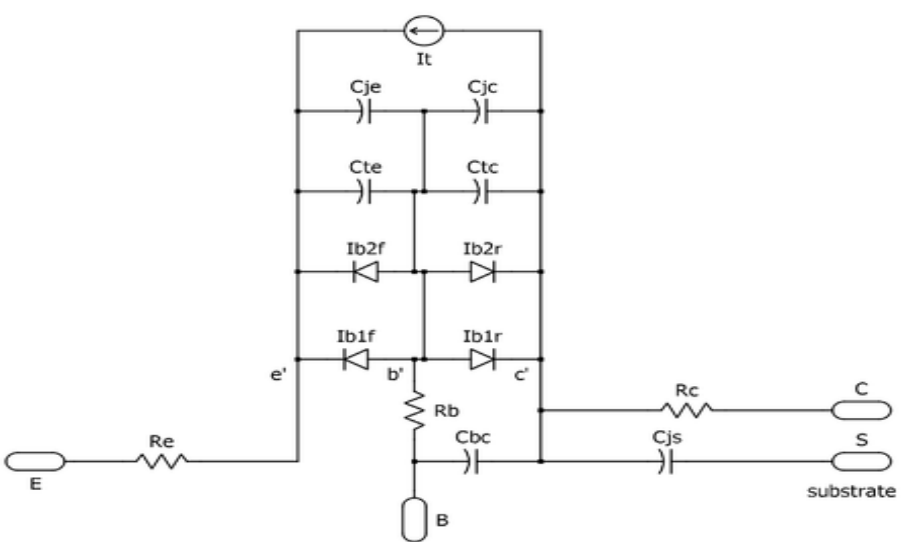
“Introduction to VLSI System”

Mead & Conway revolution



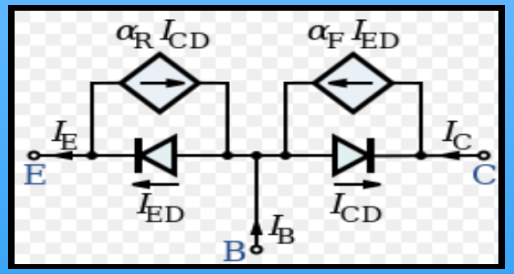
- 1980 Book by Carver Mead and Lynn Conway
- 1981 Electronics Award for Achievement
  - A *de facto* standard course material, used at >100 universities globally

Gummel–Poon Model (BJT, 1970)
Ebers-Moll Model (BJT, 1954, 1987)

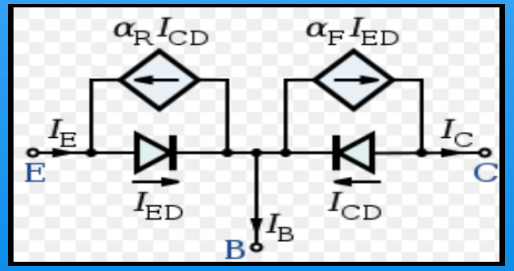


Schematic of SPICE Gummel-Poon Model NPN

G-P model: good physics; simple math; high resolution



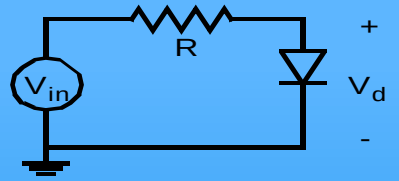
Ebers–Moll Model for an NPN transistor.



Ebers–Moll Model for an PNP transistor.

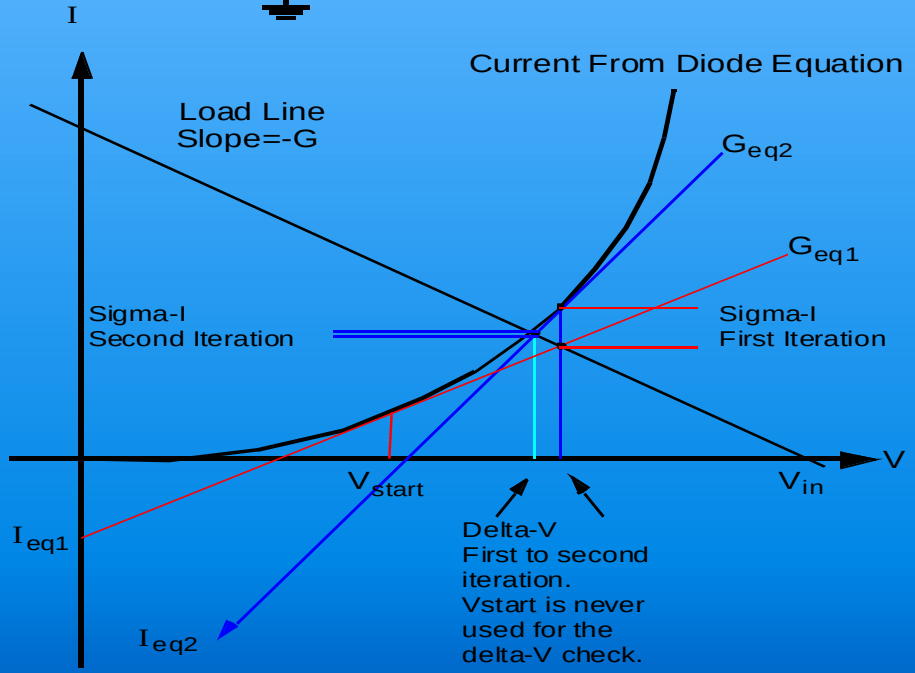
E-M model: EM1,EM2,EM3. More Complex, for big DC signal

Understanding the Newton-Raphson Iteration Method



Diode Equation

$Id = Is\ (e^{Vd/n*Vt} - 1)$



To accurately represent the tangent, both the slope (G_{eq}) and the intercept (I_{eq}) are needed. This preserves the diode terminal characteristics at only the point where the tangent is taken. The device current and the tangent are supplied by the device model.

On the third iteration, delta-V and sigma-I would be very small, and the linear solution would be very close to the nonlinear solution.

CANCER and SPICE

1970, CANCER
Computer Analysis of Nonlinear Circuits, Excluding Radiation
1971, SPICE
Simulation Program with Integrated Circuit Emphasis

Laurence Nagel, Ron Rohrer, Don Peterson

SPICE and BSIM from UCB (2008-2015)

- SPICE1 (Laurence Nagel/Prof. Donald Pederson, 1973, UCB, Fortran)
- SPICE2 (Stable release, 1975, Fortran)
- SPICE3 (Thomas Quarles/Prof. A. Richard Newton, 1989, C)
- **BSIM3 (BSIM3v3), for DSM**
- **BSIM4**, used for 0.13um, 90nm, 65nm,
  - **extended to 45/40nm, 23/28nm and 22/20nm**
- BSIM-BULK (**BSIM6**), for RF
- **BSIM-SOI**, based on BSIM3, used by IBM, AMD
- **BSIM-CMG**, for common multi-gate or FinFET
- BSIM-IMG, for independent multi-gate, the latest
  - ex. ind. double-gate (ultra-thin body) & BOS SOI transistors (UTBB)

Variants of SPICE

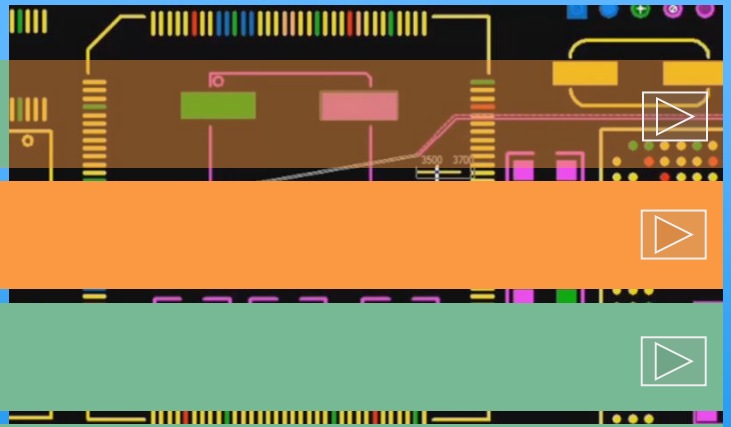
- SPICE [1971, UCB; 1970 CANCER]
- HSPICE [1981 Meta-SW, 1996 *Avant!*, 2001 Synopsys]
  - NanoSim, HSIM [SNPS]
- Spectre/SpectreRF [Cadence]
- NanoSPICE, GigaSPICE [ProPlus]
- FastSPICE [Silvaco]

Generations of SPICE Simulator

表2-7 SPICE特征与模型的应用范围 (2008)

SPICE Level	年代	模型特征	应用范围
第一代 SPICE Level 1	1968	Shichman-Hodges模型(电流-电压平方率特性)	适用于精度要求不高的长沟道MOS晶体管
SPICE Level 2	1970	二维解析模型(考虑MOS器件二阶效应), Gummel-Poon模型	适用于BJT
SPICE Level 3	1979	半经验短沟道模型	适用于MOS晶体管，>0.9 um
第二代 SPICE Level 28, BSIM1	1987	半经验式，适合DSM设计的(短沟道)模型	适用于数字和模拟设计，0.3—0.5 um
SPICE Level 39, BSIM2	1989	半经验式，适合DSM设计的模型	适用于MOS晶体管，> 0.2 um
第三代 SPICE Level 49, BSIM3v3	1995	S/D 电阻, W/L	适用于MOS晶体管，0.18 um
BSIM4v6	2001	考虑到栅极泄漏, 非对称S/D电流分布	适用于130 nm，90 nm，65 nm
PSP Model	2006	表面电势模型	适用于 90 nm，65 nm，45 nm

Development of EDA Industry



- Invention of EDA Technology
- DAC and ICCAD
- EDA Research and Community
- Phil Kaufman Award for EDA
- Summary & Discussion

57th DAC 2020, July 20-24
2020 EDA Topics

- **SEMICONDUCTOR TECHNOLOGY: A SYSTEM PERSPECTIVE**
- **TUTORIAL 2: EDA IN THE CLOUD – BEST PRACTICES FOR CLOUD MIGRATION**
- **TUTORIAL 3: PREVENT CLOCK DOMAIN CROSSINGS FROM BREAKING YOUR CHIP**
- **TUTORIAL 6: SYSTEM LEVEL POWER ANALYSIS WITH UNIFIED POWER MODELS**
- **DESIGN-ON-CLOUD PAVILION:**
  - **AWS, CDNS, MENTOR, NETAPP, PURE STORAGE…**
- 58th DAC 2021, Dec. 5-9, Moscone Center, San Francisco

57th DAC 2020 July 20-24

2020 Best Paper/Presentation Recipients

- **BEST PAPER RESEARCH: Algorithm-Hardware Co-Design of Adaptive Floating-Point Encodings for Resilient Deep Learning Inference.** Thierry Tambe, Harvard University, Cambridge, MA
- **BEST PAPER DESIGNER TRACK FRONT-END: Easy Deadlock Verification and Debug with Advanced Formal Verification.** Laurent Arditi - Arm, Ltd., Valbonne, France
- **BEST PAPER DESIGNER TRACK – BACK-END: A CPU Power Distribution Network Optimization Method Considering Routing Congestion with Genetic Algorithm.** Huajun Wen - MediaTek, Inc., Austin, TX
- **BEST PAPER – IP TRACK: PCI Gen4 Channel Optimization Using Machine Learning.** Wook Kim - Samsung Electronics Co., Ltd., Hwaseong, R. of Korea
- **BEST PAPER – EMBEDDED SYSTEMS TRACK: The Path Towards Battery-Free and Forever-Battery Life for Internet of Things.** Masoud Zargari - Atmosic Technologies, Campbell, CA

39th ICCAD Nov 2-5, 2020

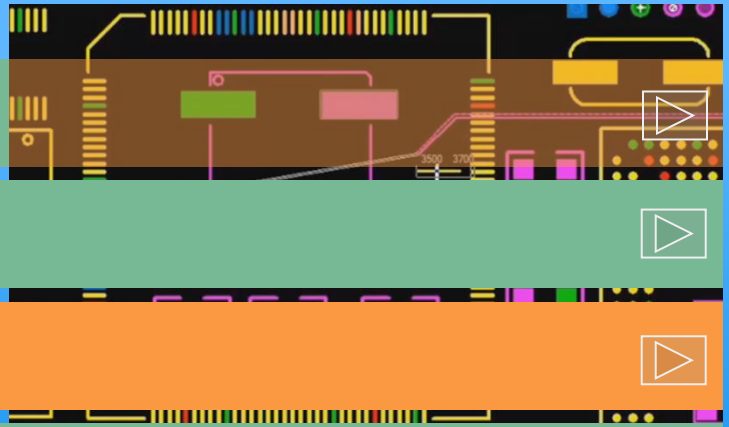
Virtual Conference

2020 International Conference On Computer Aided Design

The Premier Conference Devoted to Technical Innovations in Electronic Design Automation

- **Keynote**: Engineering the Future of AI for the Enterprises
- 1A: Routing Strategies for 2D/2.5/3D Ics
- 1B: Electromigration and Circuit Yield: Efficient Verification Techniques
- 1C: Securing Embedded and IoT Platforms
- 1D: How Machine Leaning can Reshape Technology, Manufacturability, Performance and Power
- 2A: Machining Learning Techniques for Routing and Hotspot Detection
- 2B: Exploring Optimal Mask Patterns
- 2C: Safety and Energy Optimizations for Cyber-Physical Systems
- 2D: AIoT: The Powerful Convergence of AI and the IoT – An Industrial Perspective
- 3A: Brain-inspired, Bio-engineering, and Emerging Computing
- 3B: Novel Techniques for Improving Reliability and Manufacturability
- 3C: Secure Architectures and Systems Design
- 3D: Hardware/Software Co-Design for Machine Learning in Medicine

Development of EDA Industry



ISSCC

- **The ISSCC 2021 Conference Theme is "INTEGRATED INTELLIGENCE IS THE FUTURE OF SYSTEMS"**
  - ANALOG
  - DATA CONVERTERS
  - DIGITAL CIRCUITS and ARCHITECTURES & SYSTEMS*
  - IMAGERS, MEMS, MEDICAL, & DISPLAYS
  - MACHINE LEARNING and AI
  - MEMORY
  - POWER MANAGEMENT
  - RF CIRCUITS and WIRELESS SYSTEMS**
  - TECHNOLOGY DIRECTIONS
  - WIRELINE

International Electron Devices Meeting

- IEDM, since 1955
- *Topics of Interest (2020)*
  - ADVANCED LOGIC TECHNOLOGY (ALT)
  - EMERGING DEVICE and COMPUTE TECHNOLOGY (EDT)
  - MEMORY TECHNOLOGY (MT)
  - MICROWAVE, MILLIMETER WAVE and ANALOG TECHNOLOGY (MAT)
  - MODELING and SIMULATION (MS)
  - OPTOELECTRONICS, DISPLAYS, and IMAGING SYSTEMS (ODI)
  - POWER DEVICES and SYSTEMS (PDS)
  - RELIABILITY OF SYSTEMS and DEVICES (RSD)
  - SENSORS, MEMS, and BIOELECTRONICS (SMB)

DesignCon (since Jan. 1995)

DESIGNCON 2021
HOST SPONSOR KEYSIGHT TECHNOLOGIES

DesignCon 2020 Tracks

Conference sessions cover all aspects of **hardware design**, including

signal & power integrity,

high-speed serial design, and

machine learning.

11. Electromagnetic Compatibility/Mitigating Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

DVCon (1995, OVI)

DVcon 2020 Design and Verification

March 2-5, 2020. DoubleTree Hotel, San Jose, CA

Stu Sutherland BEST PAPER AWARDS

1st Place: *UVM Reactive Stimulus Techniques*
2nd Place: *UVM - Stop Hitting Your Brother Coding Guidelines*
3rd Place: *A SystemVerilog Framework for Efficient Randomization of Images With Complex Inter-Pixel Dependencies*

Stu Sutherland BEST Posters AWARDS

1ST Place: *SoC Firmware Debugging Tracer in Emulation Platform*
2nd Place: *Deadlock Verification For Dummies - The Easy Way Using SVA and Formal*
3rd Place: *Addressing the Challenges of Generically Specifying Power Intent with Multi-Rail Macros*

SEMI/ CSTIC

- **Topics to be addressed at CSTIC 2021 include, but are not limited to, the following:**
  - Symposium I: Device Engineering and Memory Technology
  - Symposium II: Lithography and Patterning
  - Symposium III: Dry & Wet Etch and Cleaning
  - Symposium IV: Thin Film, Plating and Process Integration
  - Symposium V: CMP and Post-Polish Cleaning
  - Symposium VI: Metrology, Reliability and Testing
  - Symposium VII: Packaging and Assembly
  - Symposium VIII: MEMS, Sensors and Emerging Semiconductor Technologies
  - Symposium IX: Design and Automation of Circuits and Systems

Accellera - D&V Standards

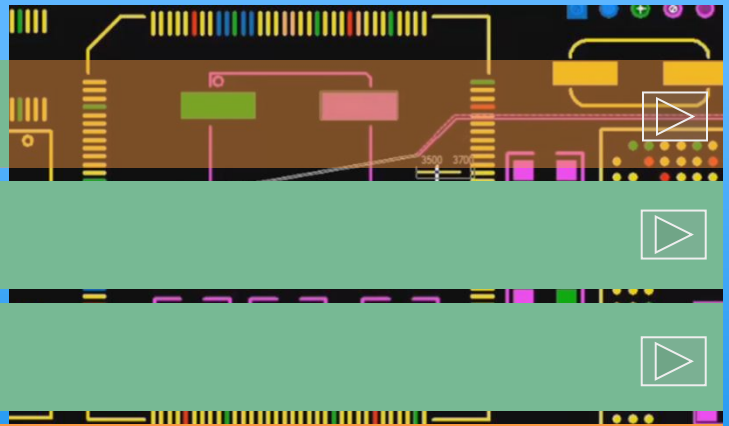
- Accellera Standards Success
  - Since 2004
- The Accellera Ecosystem
  - System/Design, Verification, Integration - Infrastructure
- Accellera Structure
  - Program Committee, Technical Committee, Administration
- Acronyms and Definitions

2020 Global Sponsors

Technical Organizations

- JEDEC (1958-), 300 members
  - Focus areas: Main memory (DDR4/5), Flash (SSDs, UFS, eMMC), Mobile memory (LPDDR, Wide I/O, Memory MCP), Memory Module Design File Registrations (DIMMs), JEP30, JEP95 (solid state devices), JESD21-C (solid state memories), Lead-Free Manuf., ESD. Web: https://www.jedec.org/
- PCI-SIG, 700+ members
  - PCIe I/O standard, http://pcisig.com/
- Wi-Fi Alliance (1999-, Austin, TX), 600+ members
  - Web: https://www.wi-fi.org/
- USB-IF (1995-, Beaverton, OR), 1000+ member companies
  - https://www.usb.org/members
- SDA (2001-, San Ramon, CA), 900 members
  - SD standard, miniSD/SDHC, microSD, https://www.sdcard.org/

Development of EDA Industry



- Invention of EDA Technology
- DAC and ICCAD
- EDA Research and Community
- **Phil Kaufman Award for EDA**
- Summary & Discussion

Phil Kaufman and Phil Kaufman Award

- Phil A. Kaufman (1942-1992)
  - president and CEO of Quickturn Systems
    - *Quickturn acq'd PiE Design Systems (Paul Huang) in 1993*
    - *Quickturn was IPO'ed on 11/04/93, acq. By CDN 12/10/98*
  - ex-chief of Silicon Compiler Systems
    - *Acq'd by MENT on 1/1/90*
- Phil Kaufman Award (annual since 1994)
  - Established by ESD Alliance (previously EDA Consortium)

ESD Alliance

- *ESD Alliance (2016-)*
  - **ESD Alliance,** 673 South Milpitas Blvd., Milpitas, CA 95035
  - Resource Center
    - Past event recordings (audios, videos, photos)
    - ESD Alliance Newsletter
    - MSS (Market Statistics Service) Newsletter (Quarterly)
- *EDA Consortium (1989-2015)*

"The Nobel Prize of the EDA Industry" (1/3)

Phil Kaufman Award

Electronic System Design Alliance

- **2003: Richard Newton,** UCB – SPICE, Dean of College Engineering
- **2002: Ron Roher,** Magma/Nonlinear –
  - pioneer, educator, circuit simulation [1970 CANCER→] SPICE Program
- **2001: Alberto Sangiovanni-Vincentelli,** UCB –
  - circuit simulation, CAD of IC, 560 papers, 15 books
- **2000: Dr. Yen-Son (Paul) Huang,** Novas, inventor' of Dracula, ECAD, Emulation
- **1999: Dr. Hugo De Man,** Katholieke U./IMEC (Leuven) –
  - Circuit & system, CAD-EDA, DSP station
- **1998: Dr. Ernest S. Kuh,** UCB – pillar of EDA, students, P&R algorithm
- **1997: James E. Solomon,** UCB – early CAD tools, SDA: CE & Framework
- **1996: Dr. Carver A. Mead,** Caltech – dielectrics to scaling theory
- **1995: Dr. Donald O. Pederson,** UCB – 1971 SPICE, algorithm and ideas
- **1994: Dr. Hermann K. Gummel,** Bell Lab – Gummel-Poon Model

"The Nobel Prize of the EDA Industry" (2/3)

Phil Kaufman Award

Electronic System Design Alliance

- **2013: Chenming Calvin Hu,** UCB – FinFET, 2015 Nat Medal Tech & Inno.
- *2012: (event merged with "50th DAC 2013")*
- **2011: Chung Laung Liu,** MIT, UIUC –
  - tech, leadership skills, biz acumen in EDA
- **2010: Pat Pistill,** DAC – pioneering EDA, DAC showcase
- **2009: Randal Bryant,** CMU – formal verification
- **2008: Aart de Geus,** Synopsys CEO – EDA/DC
- **2007: Robert K. Brayton,** UCB – logic synthesis, formal, verif./equiv. checking
- **2006: Robert Dutton,** Stanford – SUPREM, PISCES simulation in TCAD
- **2005: Phil Moorby,** Gateway –
  - inventor: Verilog HDL, Simulator Verilog-XL, SystemVerilog/VCS
- **2004: Joe Costello,** Cadence ex-CEO –
  - top 10 S/W Company, batch of DRC, NC-Verilog

"The Nobel Prize of the EDA Industry" (3/3)

Phil Kaufman Award

Electronic System Design Alliance

- **2021**: nomination due June 30, 2021!
- 2020: cancelled due to COVID-19 pandemic
- 2019**: Dr. Mary Jane Irwin**, Penn State U,
- **2018: Dr. Thomas W. Williams,** IBM/Synopsys –
  - Level Sensitive Scan Design (LSSD/DFT)
- **2017: Dr. Rob A. Rutenbar,** UIUC – Analog and MS algorithm
- **2016: Dr. Andrzej Strojwas,** CMU – IC manuf. and yield, CTO of PDF
- **2015: Dr. Walden C. Rhines,** Mentor CEO –
  - efforts of growing EDA /IC industries
- **2014: Dr. Lucio Lanza,** Lanza techVentures – vision, mentoring & financial
  - support on EDA/IP tech, leadership skills, biz acumen in EDA

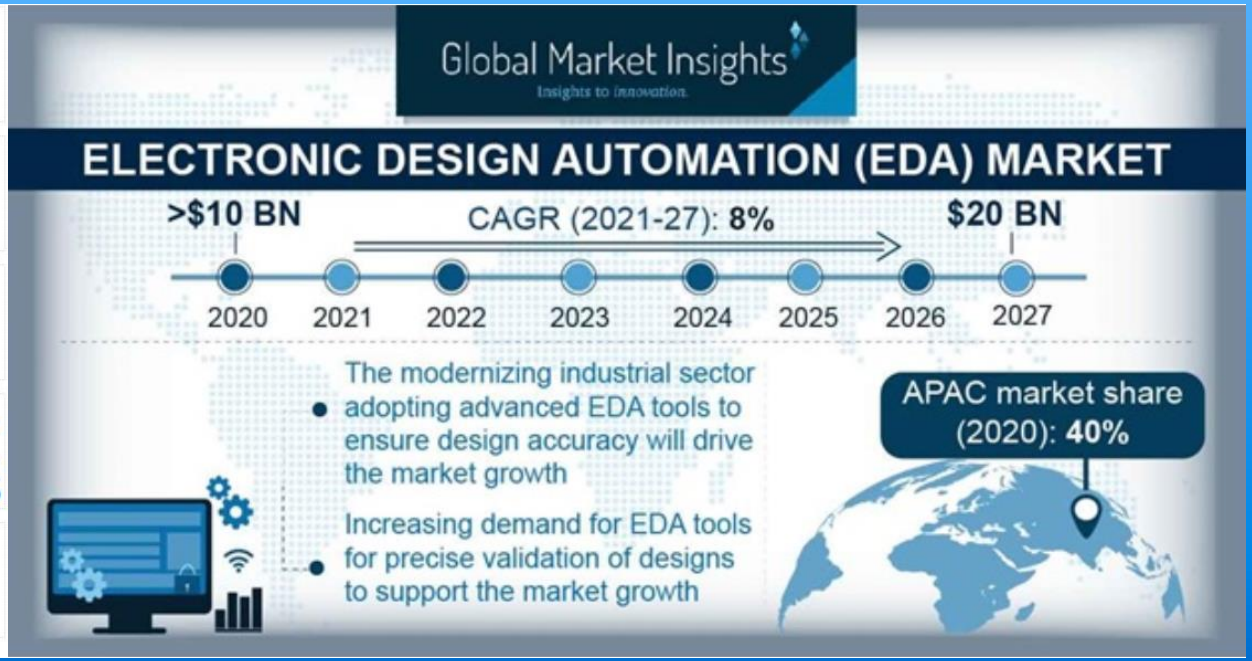
Abstract from EDA Awards

- **SPICE and Circuit**
  - SPICE, algorithm
  - Circuit Simulation
  - *CE and Framework*
- **Verification**
  - DRC, NC, Verilog HDL
  - SystemVerilog/VCS
  - Synthesis, Formal, LEC
- **Methodology and Flow**
  - FinFET – Gummel-Poon
    - Moore's Law
  - Analog-MS Algorithm
  - LSSD/DFT
- **Platform/GUI**
  - Scripts & Environment
  - Database

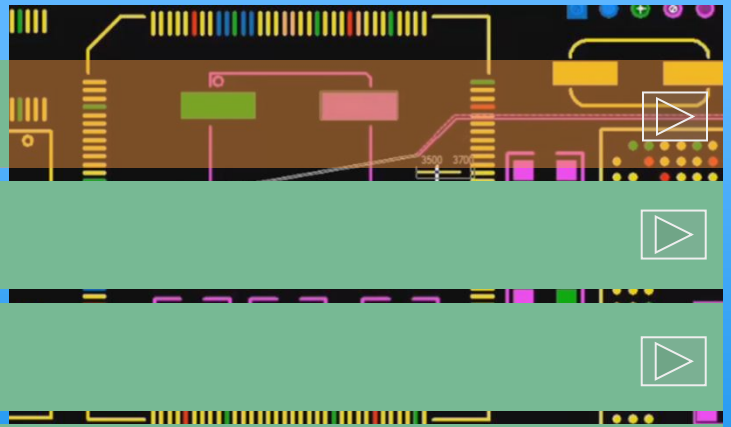
The Role of EDA in AI

- EDA for Semiconductor Engineering

SIEMENS cadence SYNOPSYS ALDEC codasip vtool smart verification onespin assuring IC integrity Valtrix SYSTEMS Si Silicon Integration Initiative, Inc. imperas



Development of EDA Industry



- Invention of EDA Technology
- DAC and ICCAD
- EDA Research and Community
- Phil Kaufman Award for EDA
- Summary & Discussion

Levels of Design and Verification

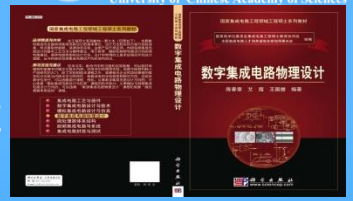
- Level of Design
  - HLS (C-to-S)
    - C/C++, SystemC, …
  - Logic synthesis (RTL)
  - Schematic capture (CDL)
  - Layout (GDS II)
- Simulation
  - Transistor level
  - Logic level
  - Behavioral simulation
  - Emulation (ICE)
  - Technology CAD
  - EM filed solvers

Summary & Discussion

Verification and Analysis

- Analysis & Verification
  - Functional verification
  - CDC
  - Formal (modeling)
  - Equivalence checking
  - STA
  - Physical (DRC and LVS)
- DFM
  - Mask data prep (MDP)
    - RET, OPC, Mask Generation
    - DFT: ATPG, BIST
- Functional Safety
  - Safety analysis
  - Safety synthesis
  - Safety verification

Partial List: Data File Formats



- Circuit or FE dominant
  - Schematic: .sch,
  - Symbol: .sym,
  - Circuit: .edif,
  - SPICE: .sp,
  - Timing: .lib [.tlf/.ctlf, TLF/CTLF],
  - Verilog: .v,
  - Gate-Level Netlist: .gln,
  - Std. Design Constraints: .sdc,
  - Value Change Dump; .vcd,
  - ATPG Test: .wgl
- Physical or BE dominant
  - Layout: .lay,
  - GDSII: .gds,
  - Design Exchange Format: .def,
  - Library Exchange Format: .lef,
  - Std. Parasitic Exchange Format: .spef [.dspf, .rspf, .spf],
  - Standard Delay Format: .sdf,
  - Toggle Change Format: .tcf,
  - Timing Window Format: .twf,
  - Common Power Format: .cpf,