University of Chinese Academy of Sciences

EDA Methodology and IC Design

IC Design Flows

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SoC Design Flow

Applications

Big Data

iCloud

AI/ML

5G/ IoT

IC Design Flows

S1	D1	C1	P1
S2	D2	C2	P2

DESIGN VERIFICATION

DFX

Design for Test

Design for Manufacturing

Design for Yield

Design for Reliability

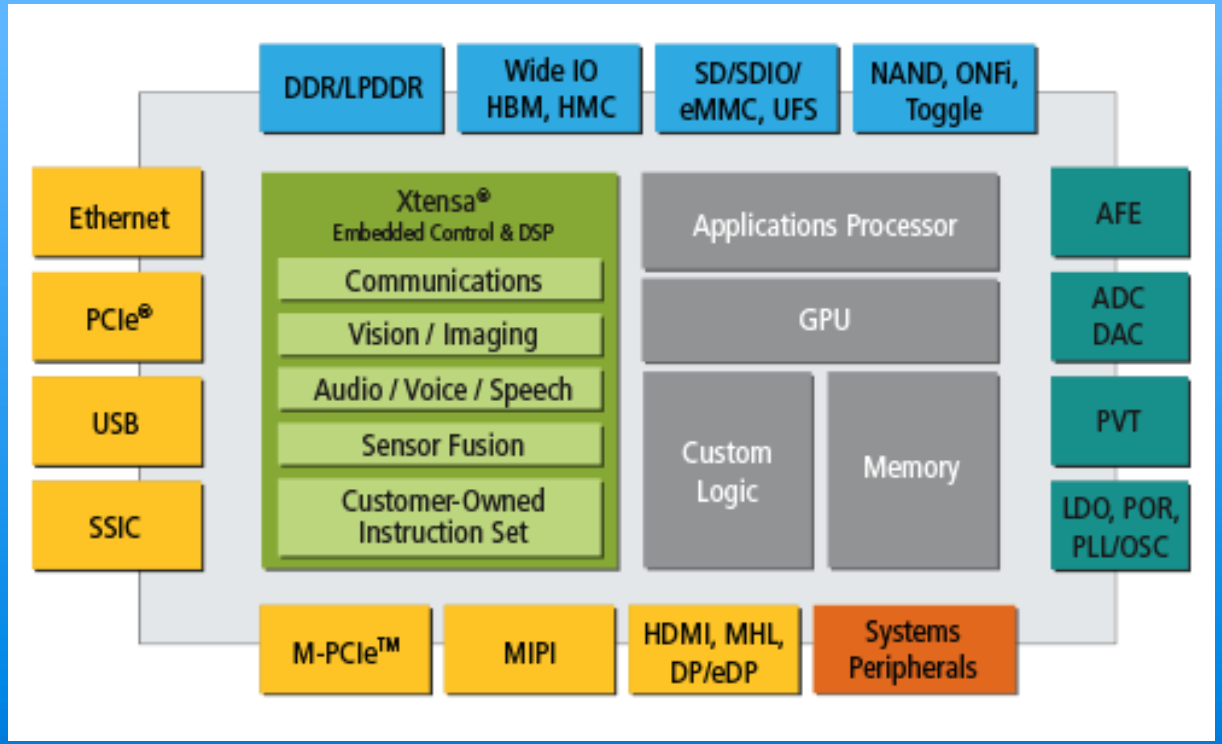
TAPE-OUT TO FOUNDRY

AI to Chip vs System/RTL to Chip

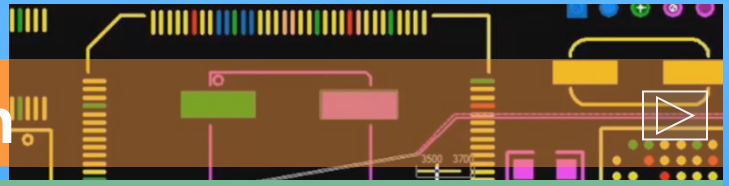
- RTL-to-GDSII (R2G)
- System to Chip (C-to-Silicon, C2S)
  - High-Level Synthesis
- ML deployment from Cloud to Edge to End Node
  - Cloud (CC/IMP) to Edge (EC) to End Node (IMC)
  - For Edge-AI (python script or pull-down menu) to become a mainstream reality
  - Software 2.0, to utilize CNN/ML libraries in SW (which determines weights and parameters, or training models)

Defining a SoC Design

- CPU
  - GPU/DSP
  - AP/MCU
- Custom Logic
- COT Block
- I/Os
- IPs
  - Memory IP



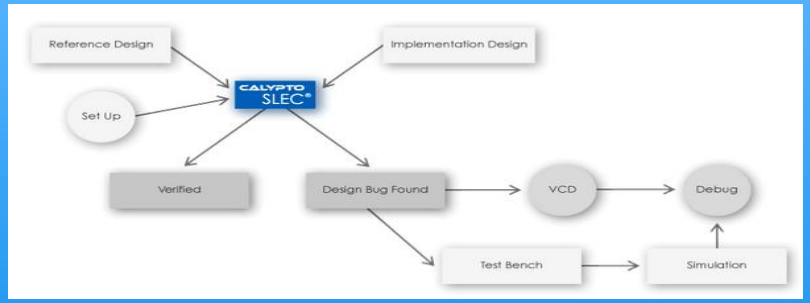
EDA and IC Design

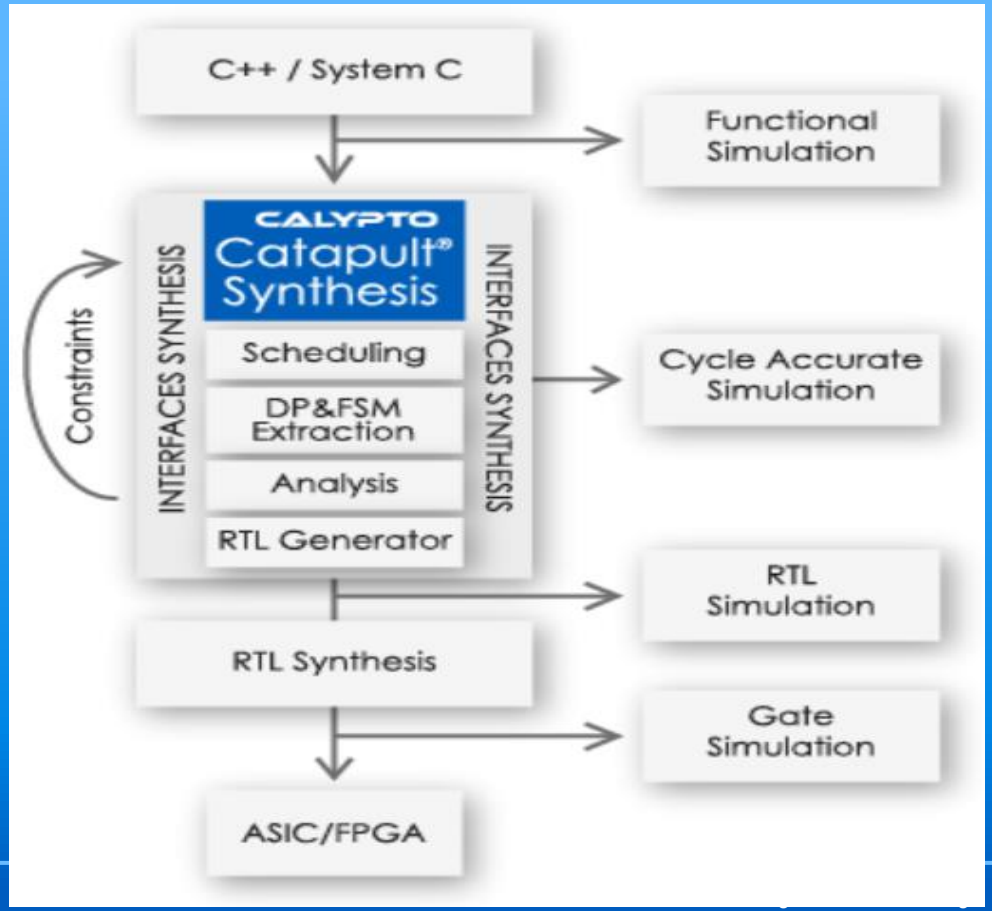


- System Design and IP Integration
- Digital IC Design and Implementation
- Analog MS Design and Simulation
- Packaging and PCB Design
- Summary

ESL and High Level Synthesis

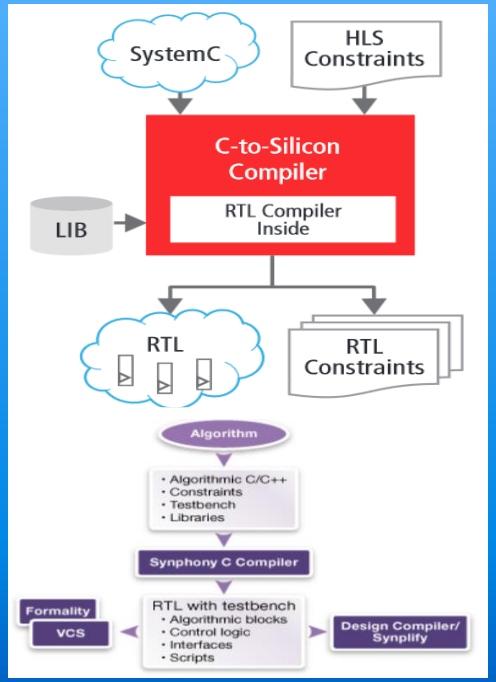
- **Catapult C [M→ Calypto]**

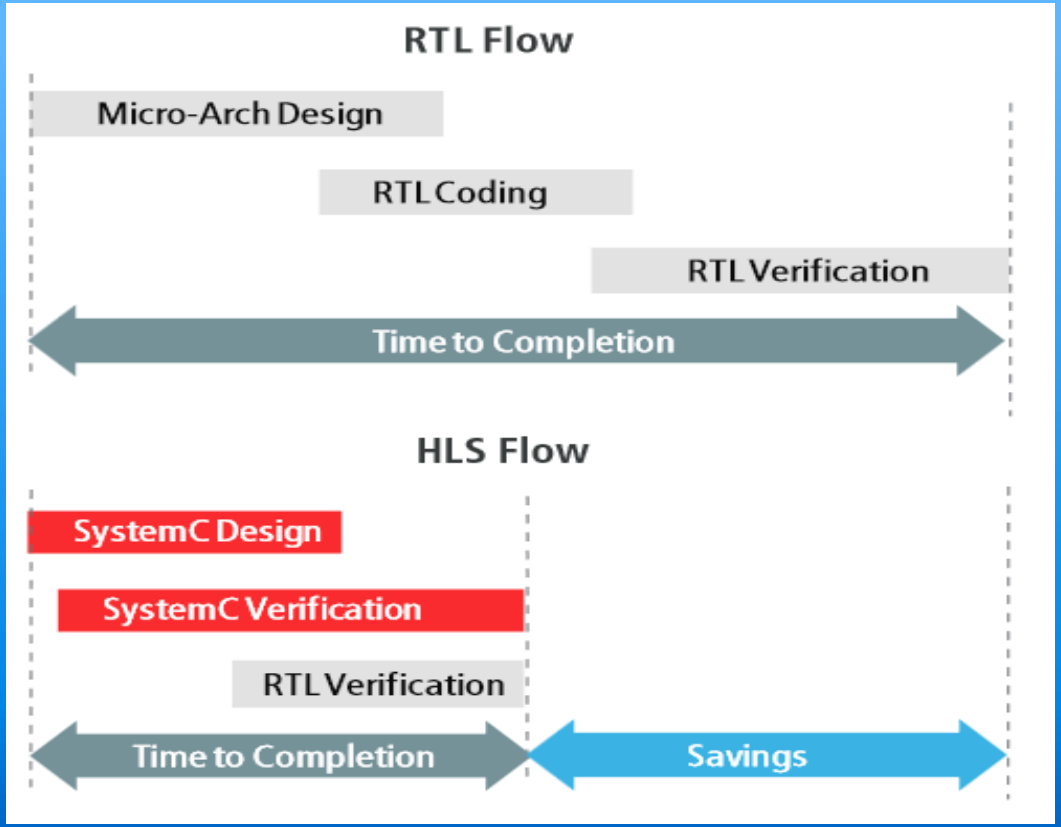




High Level Synthesis (HLS)

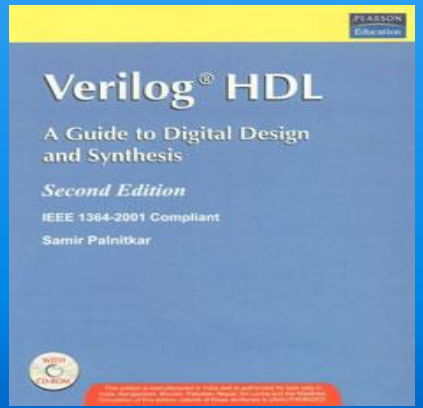
- Catapult C Synthesis from MENT
- C2Silicon from CDNS
- C-Compiler from SNPS





Verilog Description

```
/* ----- Programmable 4-bit up/down counter ----- */
MODULE COUNTER (COUNTIN: IN, UP: IN, COUNT: IN,
                COUNTOUT: OUT);
EXTERNAL COUNTER;
  DCL COUNTIN  BIT(4), /* programming input  */
      UP       BIT(1), /* 1=up, 0=down      */
      COUNT    BIT(1), /* 1=count, 0=program */
      COUNTOUT BIT(4); /* counter output     */
INTERNAL COUNTER;
  DCL I        BIT(4); /* counting variable  */
BODY COUNTER;
  DO  INFINITE LOOP
    COUNTOUT:=I;
    IF COUNT
      THEN IF UP THEN I:=I+1;
                 ELSE I:=I-1;
           ENDIF;
      ELSE I=COUNTIN;
    ENDIF;
  ENDDO;
END COUNTER;
```



Integrated TLM Design & Verification

Specification

Verify

Regress

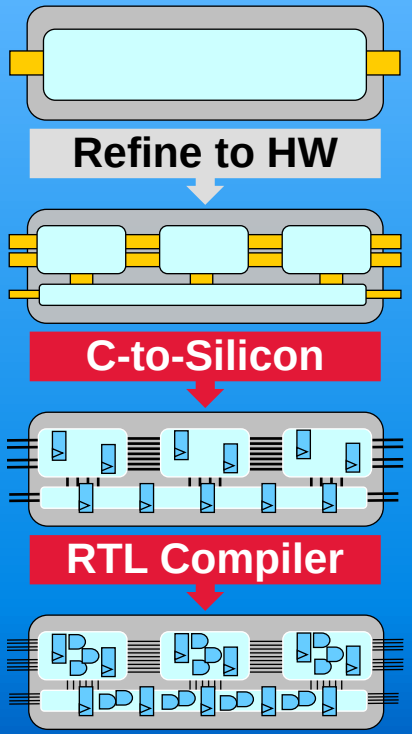
Verification Plan

Algorithm
- Input interface
- Output interface
- Core – black box

Architecture
- Input protocol
- Output protocol
- Core – white box

Micro-architecture
- User-constrained features
- HLS-generated features

Implementation
- Equivalence
- Timing



SystemC Virtual Prototype

SystemC HLS-ready (high-level syn)

RTL

Gates

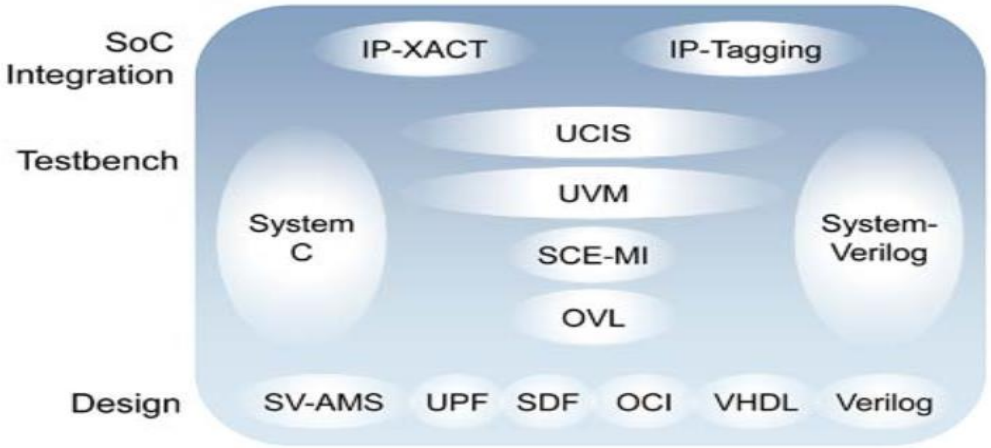
UVM and DVcon

2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

MARCH 2–5, 2015

DoubleTree, San Jose

Accellera Systems Initiative
EDA and IP Design Standards and Initiatives



DVCon is Heading to Europe!

2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION EUROPE

November 11-12, 2015
Location Coming Soon!

FIND OUT MORE >

DVCon is Heading to India!

2015 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION INDIA

More Information Coming Soon!

VIEW DVCON 2014 INDIA PHOTO GALLERY >

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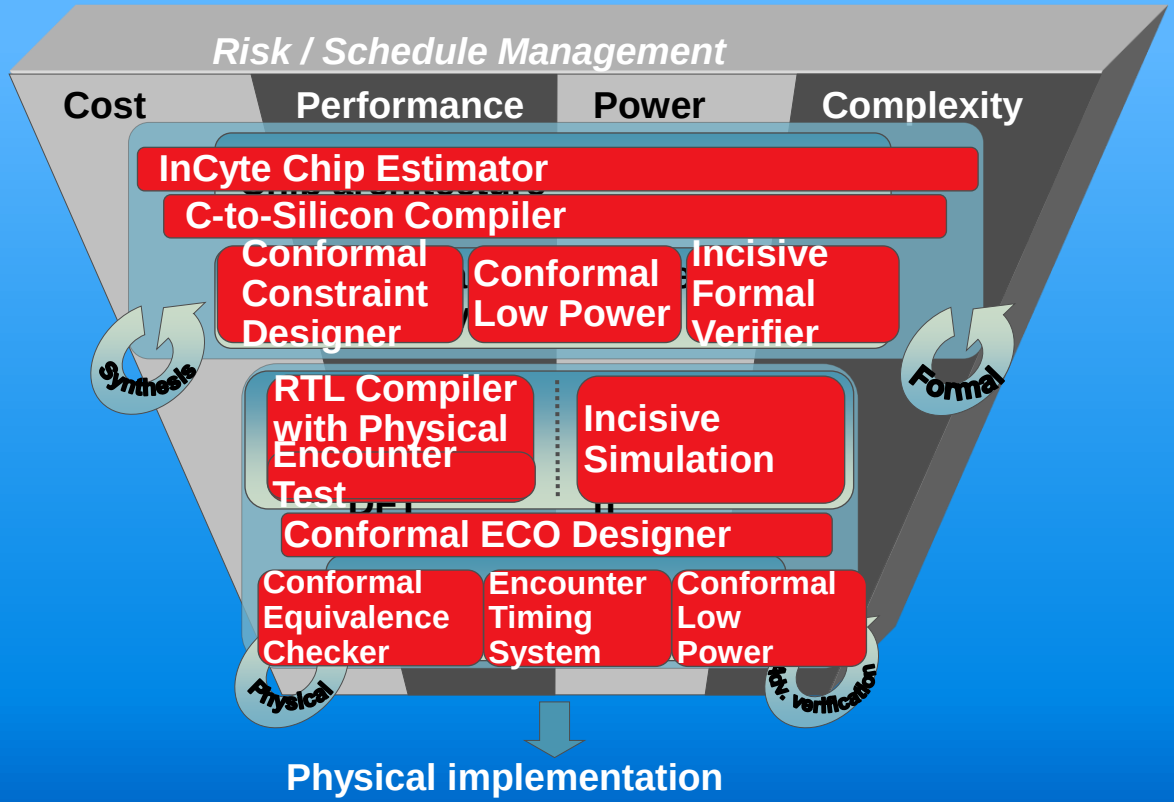
System-to-GDSII Low-Power Methods

- **System Design**
  - Chip Planning
  - ESL Design
  - Logic Design
  - Analog/Custom Design
  - Digital Implementation
  - Package Design
- **Design Verification**
  - System-level Verification
  - Functional Verification
  - System Design Manager
  - Low-Power Conformal
- **Design Implementation**
  - RTL Compiler
  - DPA w/ Emulator
  - LP Analysis System
  - Signoff

Front-End Flow

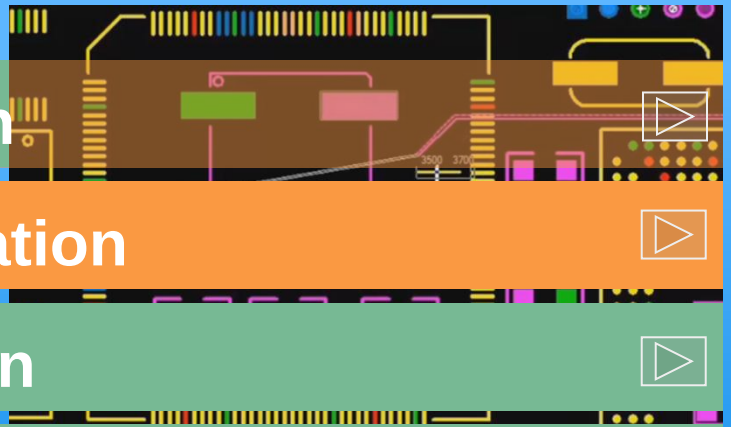
- Management
- Complexity



ESD, System Design and Verification

- ESD
- SDV
- SoC Design and IP Integration

EDA and IC Design



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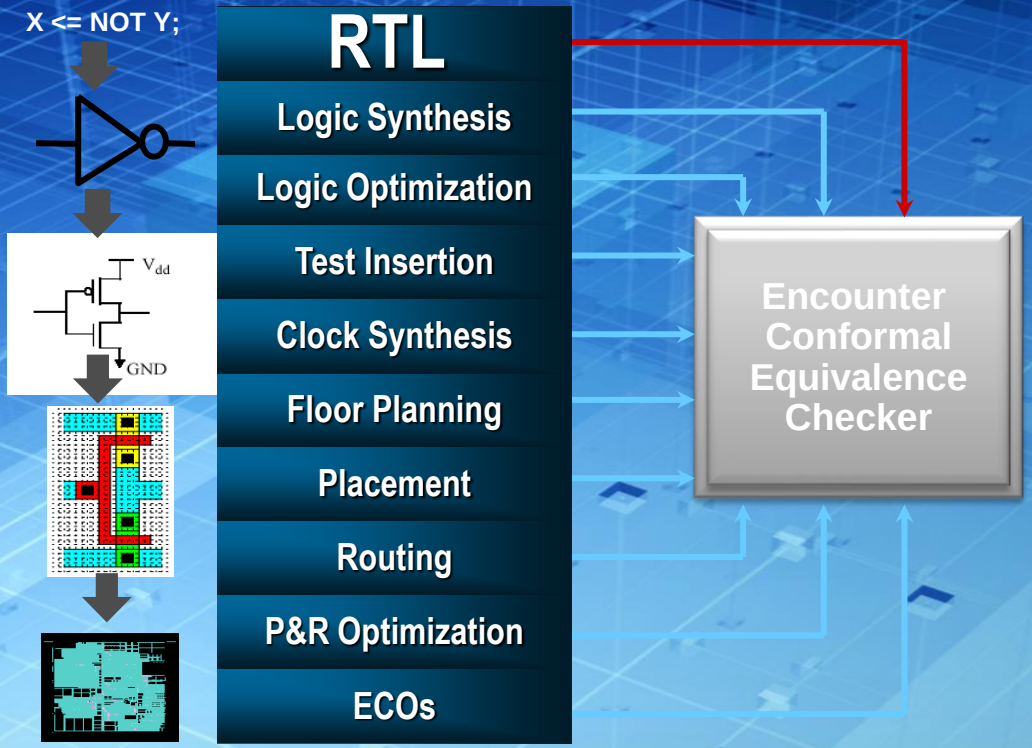
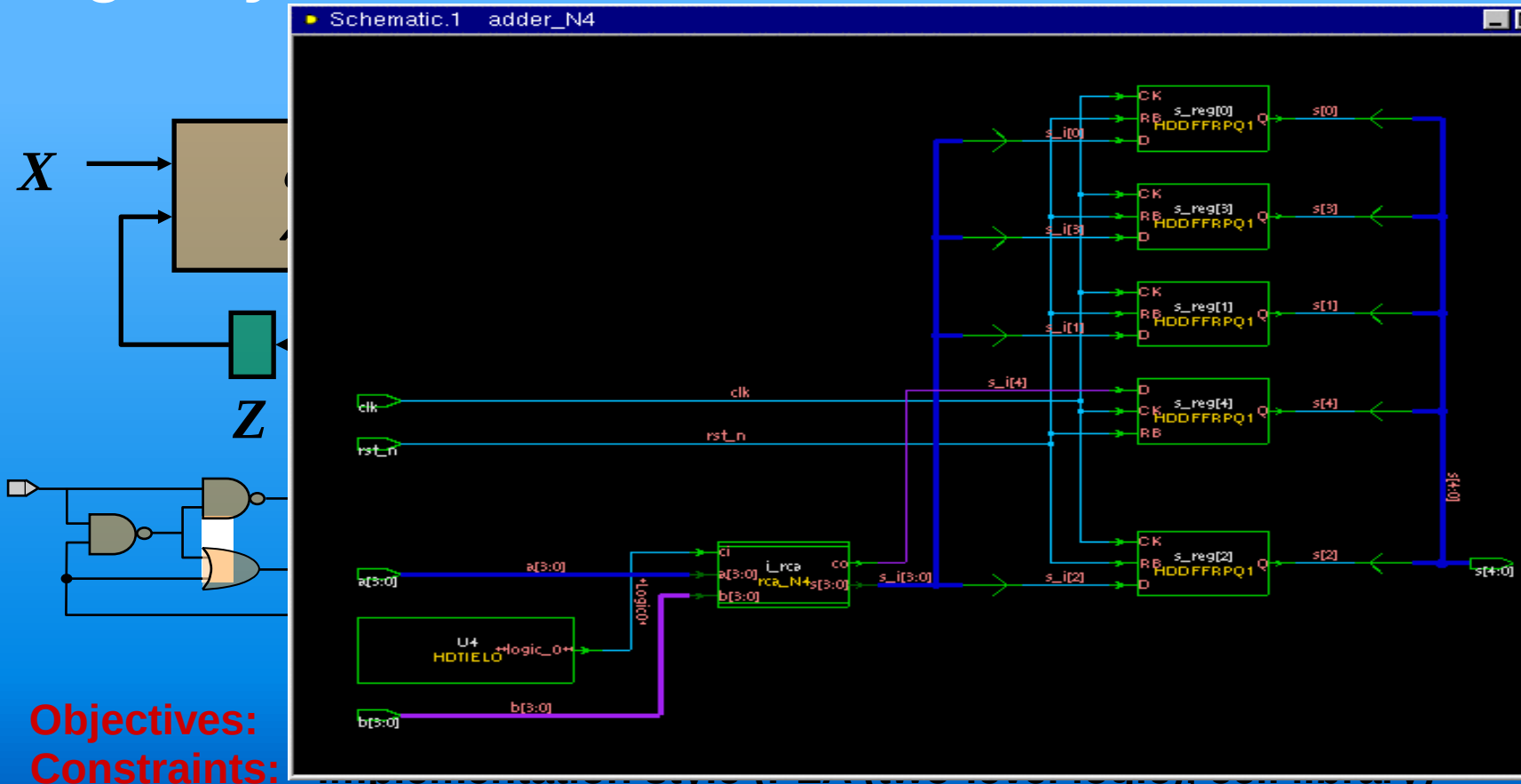
ASIC & FPGA design implementation verification



Logic Synthesis



Objectives:

Constraints: implementation style (e.g. RTL (two level logic), cell library)

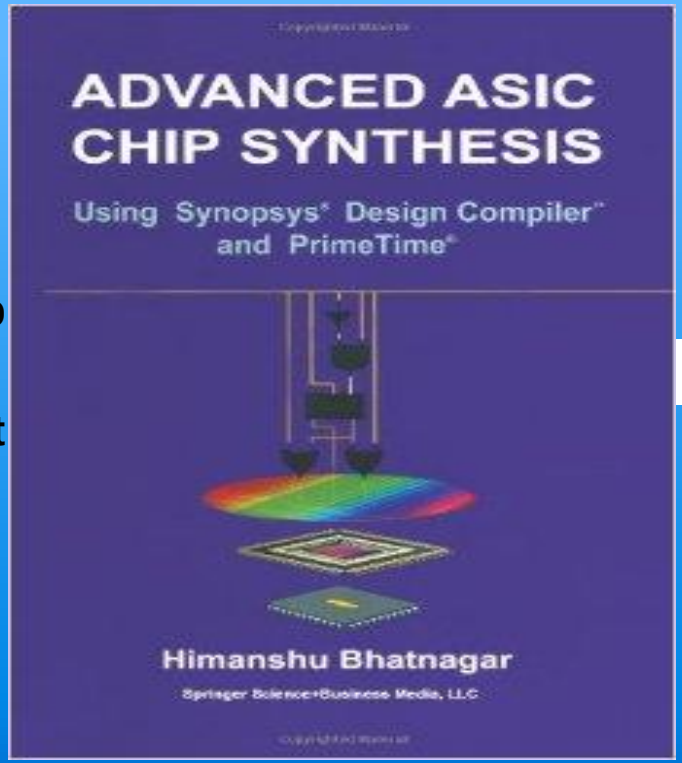
Synthesis Example

- 4-bit Up/Down Counter
  - 4-bit input "countin"
  - 4-bit output "countout"
  - up/down control "up"
  - count control "count"
  - internal state "i"
  - implied clock
- Behavior
  - up = 1 => count up
  - up = 0 => count down
  - count = 1 => count
  - count = 0 => load

up

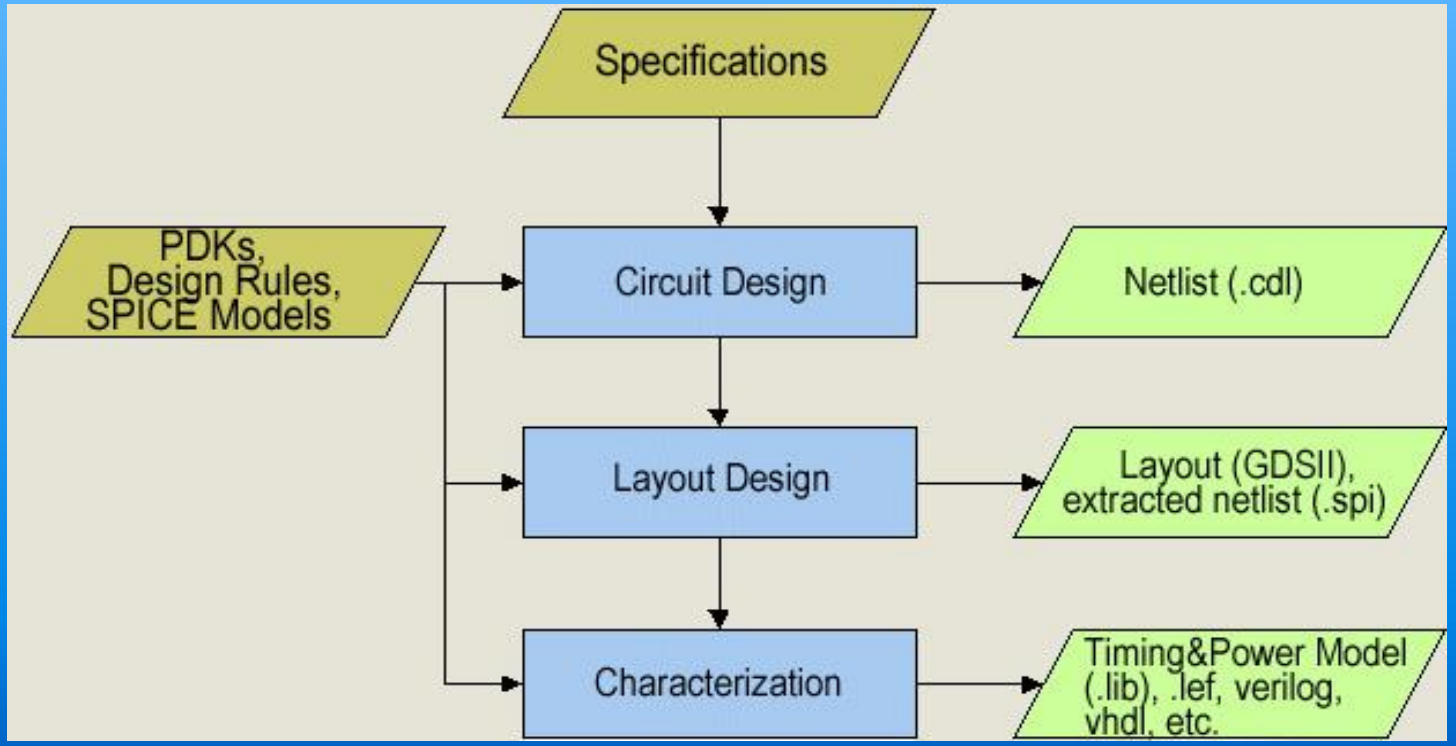
count

clock

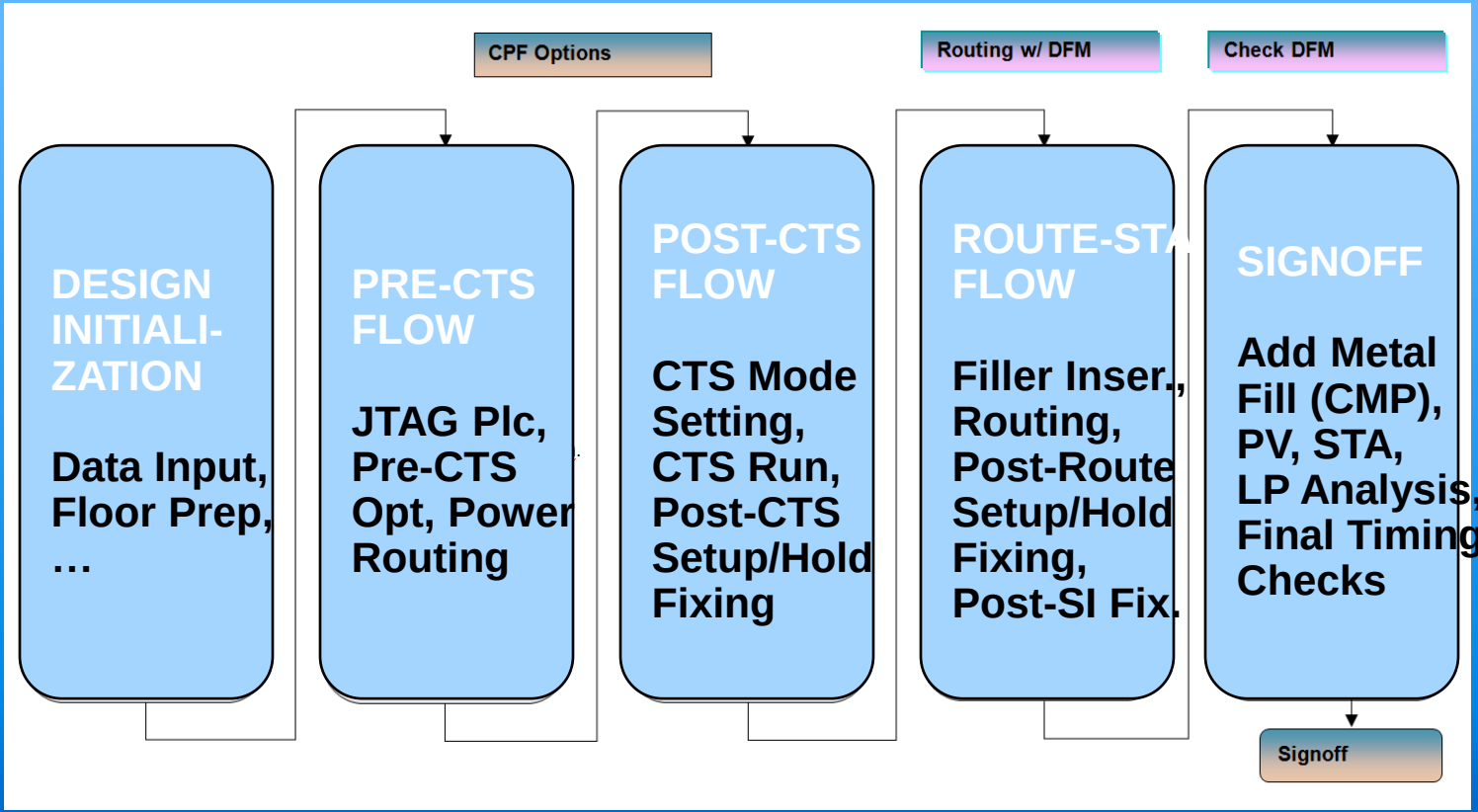


Digital Standard Cell Design Flow

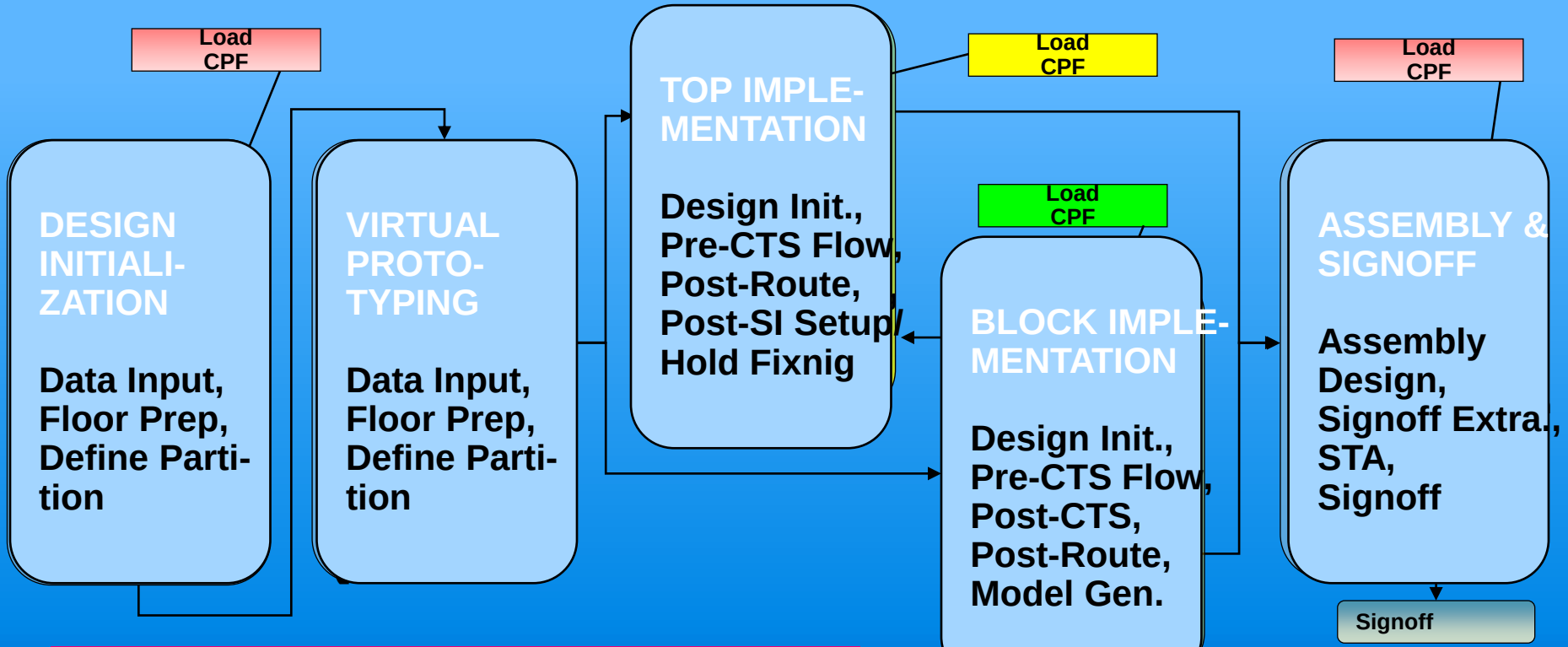
- Simplified flow



Physical Design Flow for LP-SoC



Hierarchical Flow with Low Power

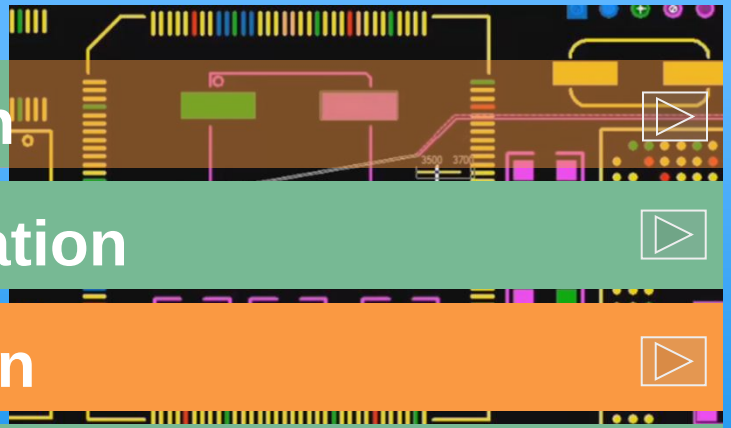


Advanced Place and Route Method

Digital Design and Implementation

- RTL (Verilog) Synthesis to GLN
- Data preparation (GLN, .lib, LEF, SDC …)
- SoC Design Implementation
  - FP, PP, Place, CTS, Route, … Sign-off

EDA and IC Design



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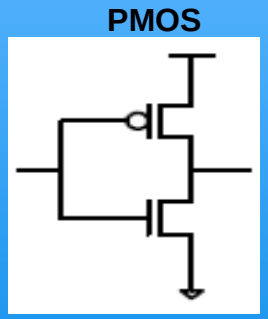
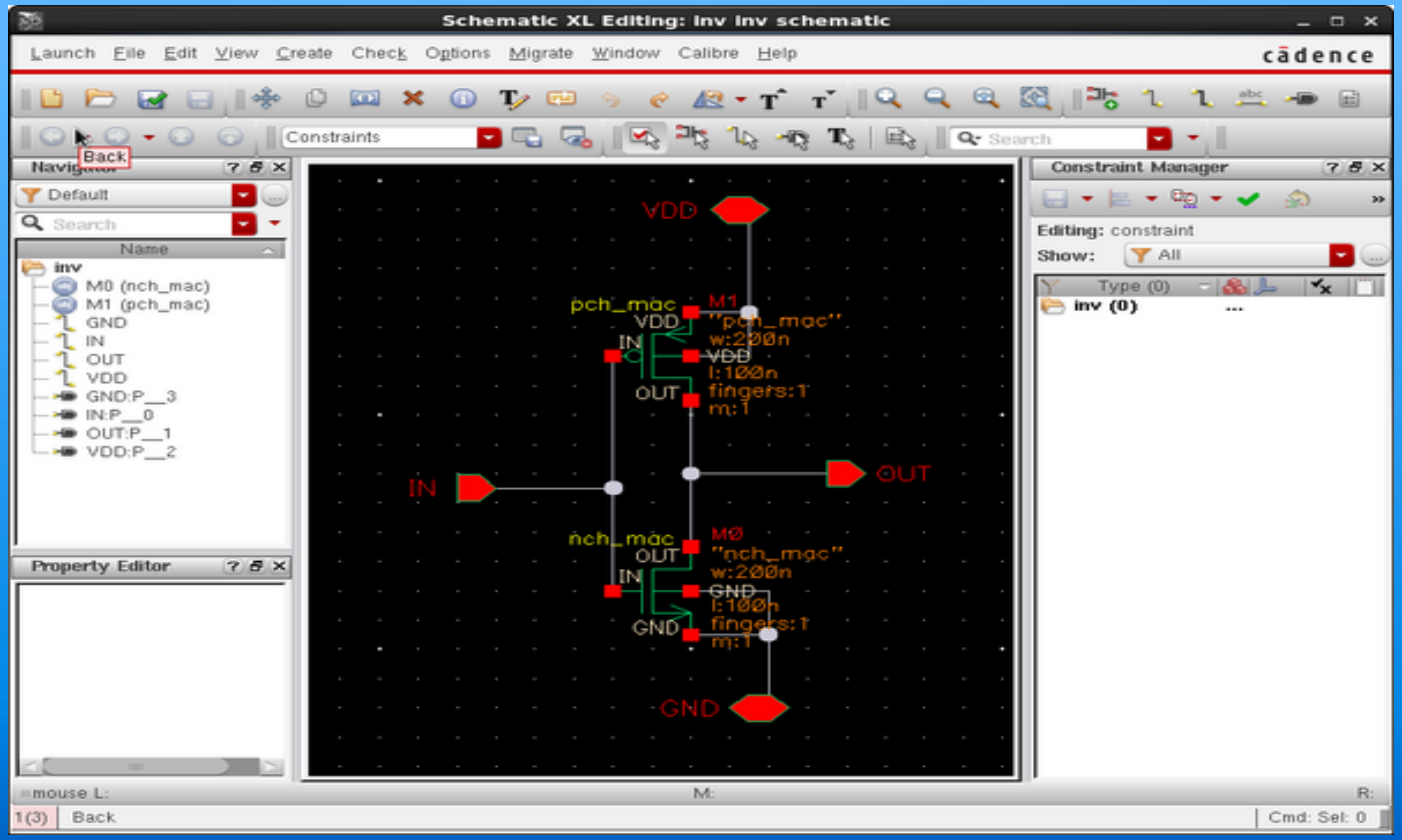
Standard Cell Design

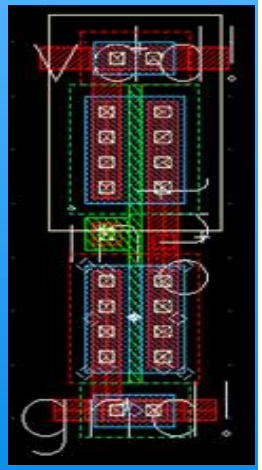
From Schematic to Layout

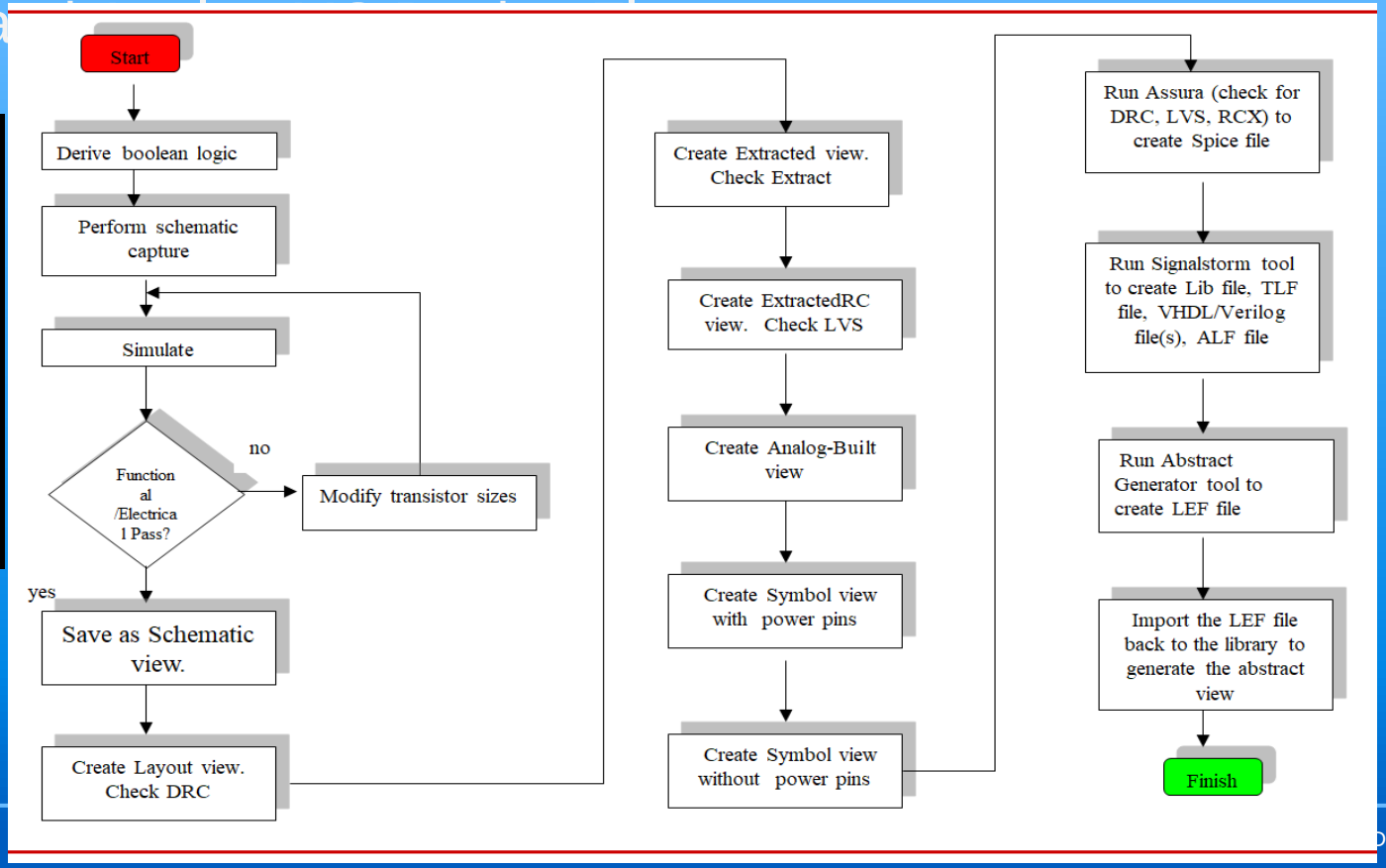




Digital IC Design and Characterization vs Circuit Design and Simulation

- Digital a





Mixed-Signal Implementation Flows

A — A/d — A/D — D/A — D/a — D

Methodology	Schematic-driven		Netlist-driven	
	Analog/Custom	AoT	MSoT	DoT
Design	Analog; might have very small number of std. cells placed and routed without digital P&R tools	Top level is analog; standard cell digital contained inside block designed using digital flow.	Analog and standard cell digital mixed at same level.	Predominantly digital design with analog integrated as hard macro
Top level connectivity	Schematic	Schematic	Verilog	Verilog
Floorplanning	VFP	VFP and EDI	VFP and EDI	EDI
Analog content	Main/Top	Main/Top	Co-designed	Black-boxed
Digital content	Custom digital	Black-boxed	Co-designed	Main/Top
Routing	All routing done by VSR	Top level and analog block by VSR; routing within digital block by NR	Analog block by VSR; Digital block by NR; Top: analog by VSR, standard cell by NR	Top level analog by VSR; all other routing by NR.
Chip Integration	Virtuoso	Virtuoso	EDI	EDI
Signoff	SPICE Simulation	MSPS	STA	STA
Chip Finishing	Virtuoso	Virtuoso	Virtuoso	Virtuoso/EDI

Note: "Analog" covers transistor level design including Analog, RF and Custom Digital

Physical Verification and DFM

Physical Verification

- Calibre nmDRC
- Calibre nmLVS
- Calibre Pattern Matching
- Calibre Auto-Waivers
- Calibre Interactive
- Calibre RVE
- Calibre DESIGNrev
- Calibre RealTime
- Calibre 3DSTACK
- Calibre InRoute

Circuit Verification

Design for Manufacturing

Calibre Interfaces

Custom IC Design

Physical Verification with Calibre®

Calibre's physical verification capabilities are the industry leader for accuracy, reliability, and performance

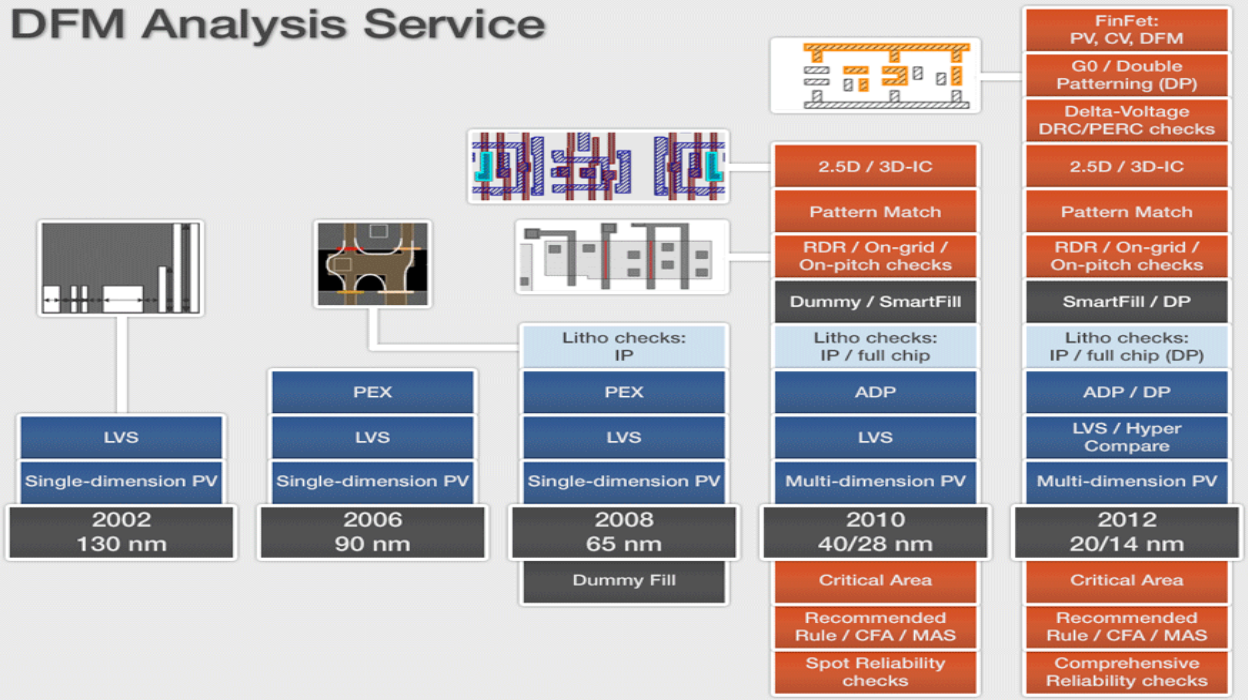
View Products

- Calibre 3DSTACK
- Calibre nmDRC
- Calibre nmLVS
- Calibre Pattern Matching
- Calibre Automatic Waivers
- Calibre Interactive
- Calibre RVE
- Calibre DESIGNrev
- Calibre RealTime

Calibre Pattern Matching

Pattern-driven design correction, analysis and verification. Streamline and simplify complex checks, integrate

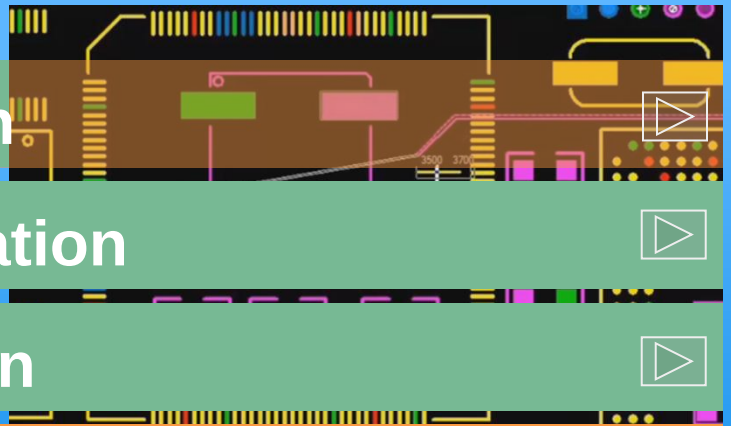
DFM Analysis Service



AMS Design and Simulation

- AMS and RF design
- Circuit design and simulation
- Custom layout design and verification
- DFM

EDA and IC Design



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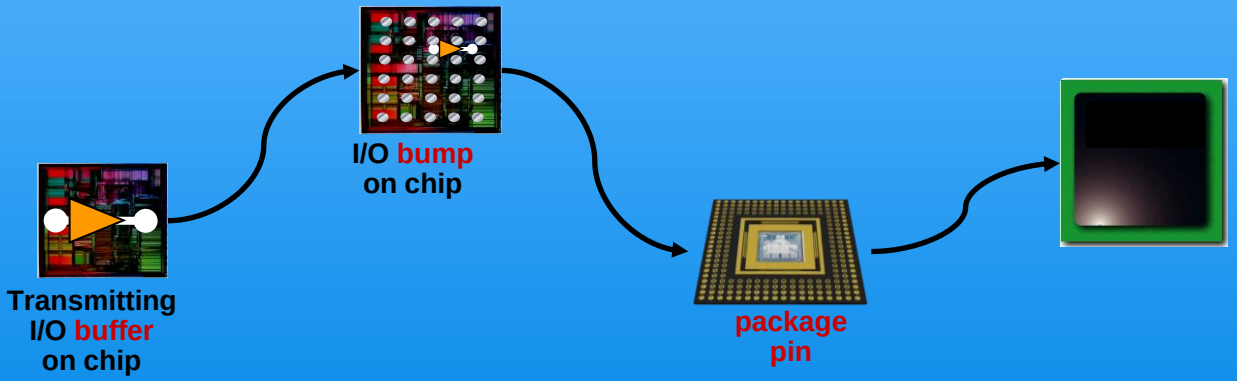
What is Silicon/Package Co-Design

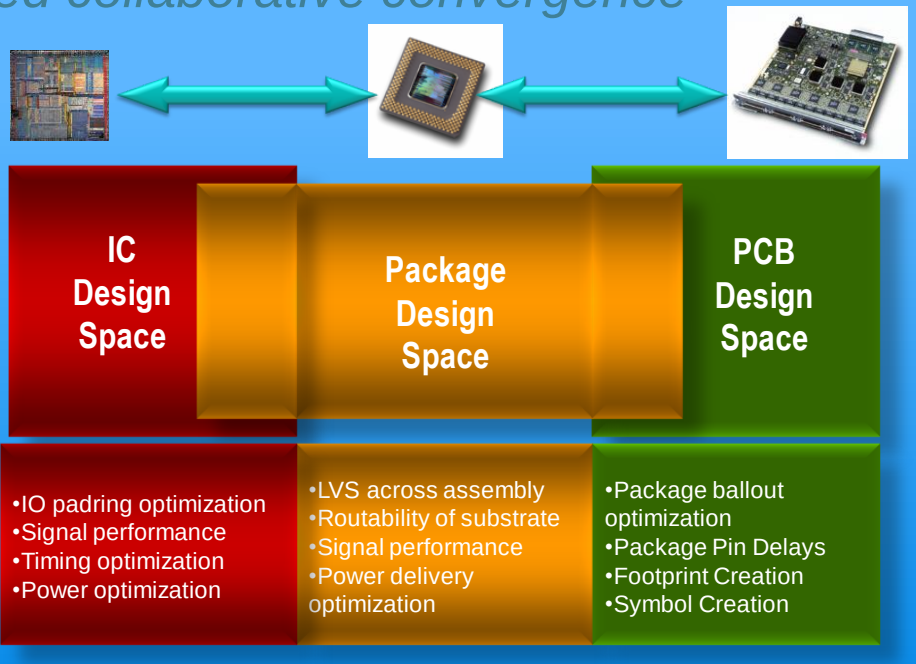
- “A Design Environment That Will Enable The Co-Design and Optimization of Chip I/O FloorPlanning and IC Packaging”



“An integrated design methodology for the Co-Design and Optimization of silicon I/O placement, Bump Matrix assignment, RDL and package feasibility”

Team Design Across Fabrics

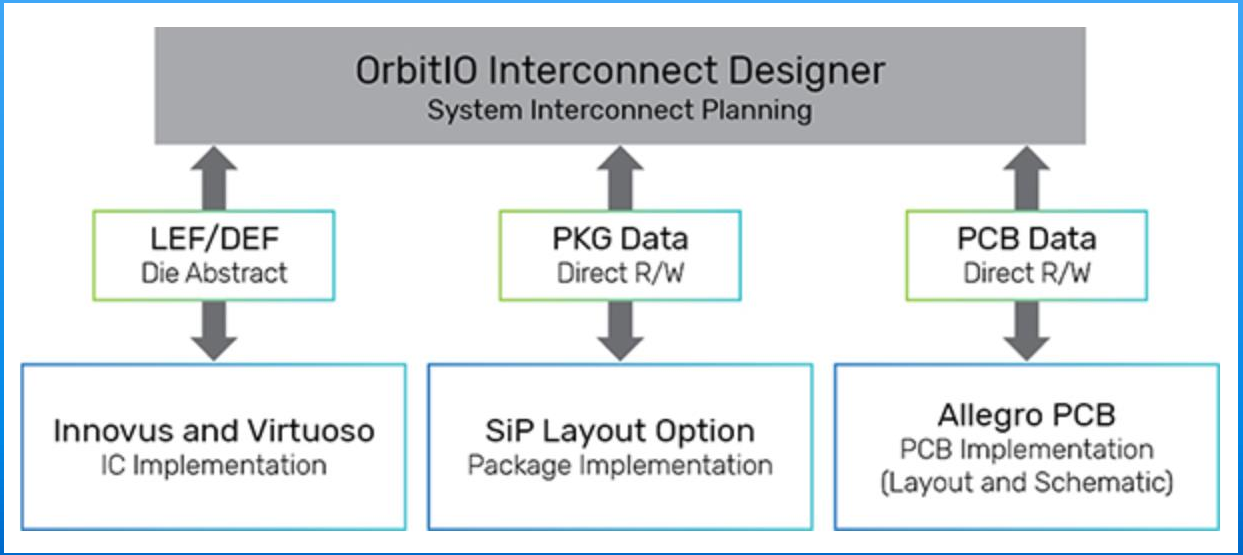
Co-design enabled collaborative convergence



- Delivers optimal package and chip (size, cost, performance, power)
- Validates device-level timing and power performance
- Minimizes board complexity and cost
- Reduces ECO risk providing schedule predictability

System Interconnect Plan/Design

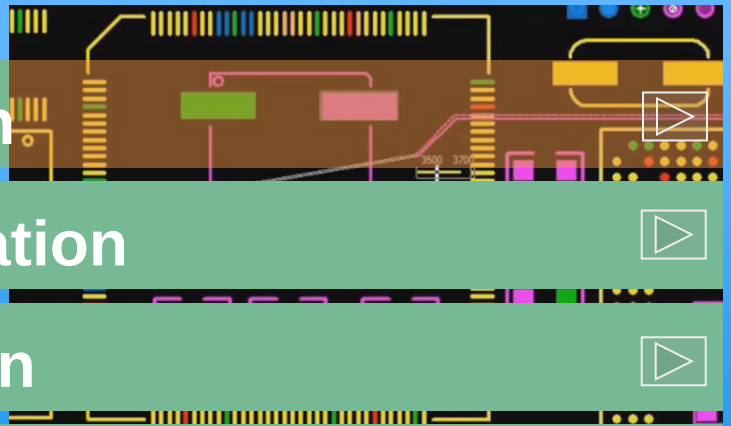
- Digital | Analog SoC Data
- Package Data
- PCB Data



Packaging and PCB Design

- Packaging
- PCB Design
- Testing

EDA and IC Design



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Thank you!

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(Anecdote)