



# IC Invention and Silicon Valley

## *Overview of Semiconductor Industry*

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# Topics

**Inventions**



**60<sup>th</sup> Anniversary of Fairchild**



**Intel and Moore's Law**



**Stanford University and UC Berkeley**



**The Creation of Silicon Valley**



# Invention of Junction Transistor

- 1947 the first junction transistor
  - John Bardeen, William Shockley & Walter Brattain
  - 1956 Nobel Prize in Physics



- BCS theory of superconductivity
  - 1972 Nobel Prize in Physics
- Shockley Semiconductor Corporation

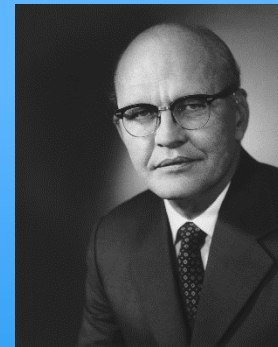
# Shockley Semiconductor Laboratory

- 1956, William Shockley founded the Lab
- The first high tech company in Silicon Valley
- A division of Beckman Instruments

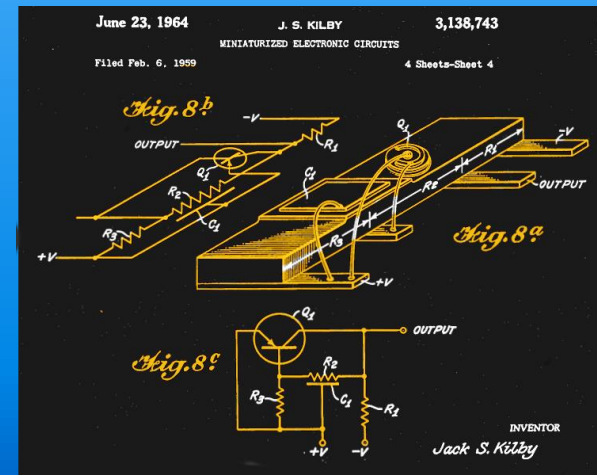
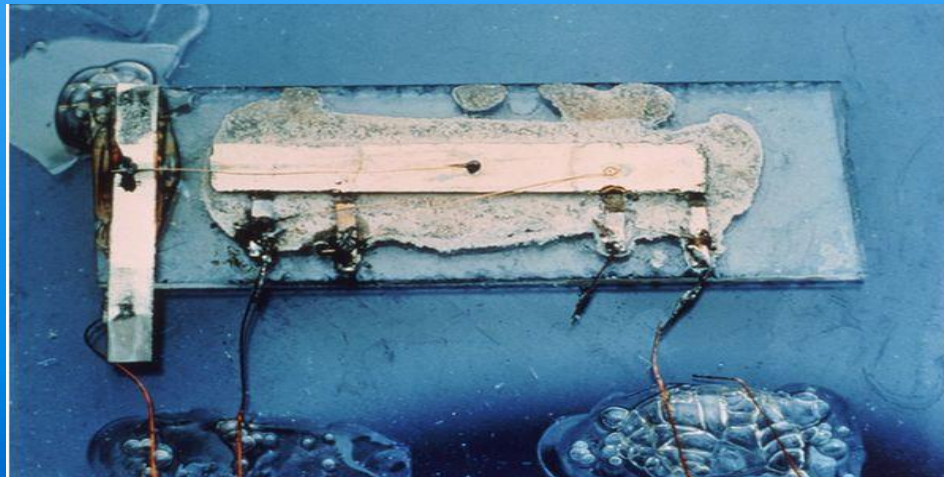


# The First Integrated Circuit (1/2)

- Jack Kilby (1923-2005)
- Inventor of (Ge) IC in 1958
- IEEE milestones, Nobel Prize in 2000
- 1964, U.S. Patent 3,138,743



US Patents filed:  
3,138,743 (2/6/59)  
3,138,744 (5/6/59)



# The First Integrated Circuit (2/2)

Arthur Rock, Chairman of Intel's Board, said:

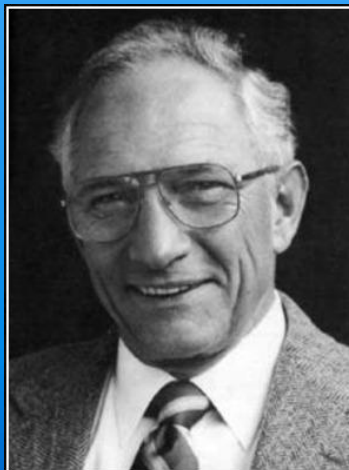
**Noyce**: the visionary, born to inspire;

**Moore**: the virtuoso of technology; and

Grove: the technologist turned management scientist.

## ● Robert Noyce (1927-1990)

- “The Traitorous 8”
- Co-founded Fairchild in 1957
- Co-inventor of (Si) IC in 1958
- Co-founded Intel in 1968
- “The Mayor of Silicon Valley”



Optimism is an essential ingredient of innovation. How else can the individual welcome change over security, adventure over staying in safe places?

— Robert Noyce —

AZ QUOTES



- Sept 2017
- FAIRCHILD SEMICONDUCTOR: THE 60TH ANNIVERSARY OF A SILICON VALLEY LEGEND



Inventions



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The Creation of Silicon Valley





- 1956, William Shockley founded the Lab
- *1957, Fairchild Semi was formed...*
  - A division of Fairchild Camera & Instruments
  - 1959, "IC-Si" (vs. "IC-Ge"); planar process
- IC-Si and Planar Process
  - Jean Hoerni, planar process (2 US patents)
  - Robert Noyce ...

# “The Traitorous Eight”

- 1956, Shockley Semiconductor Laboratory
- 1957, Fairchild Semi was formed...
- 1957, “The Traitorous Eight” resigned ...
  - Gordon Moore, C. Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni and Jay Last

# Fairchild Today



- 1957 Founded in San Jose
  - as A division of Fairchild Camera & Instruments
  - Schlumberger bought the firm in 1979
  - Schlumberger sold it to National Semiconductor in 1987;
- Fairchild was spun off as an independent company in 1997
- ON Semiconductor acquired Fairchild in September 2016



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# Intel and Microprocessors

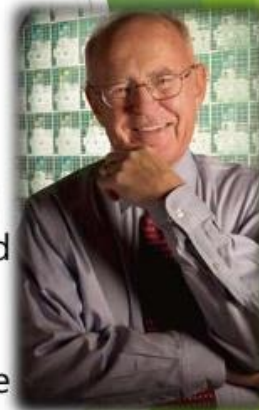
- An IDM of *Int*egrated *el*ectronics
  - x86 Series and PC
  - Supplies for Apple, Lenovo, HP and Dell
- Arthur Rock: “Intel needs Noyce, Moore and Grove...”
  - Robert Noyce, “The Mayor of Silicon Valley”
  - Gordon Moore, Moore’s Law (1965/1975)
  - Andrew Grove, *Only the Paranoid Survive* (1996)



- Moore's Law
- Dennard Scaling
- Intel
  - Tick-Tock
  - Process-Architecture Optimization

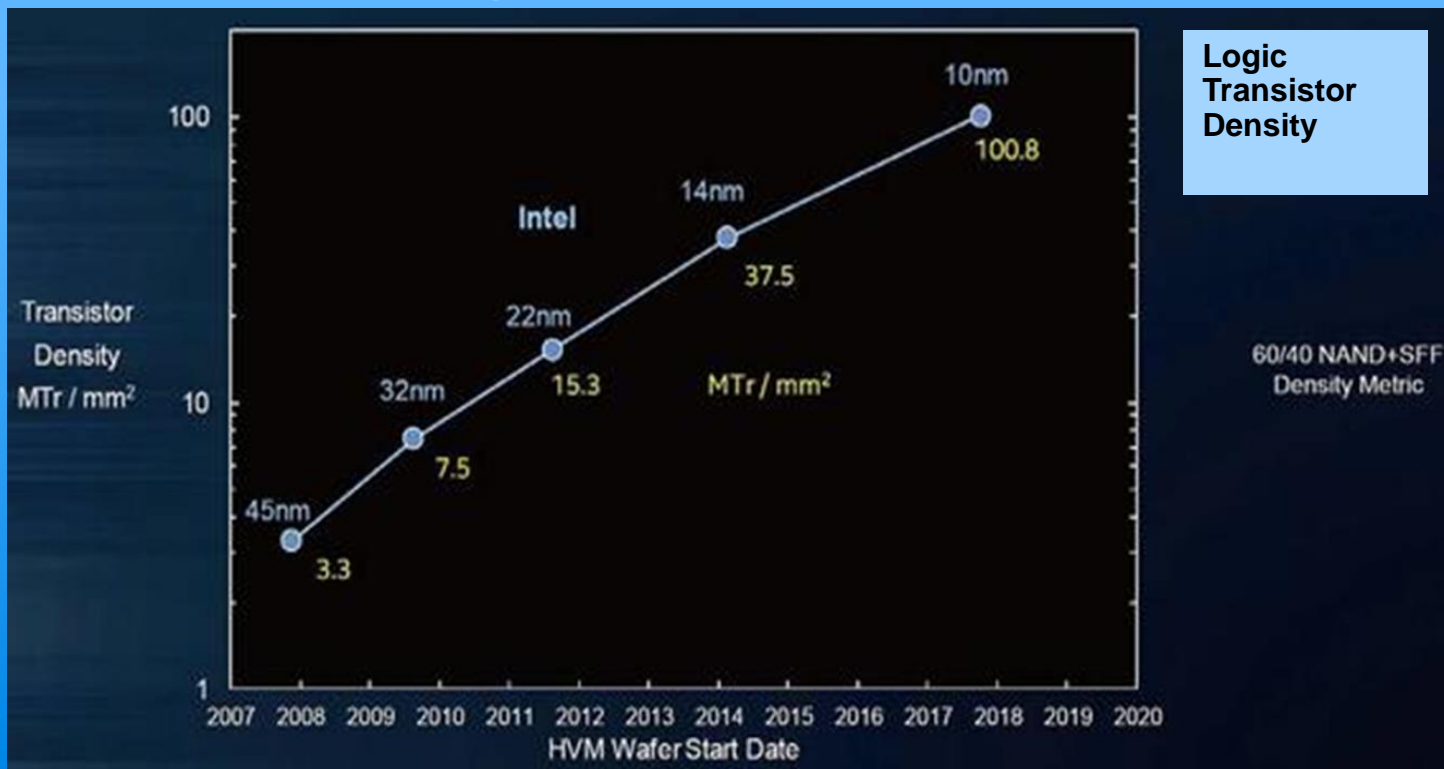
## Moore's law

- ▶ Moore's law is the observation that the number of transistors in a dense integrated circuit doubles approximately every two years.
- ▶ The observation is named after Gordon Moore, the co-founder of Intel and Fairchild Semiconductor, whose 1965 paper described a doubling every year in the number of components per integrated circuit, and projected this rate of growth would continue for at least another decade



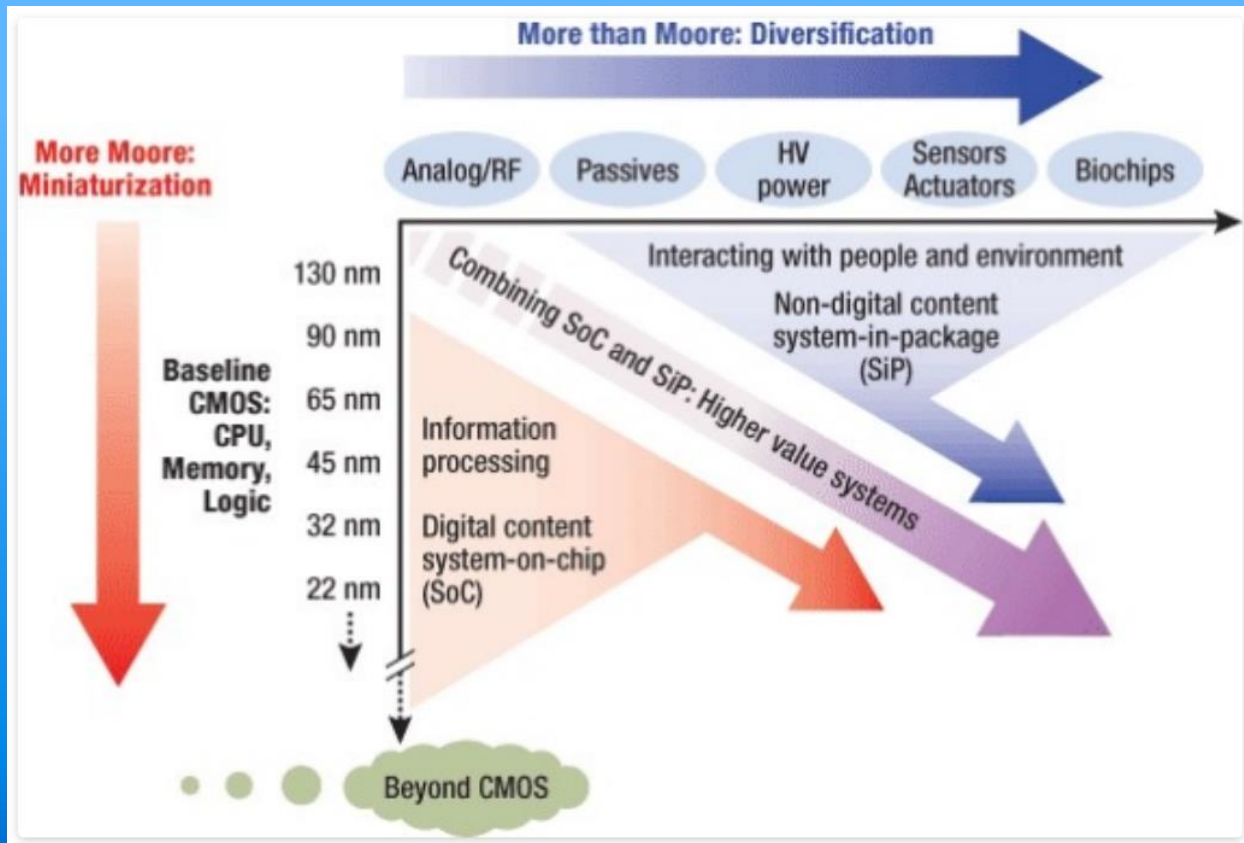


# Transistor Density and Moore's Law



Intel, at 10nm, Transistor Density >100MTr/mm²

# More Moore, More than Moore, & Beyond CMOS



**Figure 1:** The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the ITRS: miniaturization of the digital functions ("More Moore") and functional diversification ("More-than-Moore").

# Dennard Scaling Law

- Dennard (1974) observed that voltage and current should be proportional to the linear dimensions of a transistor
- Thus, as transistors shrank, so did necessary voltage and current; power is proportional to the area of the transistor.
- Capacitance is related to area
  - So, as the size of the transistors shrunk, and the voltage was reduced, circuits could operate at higher frequencies at the same power
  - Why haven't clock speeds increased, even though transistors have continued to shrink?

# End of Dennard Scaling

- Dennard scaling ignored the “leakage current” and “threshold voltage”, which establish a baseline of power per transistor.
- As transistors get smaller, power density increases because these don't scale with size
- These created a “Power Wall” that has limited practical processor frequency to around 4 GHz since 2006

**Inventions**



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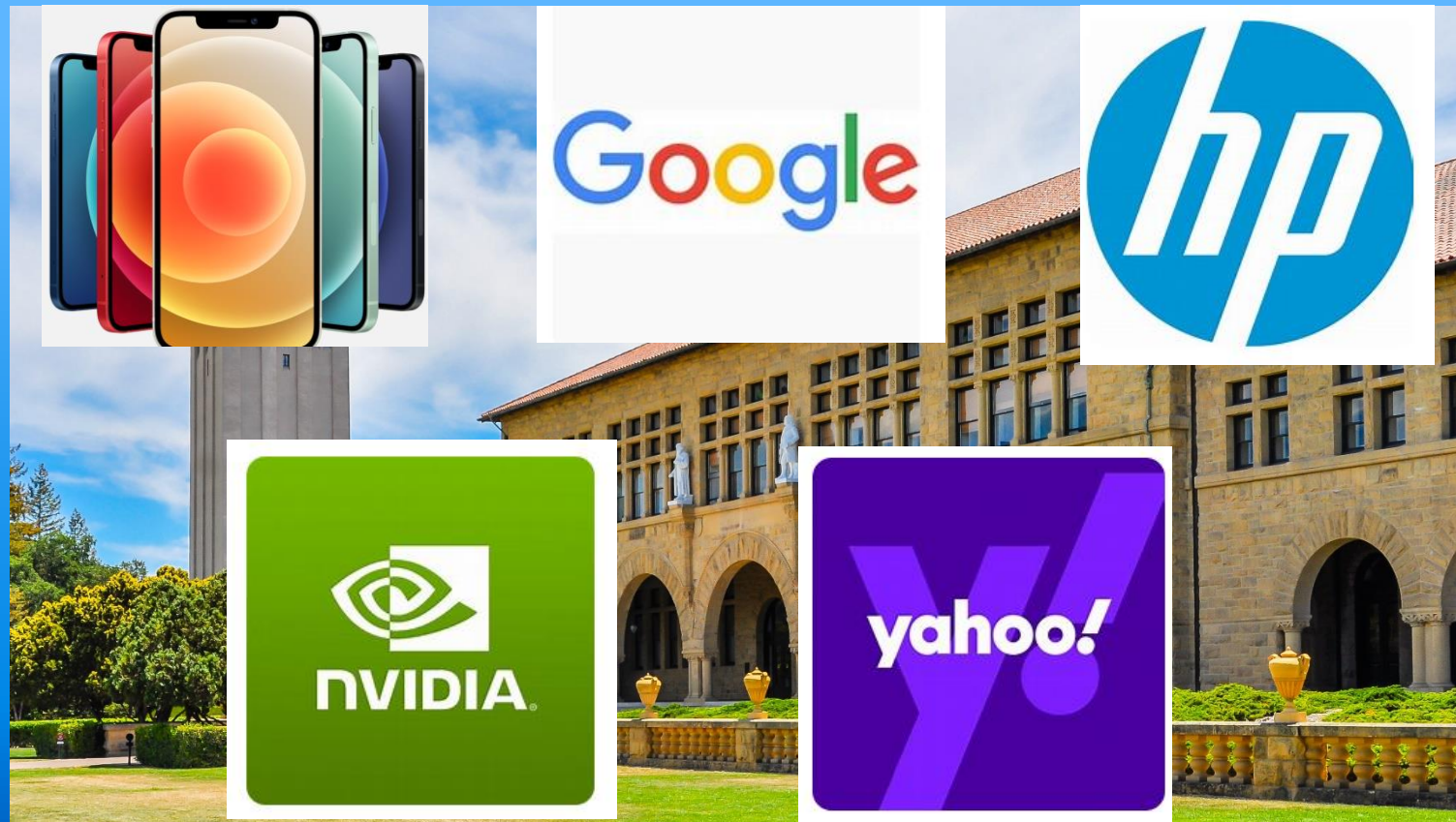


**The Creation of Silicon Valley**



# Stanford and Silicon Valley

*Storied past, uncertain future*





# Stanford University, 1950 vs Today

## Stanford University: 1950 vs. Today

Undergraduate students	4,800	6,700
Graduate students	2,800	8,200
Faculty Members	370	1,800
Tuition	\$600	\$33,000
Endowment	\$44M	\$14B



# CANCER and SPICE

1970, CANCER

Computer Analysis of Nonlinear Circuits, Excluding Radiation

1971, SPICE

Simulation Program with Integrated Circuit Emphasis



Laurence Nagel, Ron Rohrer, Don Peterson

- RISC-V ISA



- Berkeley Architecture Research

- <https://bar.eecs.berkeley.edu/projects/riscv.html>

- Nobel Prize in EDA



- Phil Kaufman Award, <https://ieee-ceda.org/>

- EECS

- Courses, <https://eecs.berkeley.edu/academics/courses>



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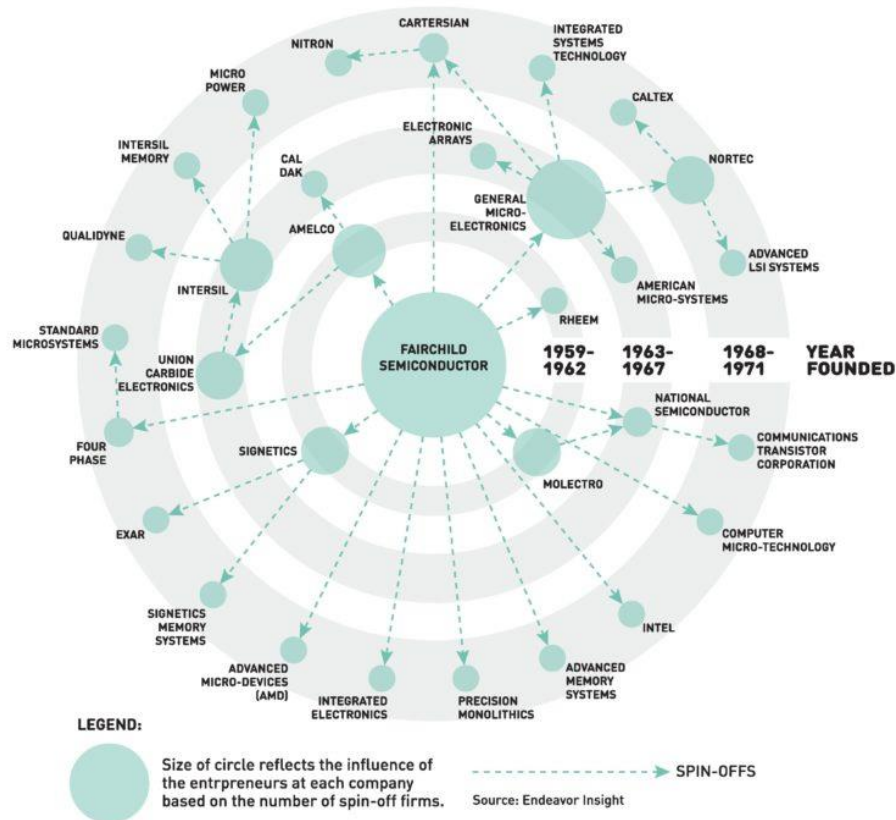
**The Creation of Silicon Valley**



# The Creation of Silicon Valley

## THE CREATION OF SILICON VALLEY: GROWTH OF THE LOCAL COMPUTER CHIP INDUSTRY

*Spinoff of Fairchild*



- 
- Geography
    - Climate in the Valley
  - Incubator for Innovation
    - Incubate, Nourish & Grow
  - Overtaking on the Curve?
    - Are driving and overtaking on right curves more dangerous than on left curves?



# In the Silicon Valley



# IC Design and EDA in 20<sup>th</sup> Century



中国科学院大学  
University of Chinese Academy of Sciences

SILICON



60s

70s

80s

90s