ECSE 323
Digital System Design

CMOS Digital Circuits

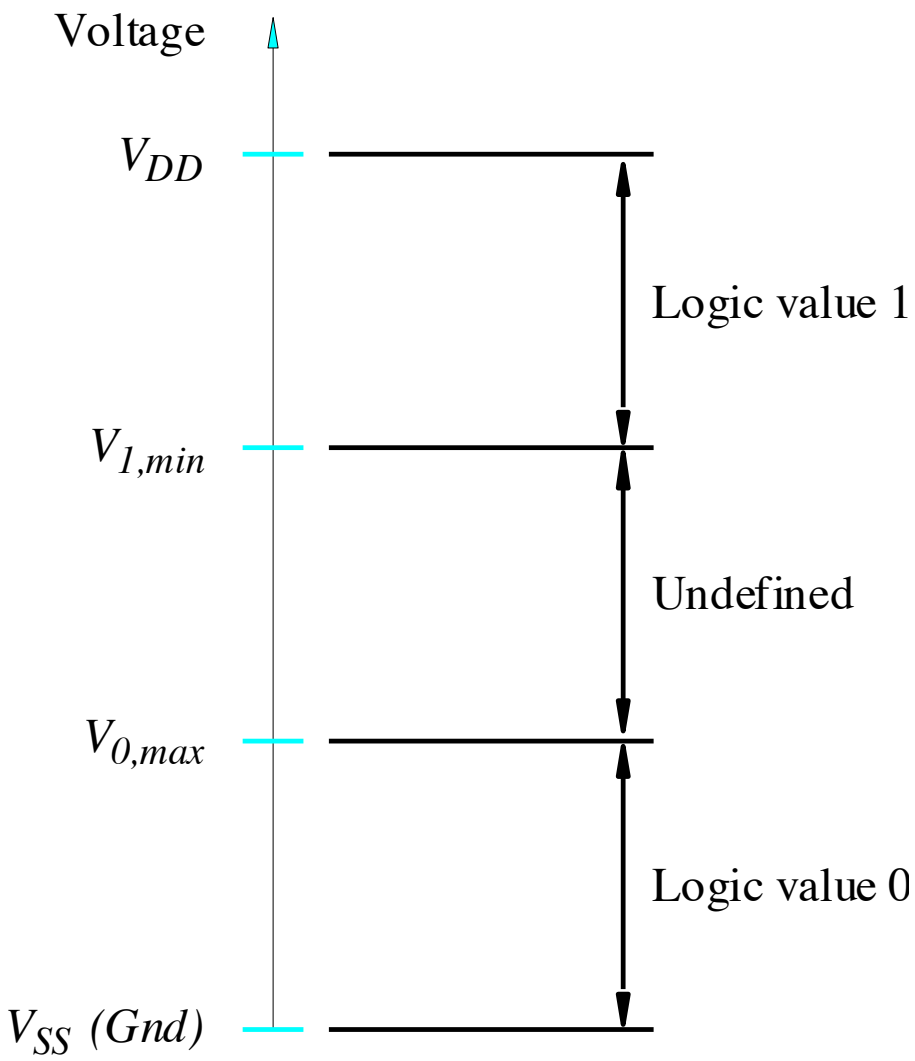
Prof. Warren Gross

Material used in this set of slides was based on "*Fundamentals of Digital Logic with VHDL Design*" by S. Brown and Z. Vranesic

Textbook Reading

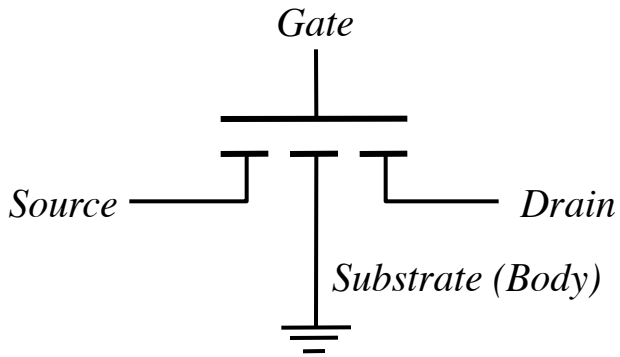
- This topic is about how logic gates are implemented using transistors.

- This topic will cover part of Chapter 3 (Implementation Technology).
- Sections 3.1-3.4, 3.8, and 3.9
- The skipped sections will be covered in a later topic

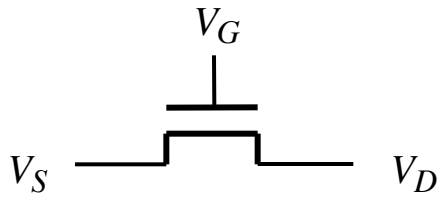


Logic values as voltage levels (positive logic system)
Typical values of V_{DD} = 5V, 3.3V, 1V

(a) A simple switch controlled by the input *x*



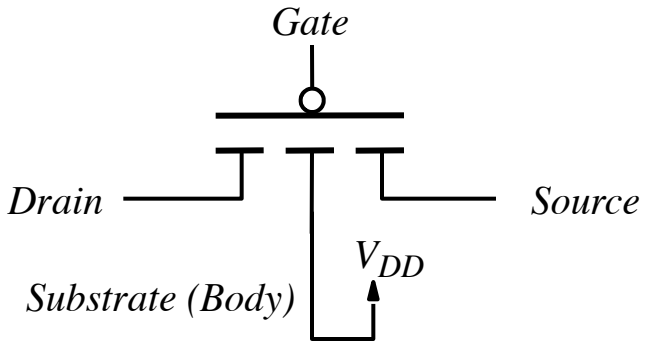
(b) NMOS transistor (n-channel MOSFET)



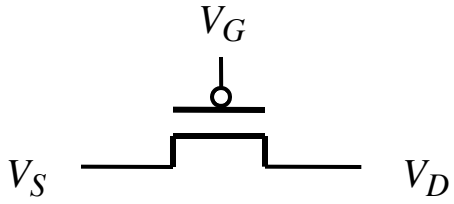
(c) Simplified symbol for an NMOS transistor.

NMOS transistor as a switch

(a) A switch with the opposite behavior of Figure 3.2 *a*



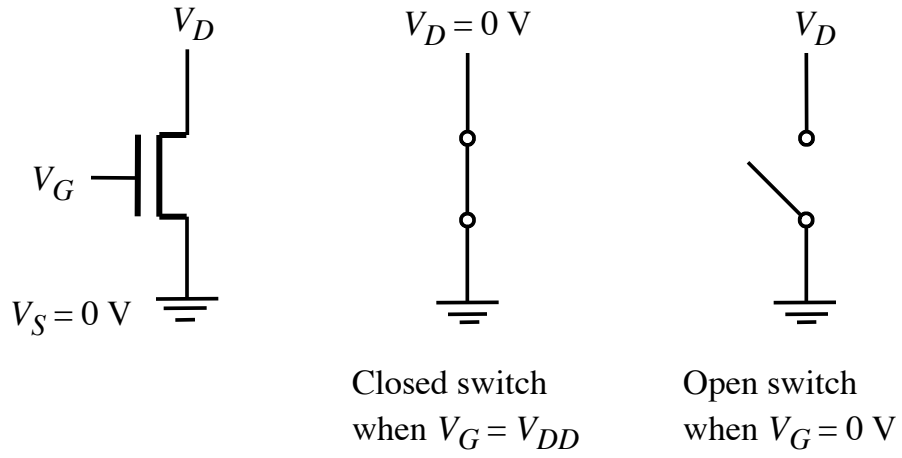
(b) PMOS transistor (p-channel MOSFET)



(c) Simplified symbol for a PMOS transistor

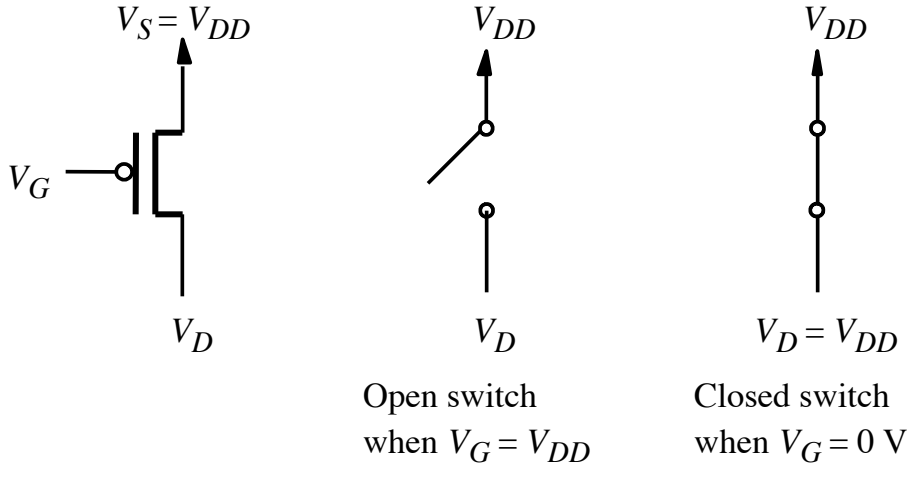
PMOS transistor as a switch

- Convention: the terminal with the lowest voltage applied is the source
- V_G low → transistor is off
- V_G high → transistor is on



(a) NMOS transistor

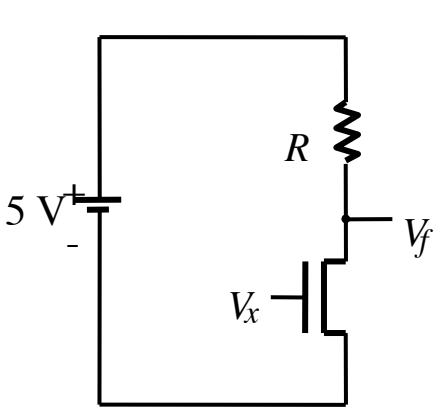
- Convention: the terminal with the highest voltage applied is the source
- V_G low → transistor is on
- V_G high → transistor is off



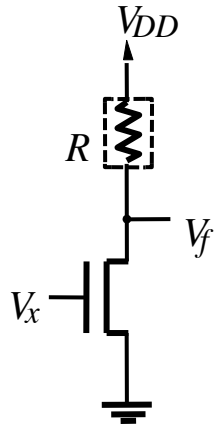
(b) PMOS transistor

NMOS and PMOS transistors in logic circuits

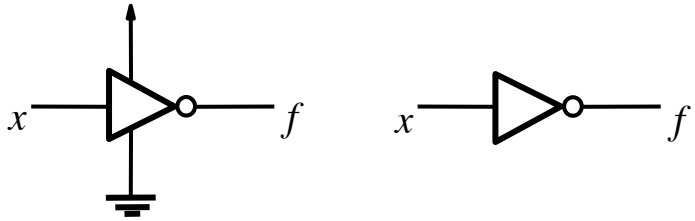
NMOS Circuits



(a) Circuit diagram

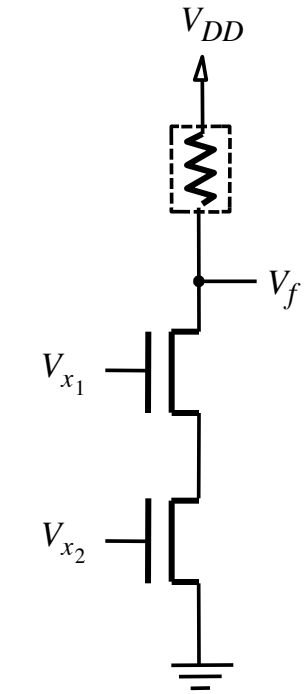


(b) Simplified circuit diagram



(c) Graphical symbols

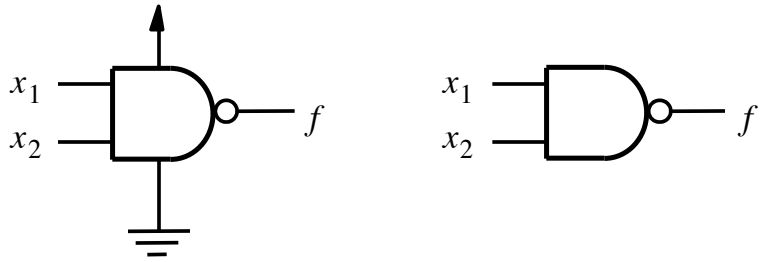
A NOT gate built using NMOS technology



(a) Circuit

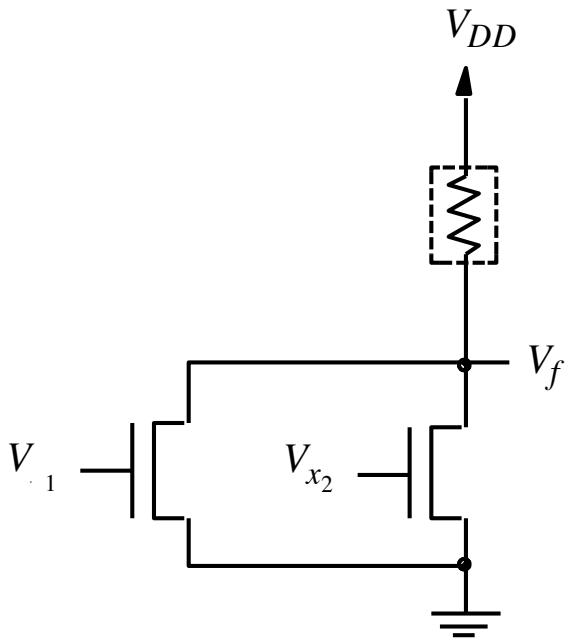
x_1	x_2	f
0	0	1
0	1	1
1	0	1
1	1	0

(b) Truth table



(c) Graphical symbols

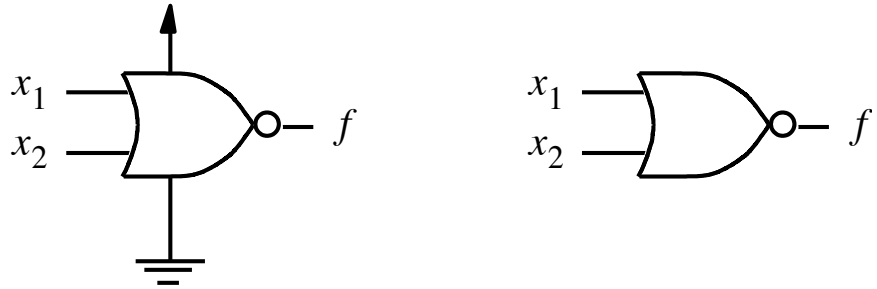
NMOS realization of a NAND gate



(a) Circuit

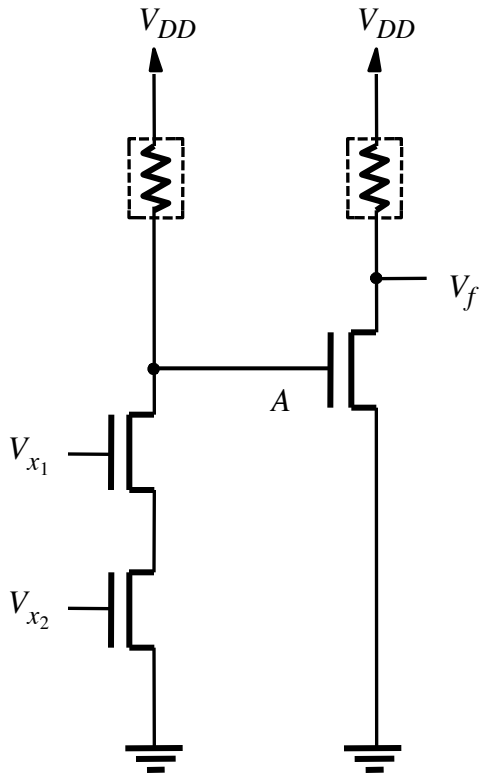
x_1	x_2	f
0	0	1
0	1	0
1	0	0
1	1	0

(b) Truth table



(c) Graphical symbols

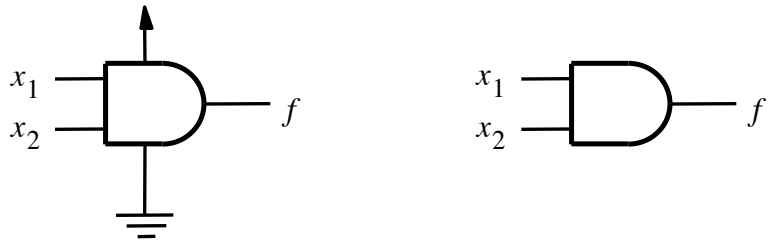
NMOS realization of a NOR gate



(a) Circuit

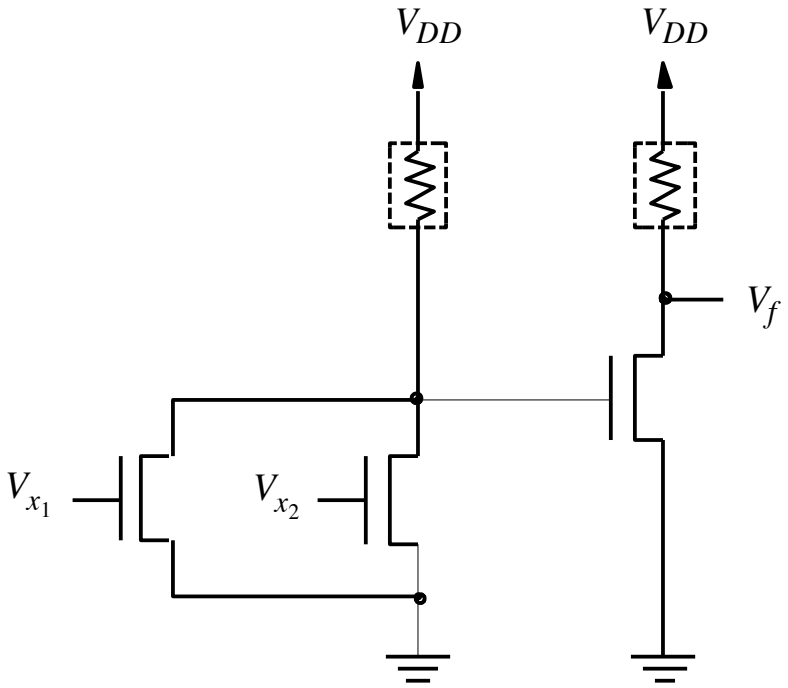
x_1	x_2	f
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table



(c) Graphical symbols

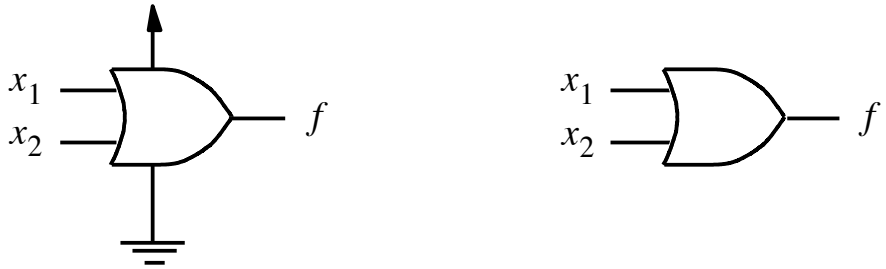
NMOS realization of an AND gate



(a) Circuit

x_1	x_2	f
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table

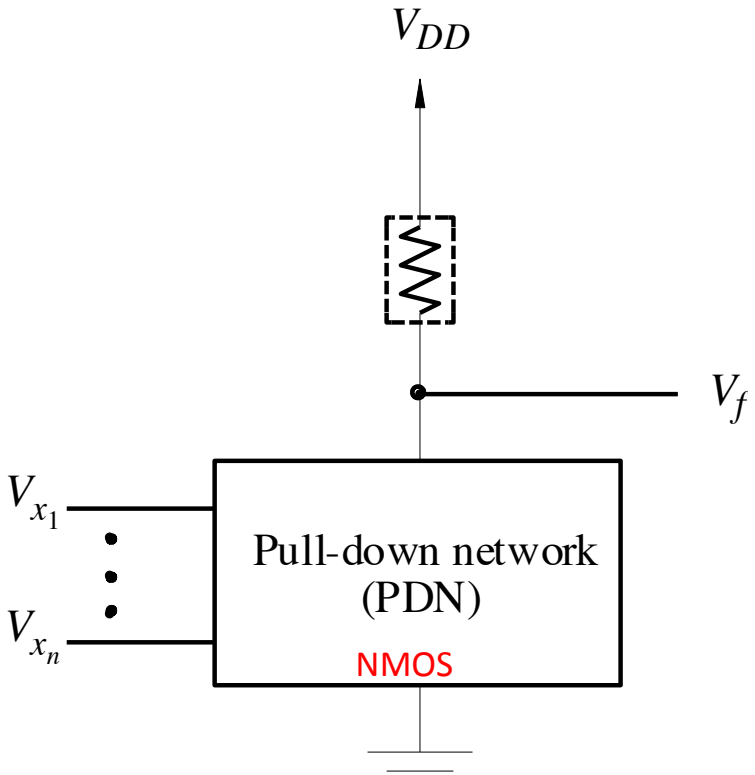


(c) Graphical symbols

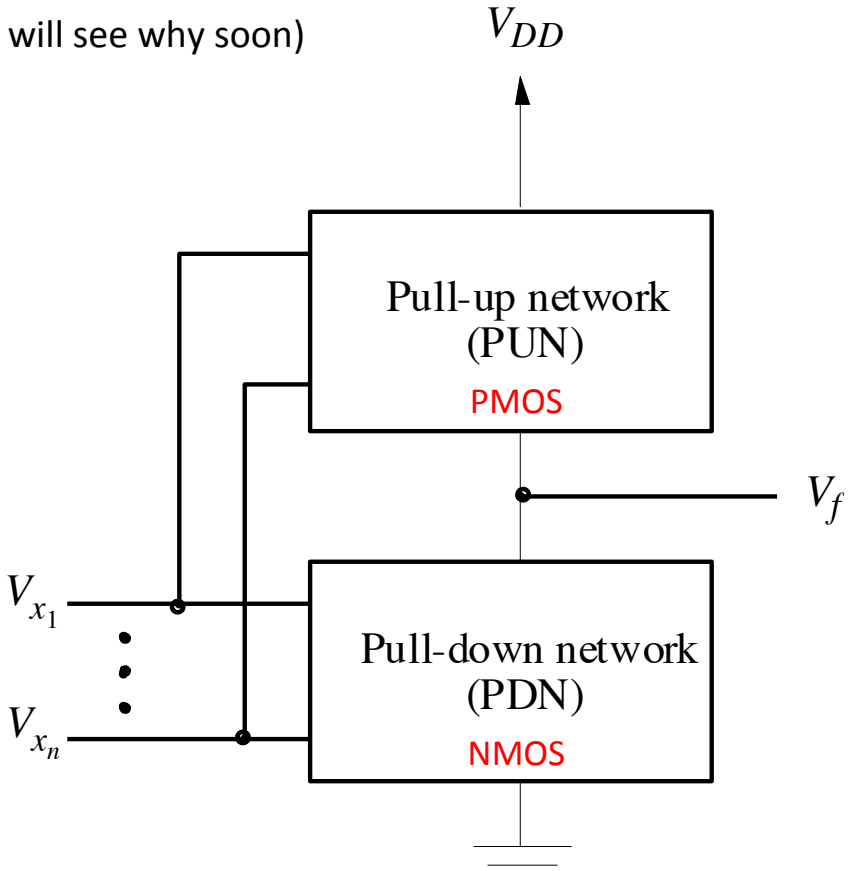
NMOS realization of an OR gate

CMOS Circuits

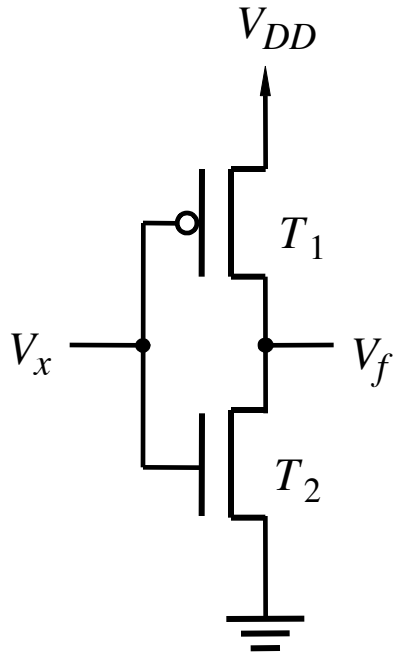
- Complementary MOS
  - uses NMOS and PMOS together
  - duals (same # transistors, series/parallel)
  - V_f either pulled up to V_{DD} or down to Gnd
  - Why CMOS? Lower power consumption ! (we will see why soon)



NMOS gate



CMOS gate

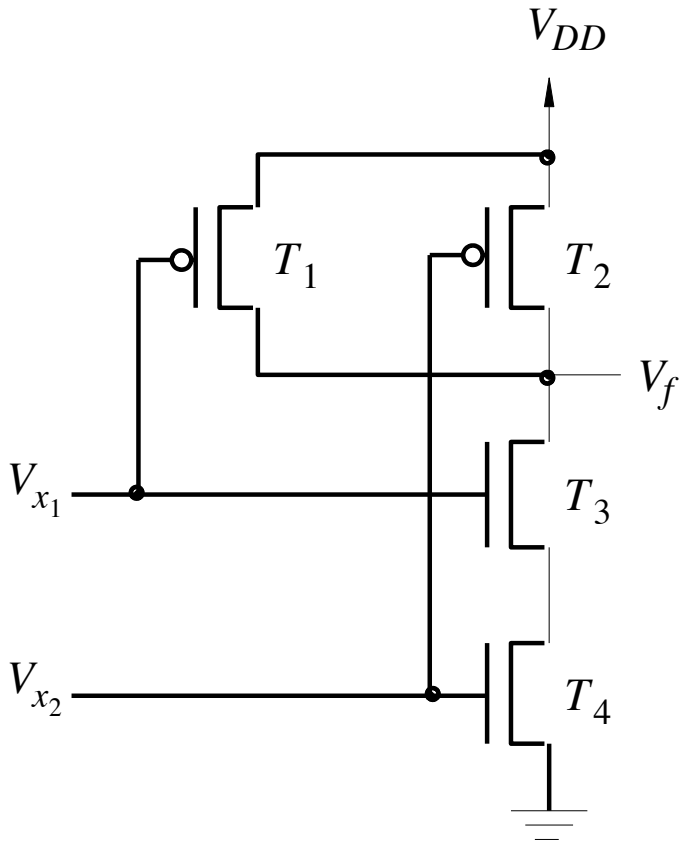


(a) Circuit

x	T_1	T_2	f
0	on	off	1
1	off	on	0

(b) Truth table and transistor states

CMOS realization of a NOT gate

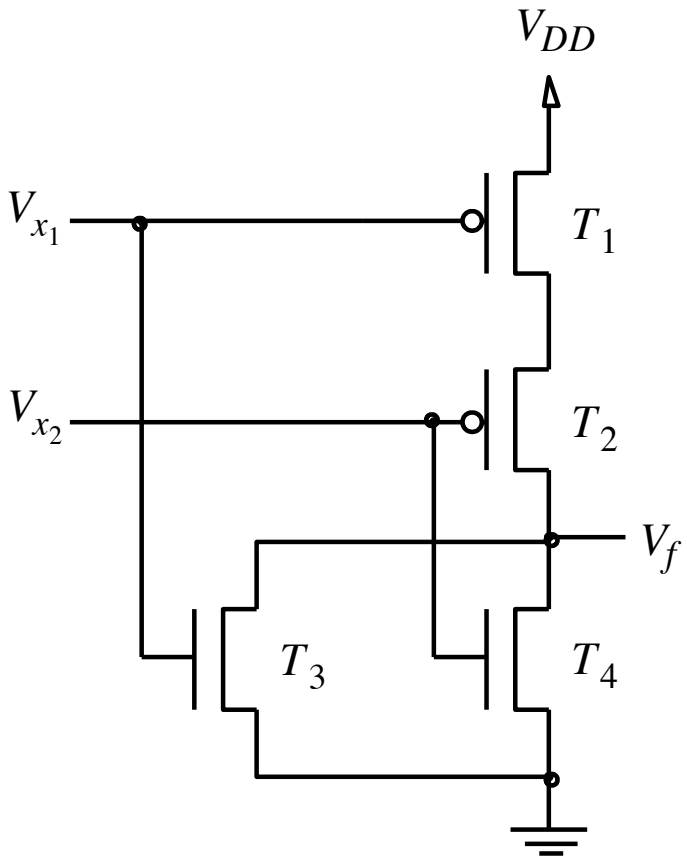


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	1
1	0	off	on	on	off	1
1	1	off	off	on	on	0

(b) Truth table and transistor states

CMOS realization of a NAND gate

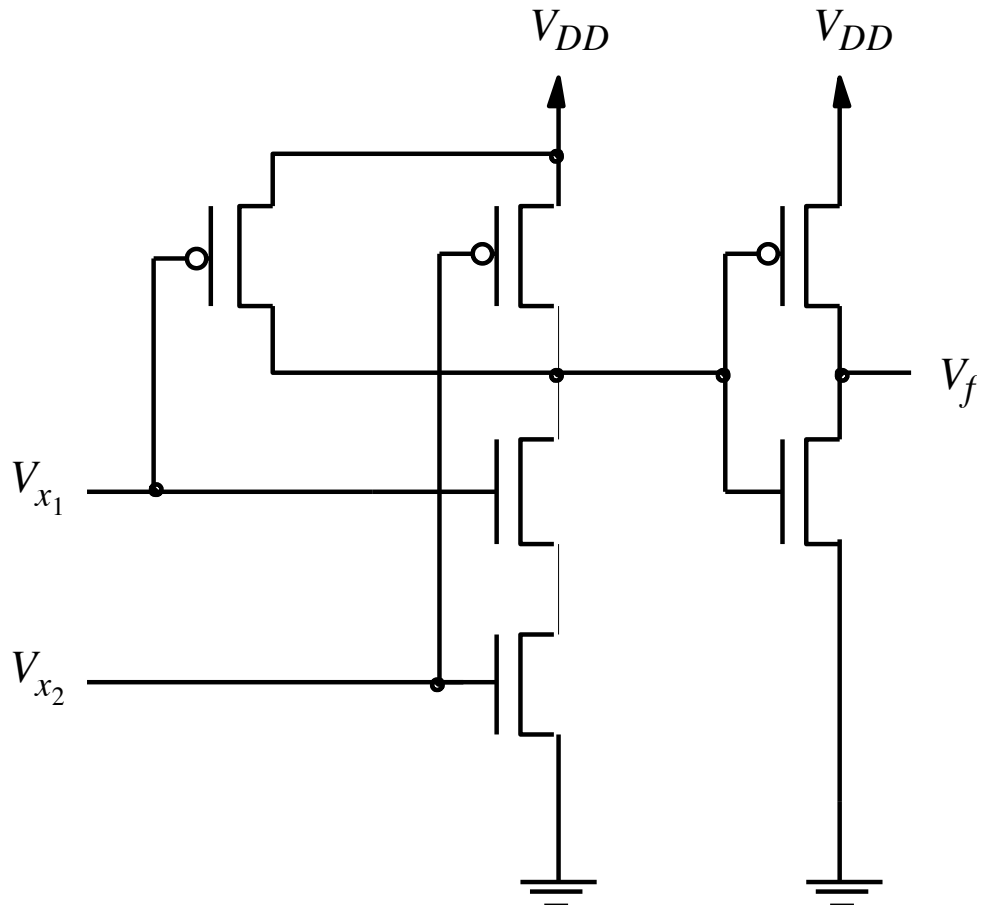


(a) Circuit

x_1	x_2	T_1	T_2	T_3	T_4	f
0	0	on	on	off	off	1
0	1	on	off	off	on	0
1	0	off	on	on	off	0
1	1	off	off	on	on	0

(b) Truth table and transistor states

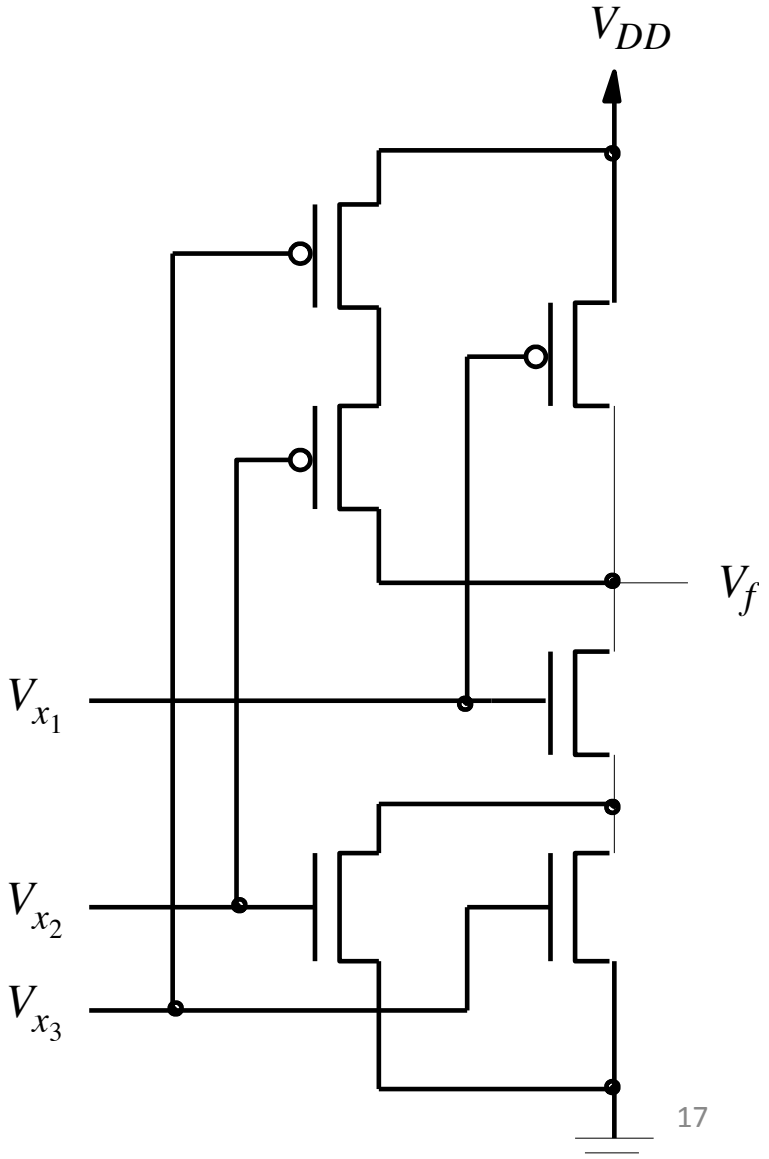
CMOS realization of a NOR gate



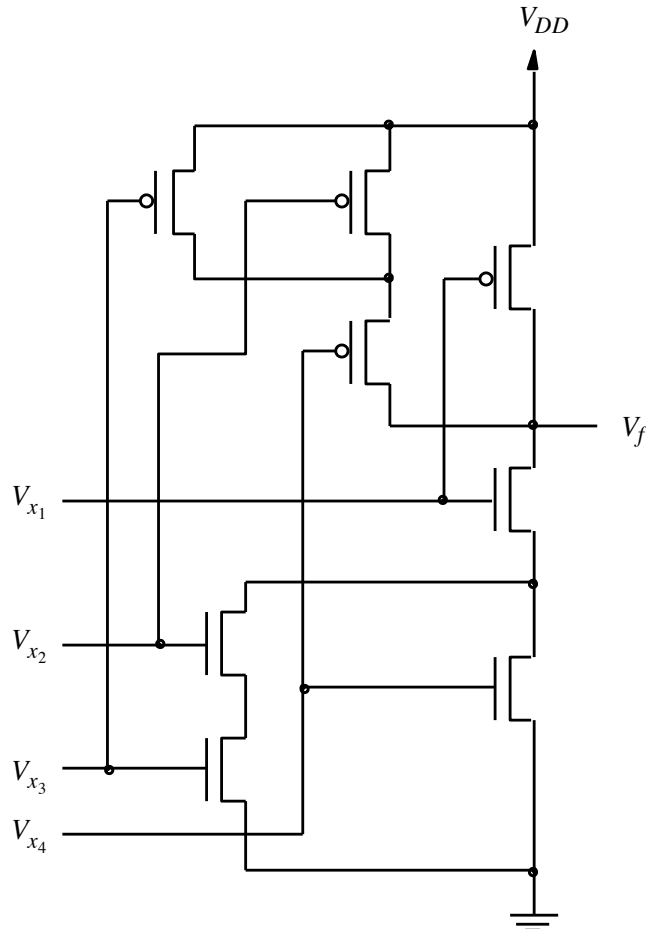
CMOS realization of an AND gate

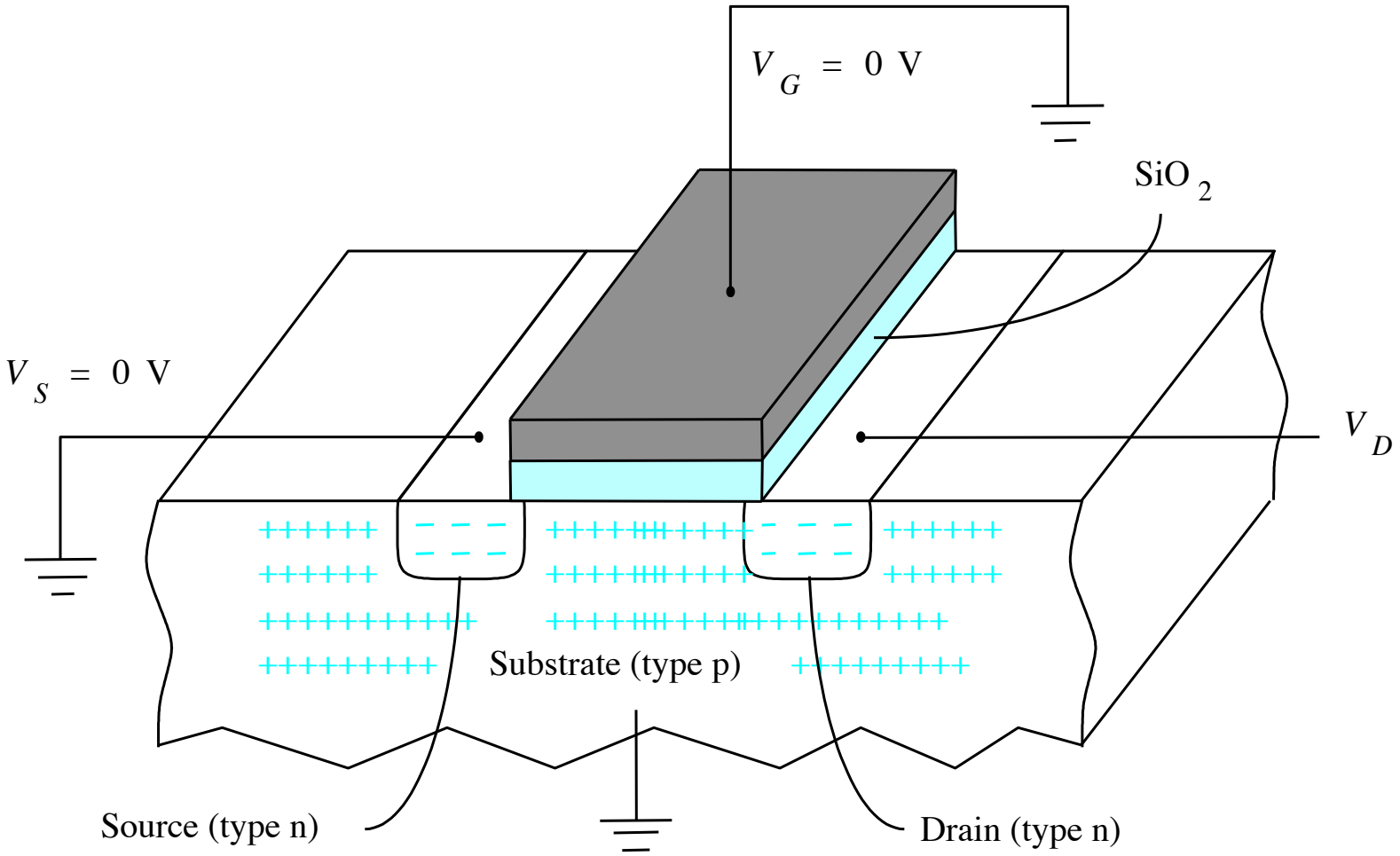
Example 1 (Complex CMOS Gate)

PDN: synthesize f’
PUN: synthesize f



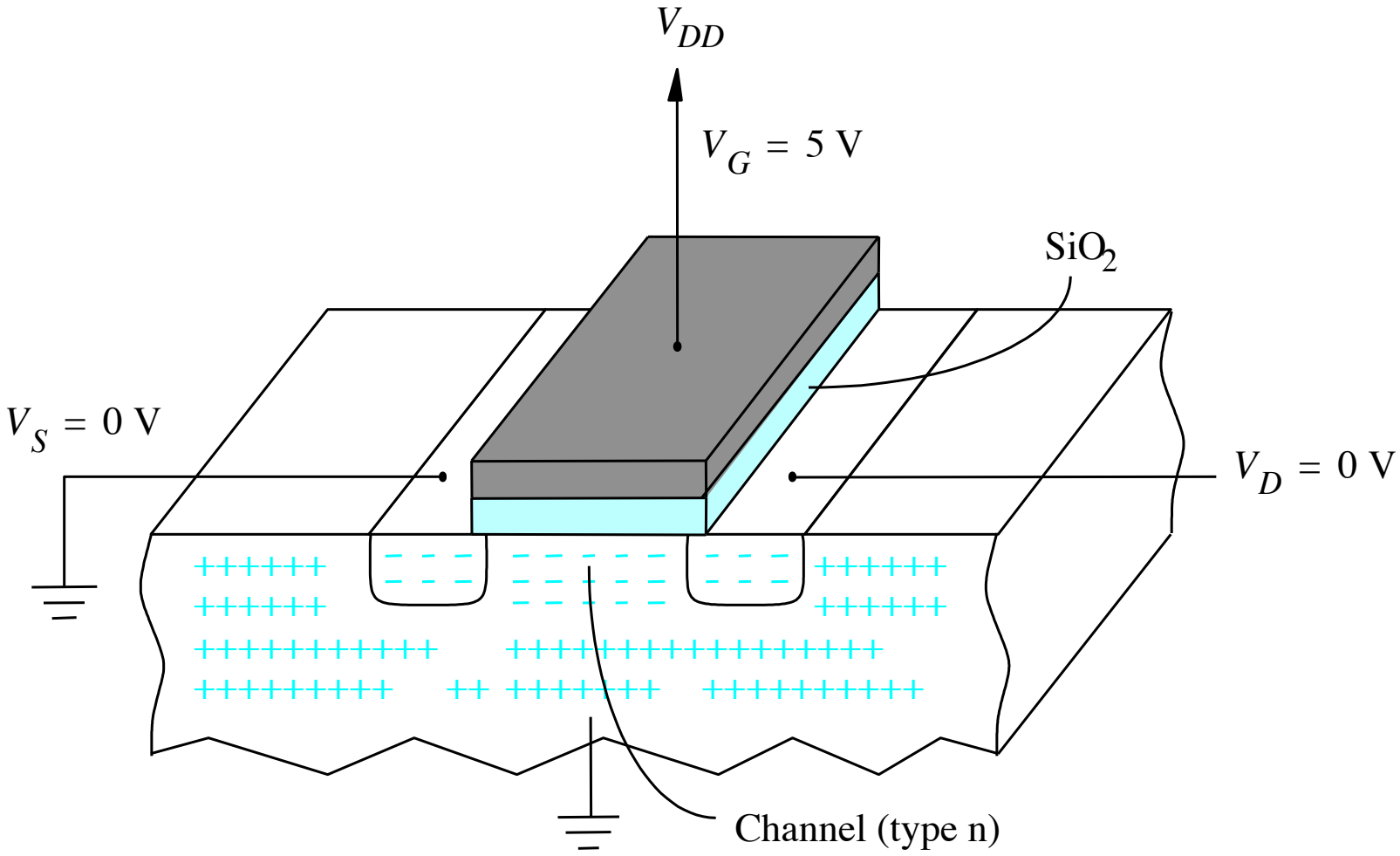
Example 2





(a) When $V_{GS} = 0$ V, the transistor is off

NMOS transistor when turned off



(b) When $V_{GS} = 5$ V, the transistor is on

NMOS transistor when turned on

$V_{GS} < V_T$ (threshold voltage) → Transistor is off

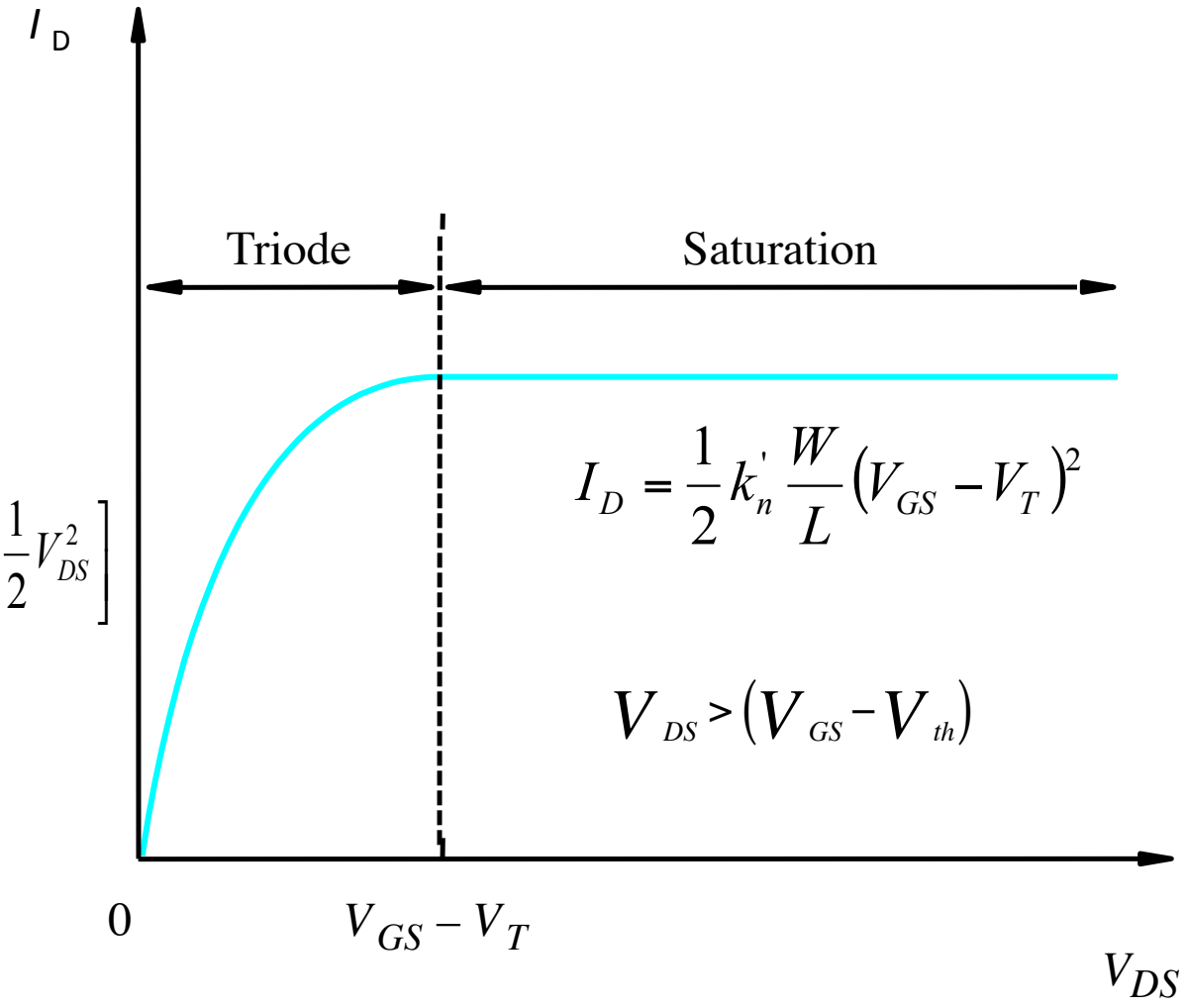
For $V_{GS} > V_t$, a current, I_D, may flow from the drain to the source

$$k_n' = \mu_n C_{ox}$$

$$\beta = k_n' \frac{W}{L}$$

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

$$V_{DS} < (V_{GS} - V_{th})$$



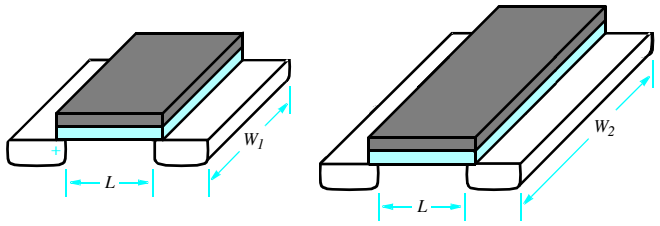
The current-voltage relationship in the NMOS transistor

PMOS

- Same behavior as NMOS, but all voltages and currents reversed
  - Source has higher voltage, V_t is negative.
- The conduction mechanism is different in a PMOS transistor, current does not flow as readily

$$k_p' \approx 0.4 k_n'$$

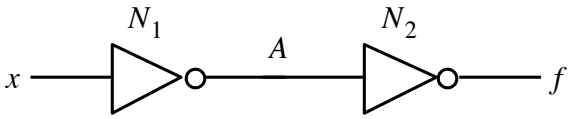
→ Size the W/L of the PMOS transistors 2 to 3 times larger than NMOS



(a) Small transistor (b) Larger transistor

Dynamic Operation of Logic Gates

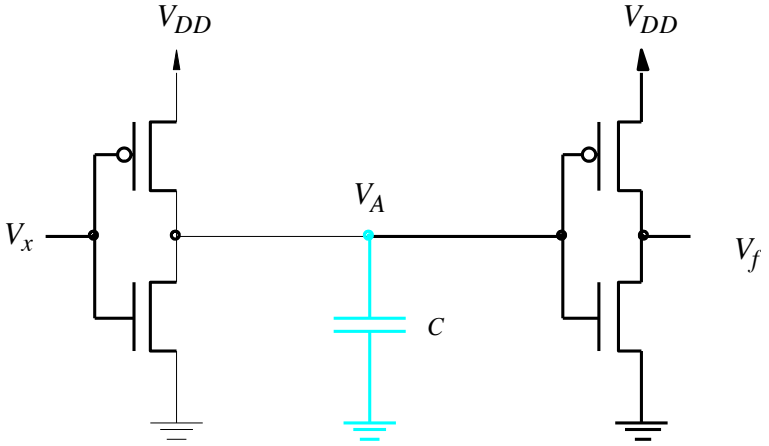
- Static – steady state
- Dynamic – when the transistor is switching



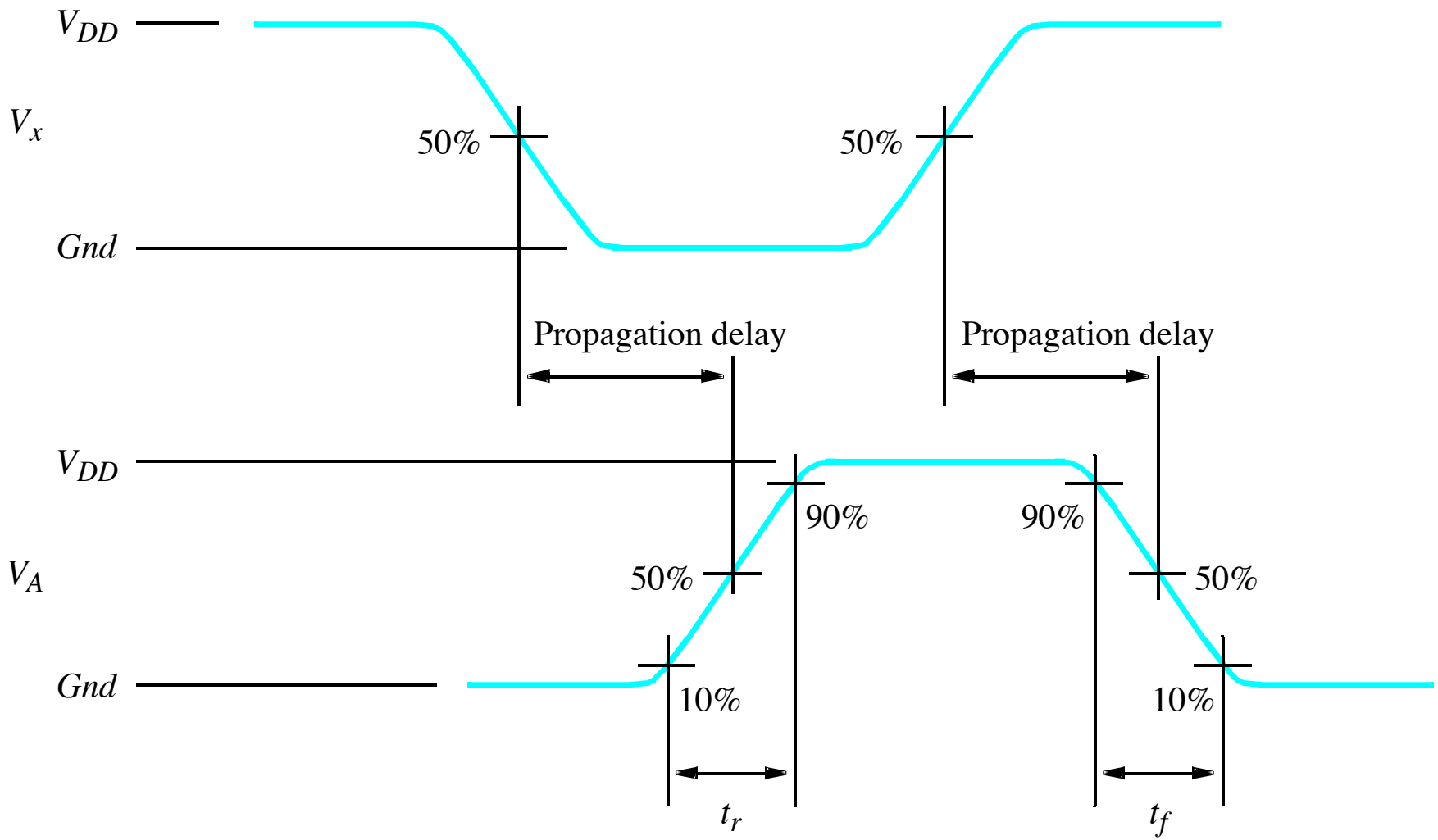
(a) A NOT gate driving another NOT gate

Parasitic capacitance at A caused by overlap of layers in the physical structure of the transistor (for example, the gate capacitance of N_2 is seen as an output capacitance to N_1)

This capacitor takes time to charge and discharge (depends on the current I_d and the value of the capacitance)

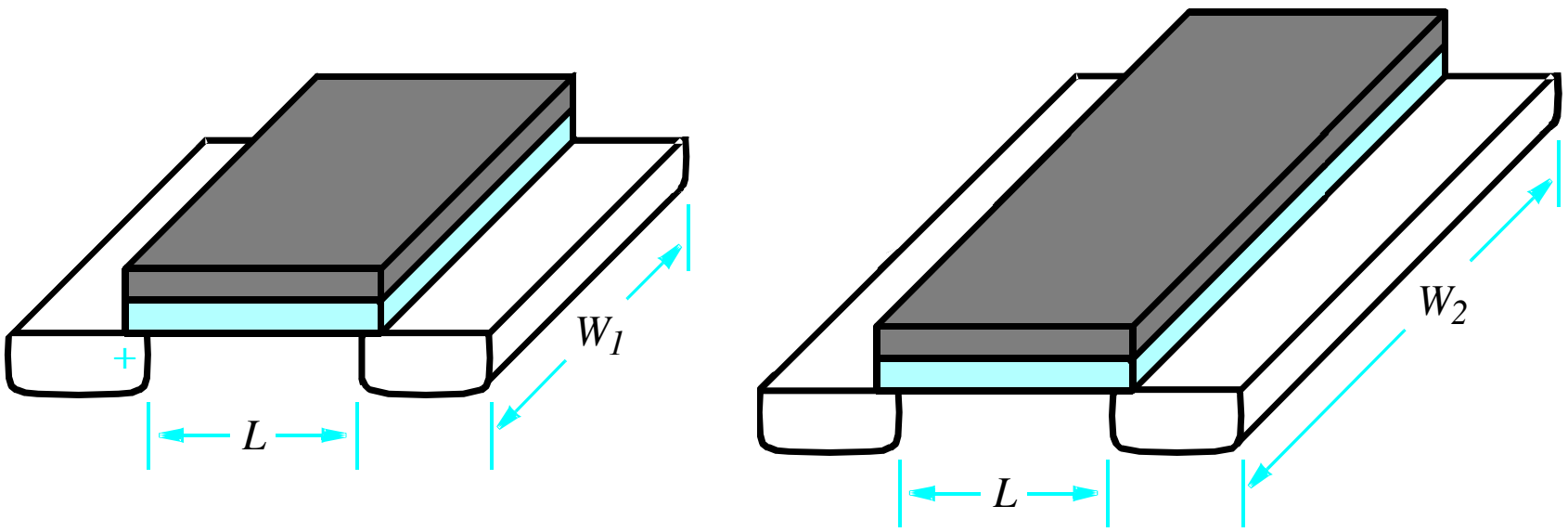


(b) The capacitive load at node A



Voltage waveforms for logic gates

Size the PMOS and NMOS (W and L) to make rise time and fall time roughly equal
L is usually set to the minimum (e.g. 45 nm)



(a) Small transistor

(b) Larger transistor

Transistor sizes

Power Dissipation

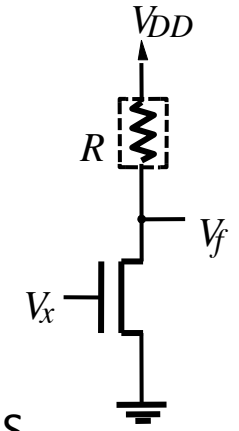
- Static power: power due to current flow when the gate is in steady state
- Dynamic power: power due to current flow when the gate is switching (signals changing)

- NMOS: when V_x = 0V, no current flows
  when V_x = 5V, current flows

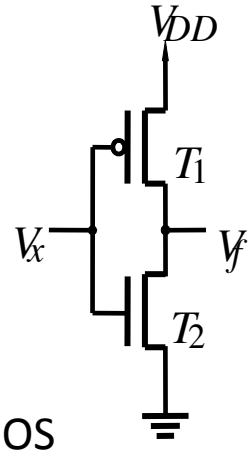
→ static power consumption !!

- CMOS: No current flows in steady state for either V_x = 0V or V_x = 5V
- --> zero static power consumption

(in theory! in reality there is some static power because in modern technologies the transistor never fully turns off and also there are other mechanisms such as current leaking through the gate) – solving these problems are important to continue scaling CMOS



NMOS

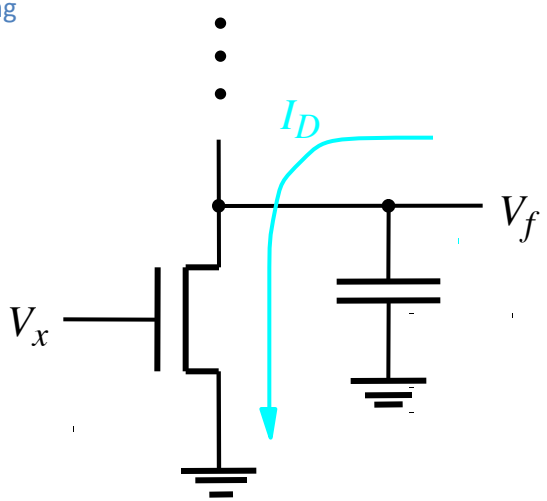


CMOS

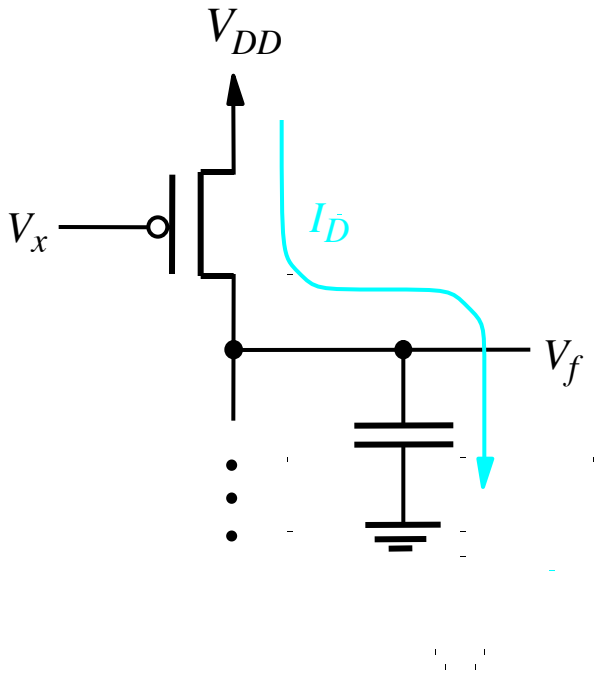
Dynamic Power

Currents flow to charge and discharge the parasitic capacitor

There is also a small short-circuit current that flows for a short time when both transistors are on during switching



(a) Current flow when input V_x changes from 0 V to 5 V



(b) Current flow when input V_x changes from 5 V to 0 V

See Example 3.12 to find out why the energy stored in the capacitor is $(1/2)CV_{DD}^2$ J

Every charge-discharge cycle dissipates CV_{DD}^2 J

$$P_D = fCV_{DD}^2$$

Example

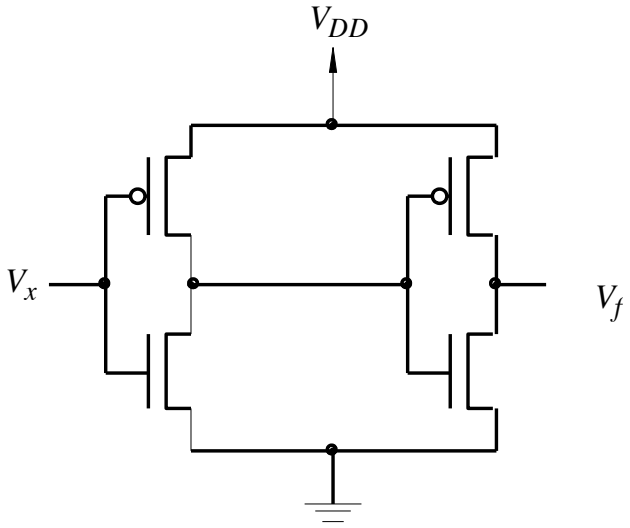
- If C = 70 fF and f = 100 MHz, the dynamic power consumed by a gate is 175 μW.

- If the chip has the equivalent of 10,000 inverters and on average 20% of the gates change values at any given time then the total dynamic power used in the chip is

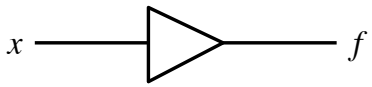
$$P_D = 0.2 \times 10,000 \times 175\mu W = 0.35W$$

Buffers

- When a logic gate has to drive a large capacitive load, it can be slow
- Use a buffer (f = x) to improve performance
- Buffers usually are designed with large transistors to drive a large current
  - Used for driving long wires on the chip or for driving signals off the chip
- Often inserted by the CAD tools to meet performance goals



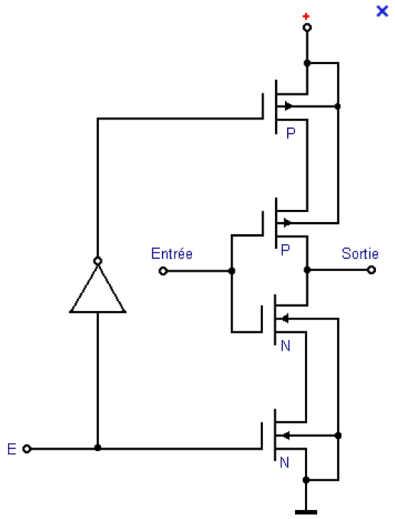
(a) Implementation of a buffer



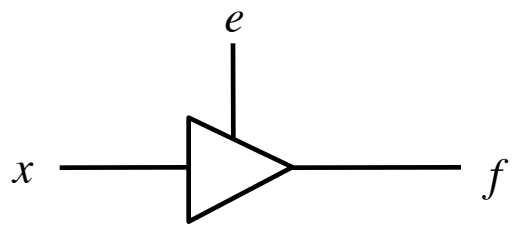
(b) Graphical symbol

Tri-State Buffers

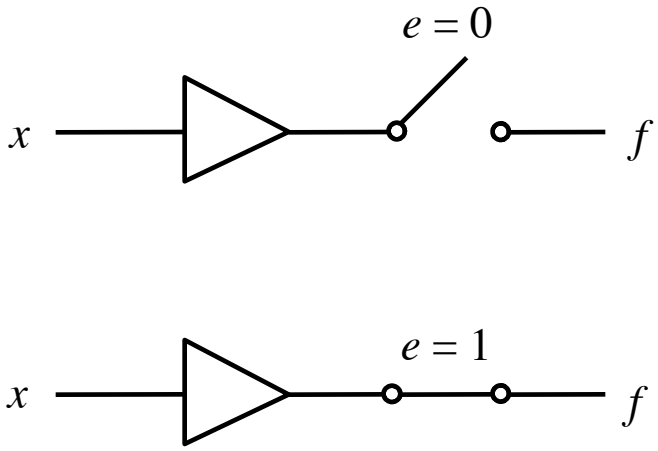
- When the control signal “enable” is low the buffer is completely disconnected from the output f
  - When e is high, the buffers drives x onto f
  - The disconnected state “Z” is “high impedance”



e	x	f
0	0	Z
0	1	Z
1	0	0
1	1	1



(a) A tri-state buffer



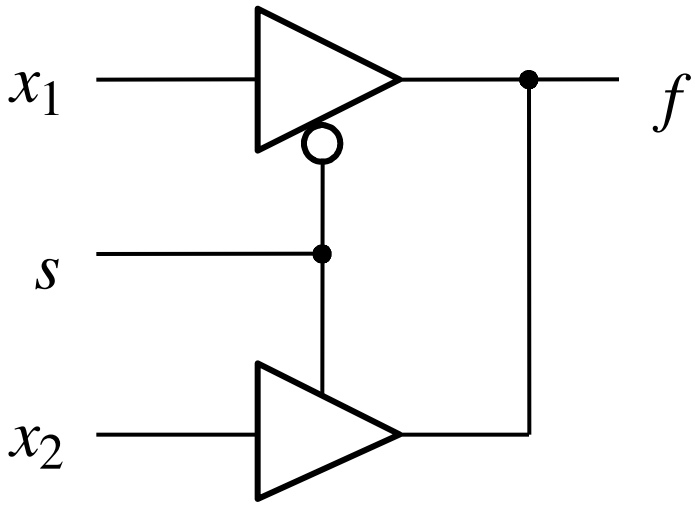
(b) Equivalent circuit

Application of Tri-State Buffers

- Be careful! Connecting two gates ("drivers") to the same line can short V_{DD} and Gnd! The CAD tools should warn you if this happens (although nothing stops you from doing this when connecting chips on a board).

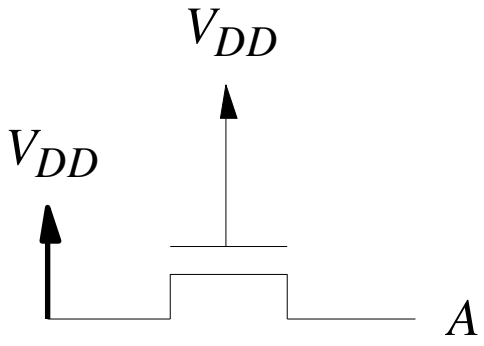
- This is not the only way to choose signals (e.g. you can use multiplexers which we introduce in the next chapter)
  - Some technologies (e.g. FPGAs) may or may not have tri-states and if so, may only have them in certain places (e.g. output pins)

- Used in some cases, such as driving a common bus

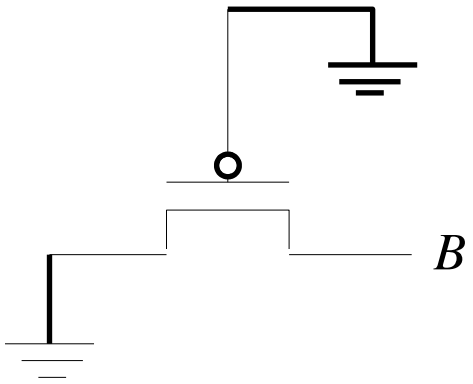


Transmission Gates

- Why can't we use a single transistor as a switch and build logic out of that?
  - A single NMOS passes a '0', but doesn't fully pass a '1' (only pulls up to $V_{DD} - V_t$)
  - A single PMOS passes a '1', but doesn't fully pass a '0' (only pulls down to V_t)



(a) NMOS transistor

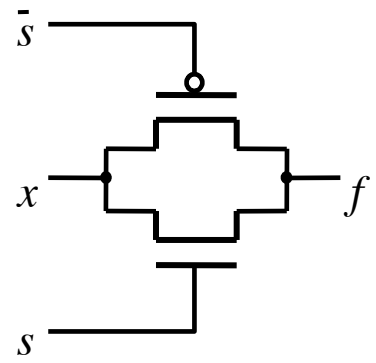


(b) PMOS transistor

- The solution is to use both a NMOS and a PMOS to build the switch → Transmission Gate

- Only one (the appropriate) transistor is on for x = 0 or x= 1

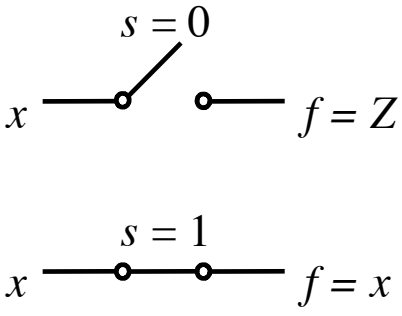
- Can be used as alternative style for implementing logic circuits compared to "static CMOS" gates



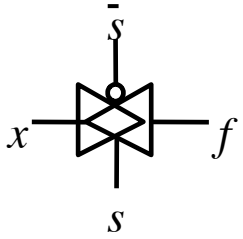
(a) Circuit

s	f
0	Z
1	x

(b) Truth table



(c) Equivalent circuit



(d) Graphical symbol