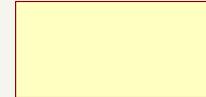


A

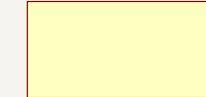
Programmable Logic (PL)

Bank 34 (3.3V)



File: pl_bank34.kicad_sch

Bank 35 (1.8V)



File: pl_bank35.kicad_sch

HDMI



File: pl_hdmi.kicad_sch

Audio CODEC



File: pl_codec.kicad_sch

PL Configuration



File: pl_config.kicad_sch

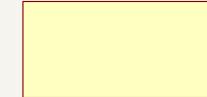
FTDI



File: ftdi.kicad_sch

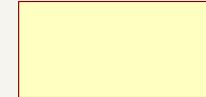
Processing System (PS)

PS IO pins



File: ps_gpio.kicad_sch

USB HS PHY



File: ps_usb.kicad_sch

DRAM DDR3



File: ps_ddr3.kicad_sch

Gigabit Ethernet PHY



File: ps_eth.kicad_sch

PS Configuration



File: ps_config.kicad_sch

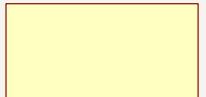
SD Card + QSPI Flash



File: ps_sd_qspi.kicad_sch

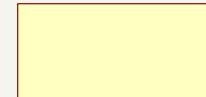
Power Block

Power Sequence



File: power_seq.kicad_sch

SoC Power Pins



File: power_pins.kicad_sch

BMS

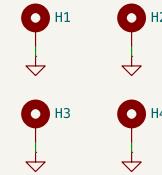


File: bms.kicad_sch

PMIC



File: pmic.kicad_sch



Sheet: /

File: zynq7000.kicad_sch

Title: FPGA Zynq7000 Dev Board

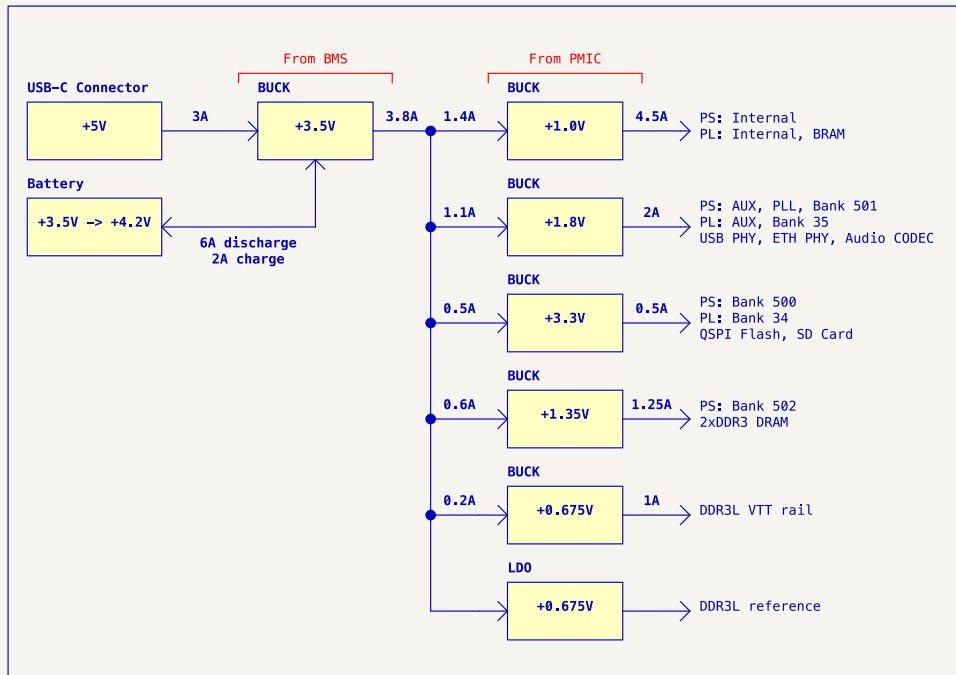
Size: A4 | Date: 2025-07-10

KiCad E,D,A. 9.0.3

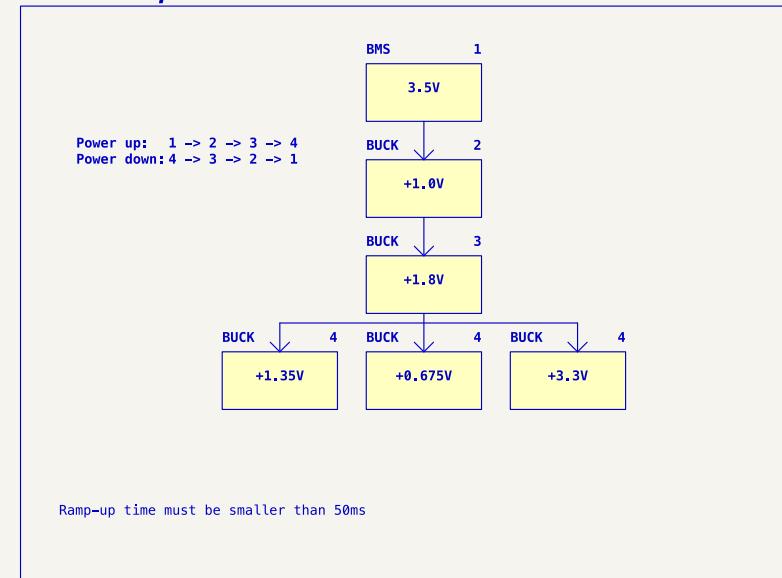
Rev: A

Id: 1/17

A

Power Tree

B

Power Sequence

C

D

Sheet: /Power Sequence/
File: power_seq.kicad_sch

Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 2/17

A

A

B

B

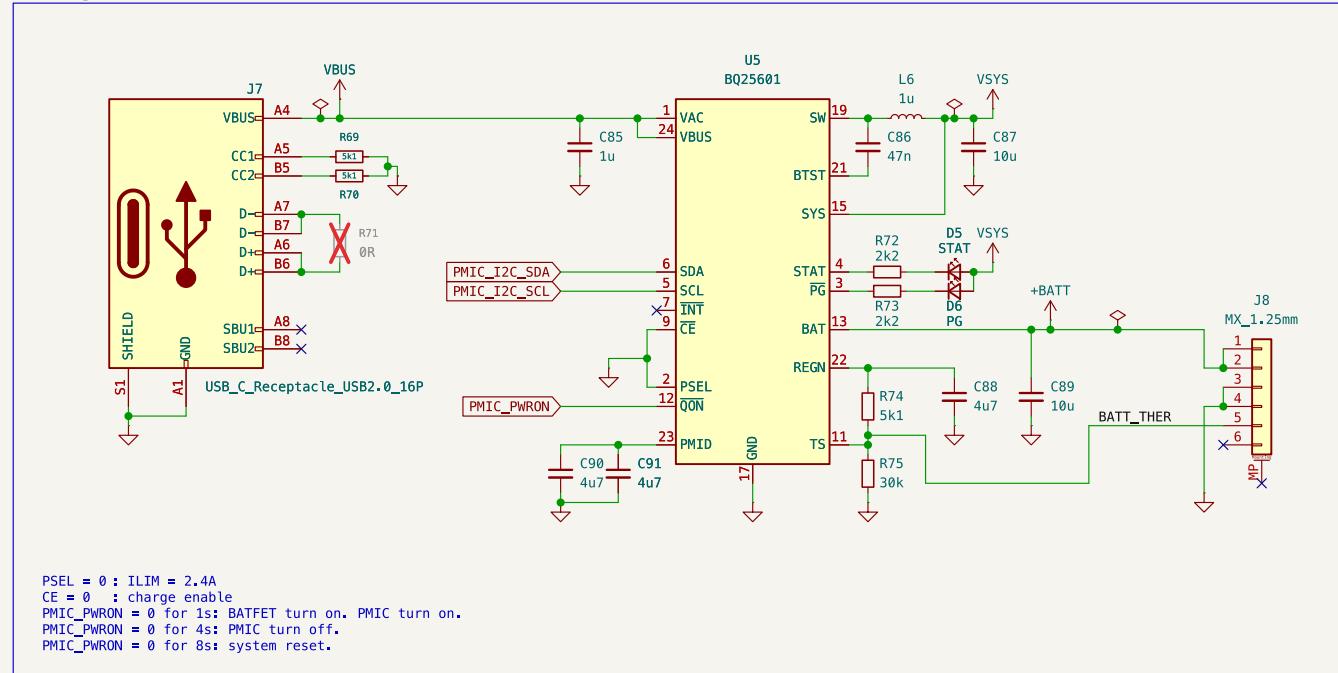
C

C

D

D

Charger



Sheet: /BMS/
File: bms.kicad_sch

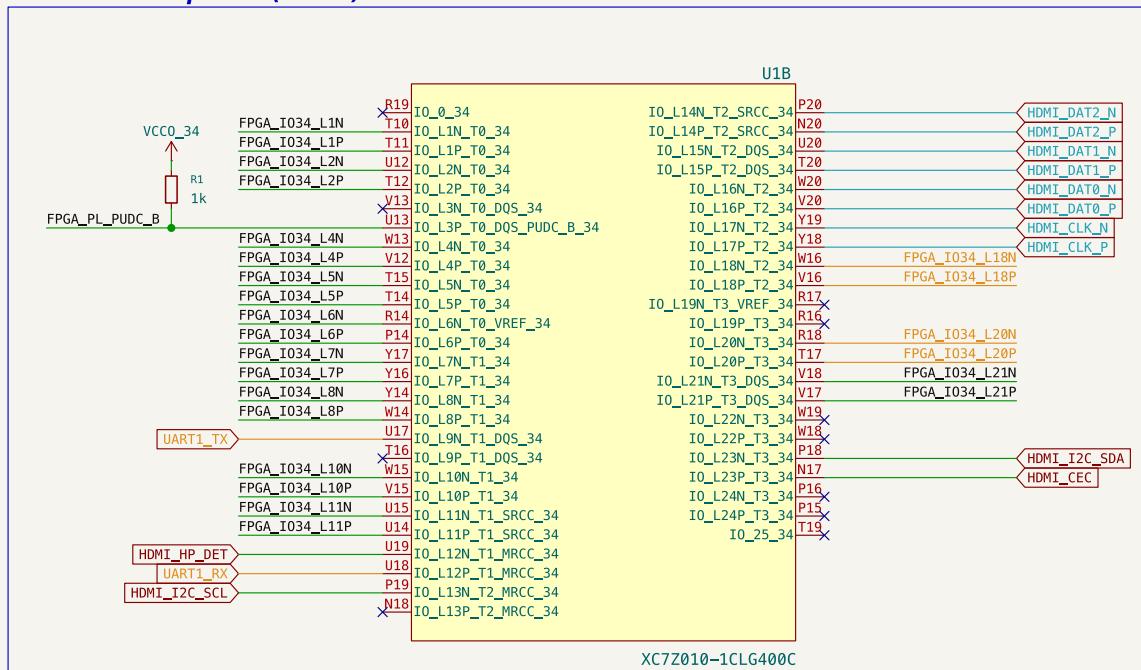
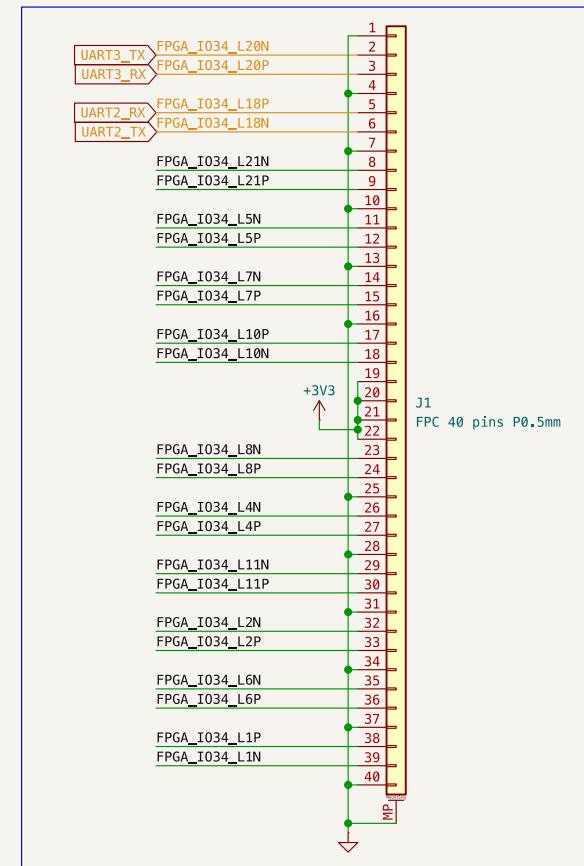
Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 10/17

Bank 34 IO pins (3.3V)**Extended connector**

Sheet: /Bank 34 (3.3V)/
File: pl_bank34.kicad_sch

Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 3/17

A

A

B

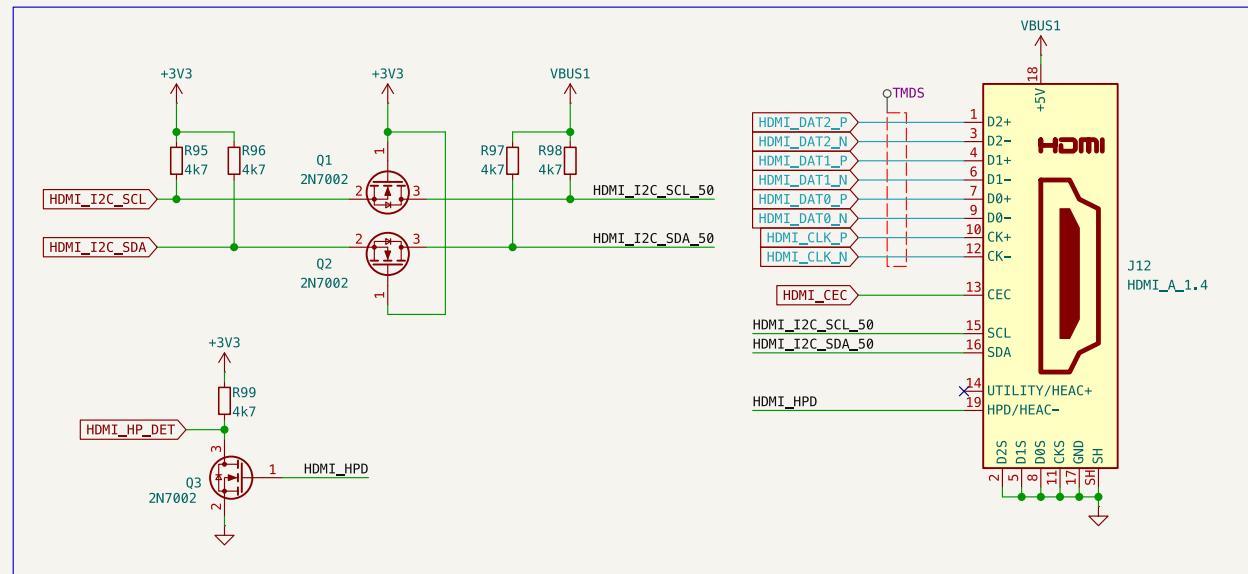
B

C

C

D

D

HDMI

Sheet: /HDMI/
File: pl_hdmi.kicad_sch

Title: **FPGA Zynq7000 Dev Board**

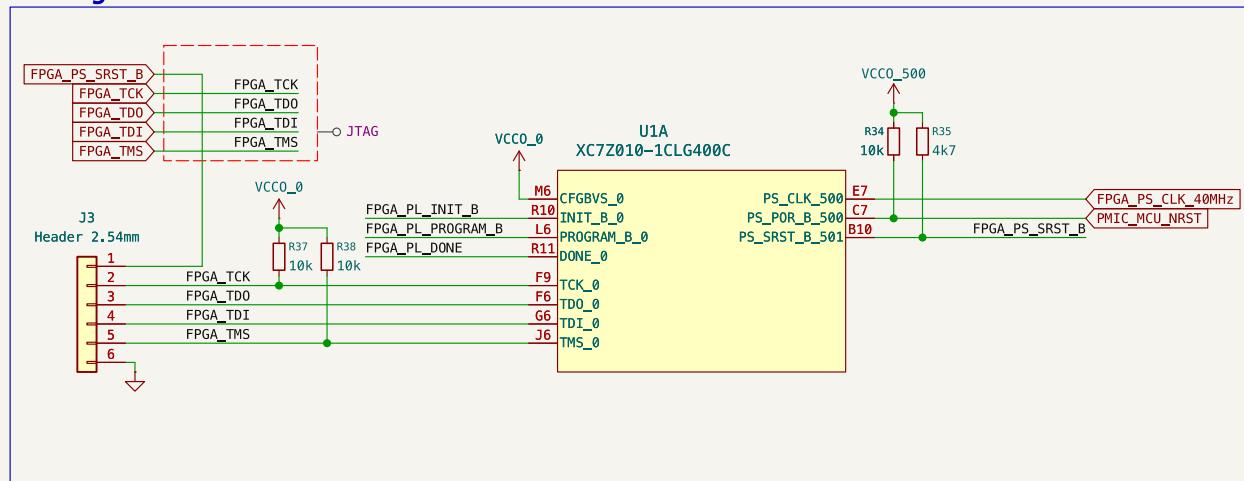
Size: A4 | Date: 2025-07-10

KiCad E,D,A. 9.0.3

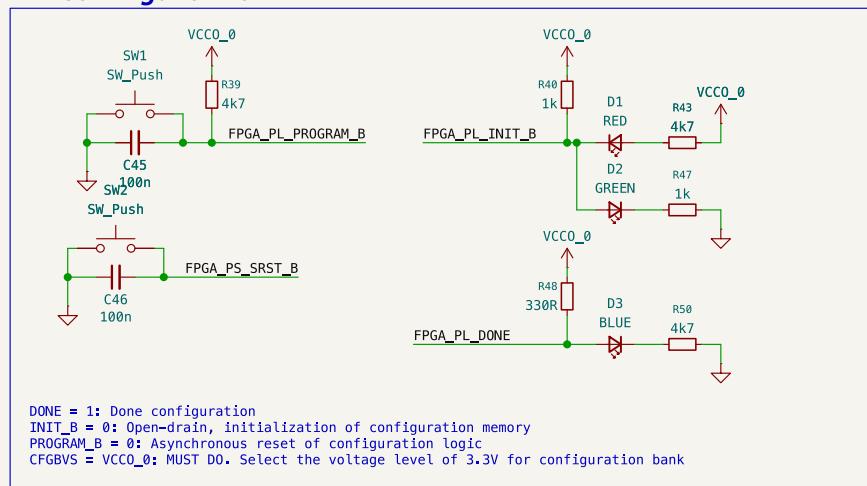
Rev: A

Id: 16/17

Configuration Block and JTAG conn.



PL Configuration



OK PS_POR_B input is required to be asserted to GND during the power-on sequence
OK The PS system reset (PS_SRST_B) is an active-Low signal that is mostly used for debugging proposes.
OK PS_SRST_B must be High for begin the boot process
OK 30MHz < PS_CLK < 60MHz
OK TMS and TCK have 10k pull up
OK PROGRAM_B pull up
OK INIT_B: 0 when init, error. 1 when done. pull up < 4k7

Sheet: /PL Configuration/
File: pl_config.kicad_sch

Title: FPGA Zynq7000 Dev Board

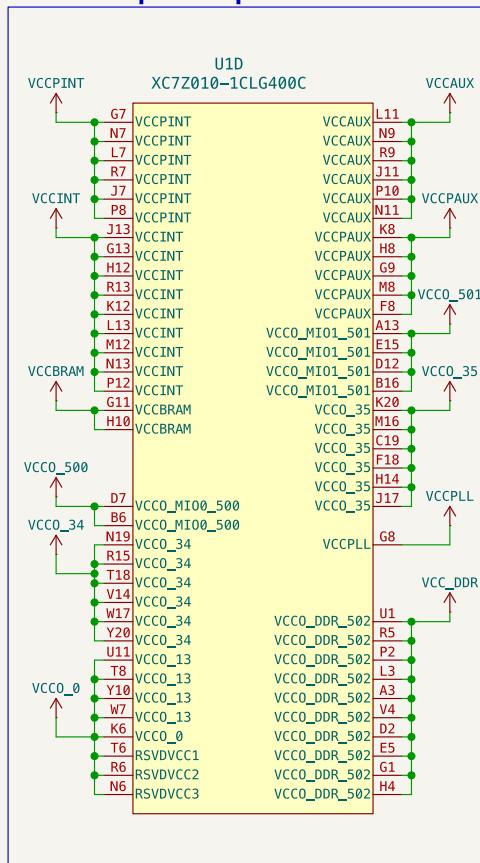
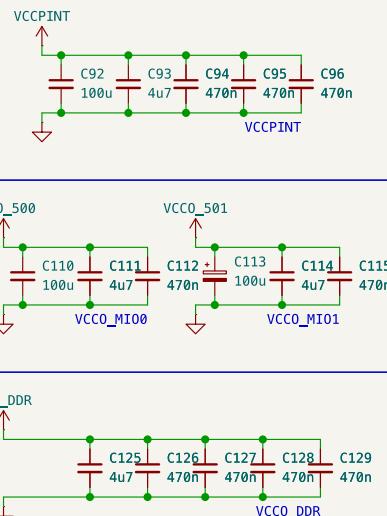
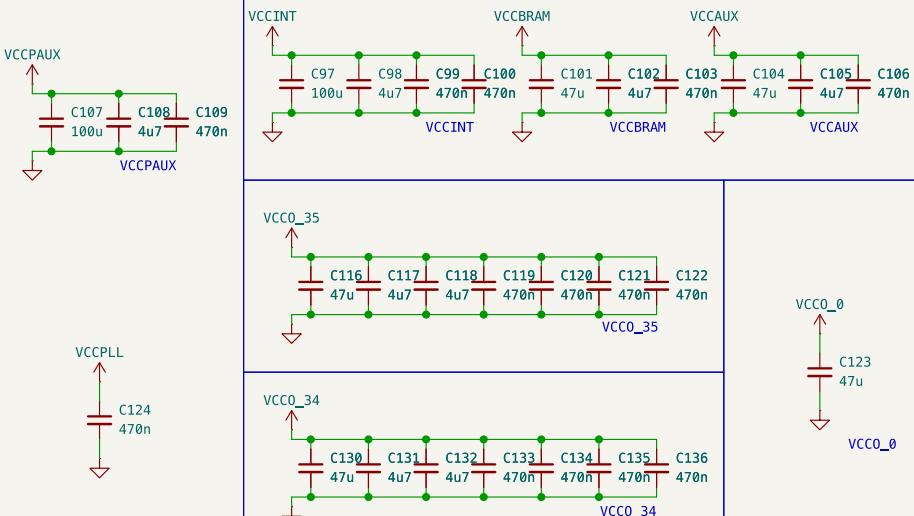
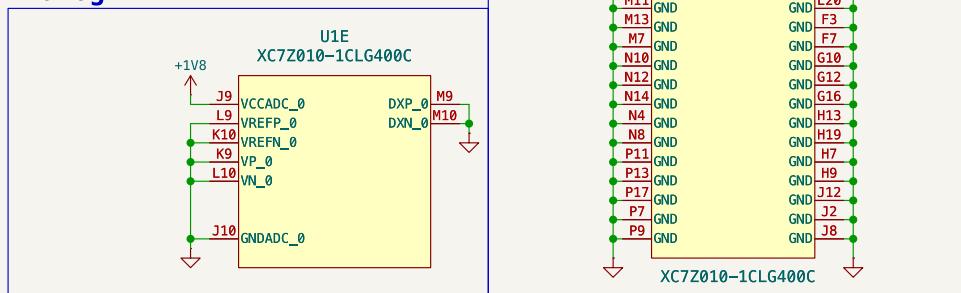
Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 6/17

1 2 3 4 5 6

XC7Z010 power pins**PS Bypass Caps.****PL Bypass Caps.****Analog**

Sheet: /SoC Power Pins/
File: power_pins.kicad_sch

Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

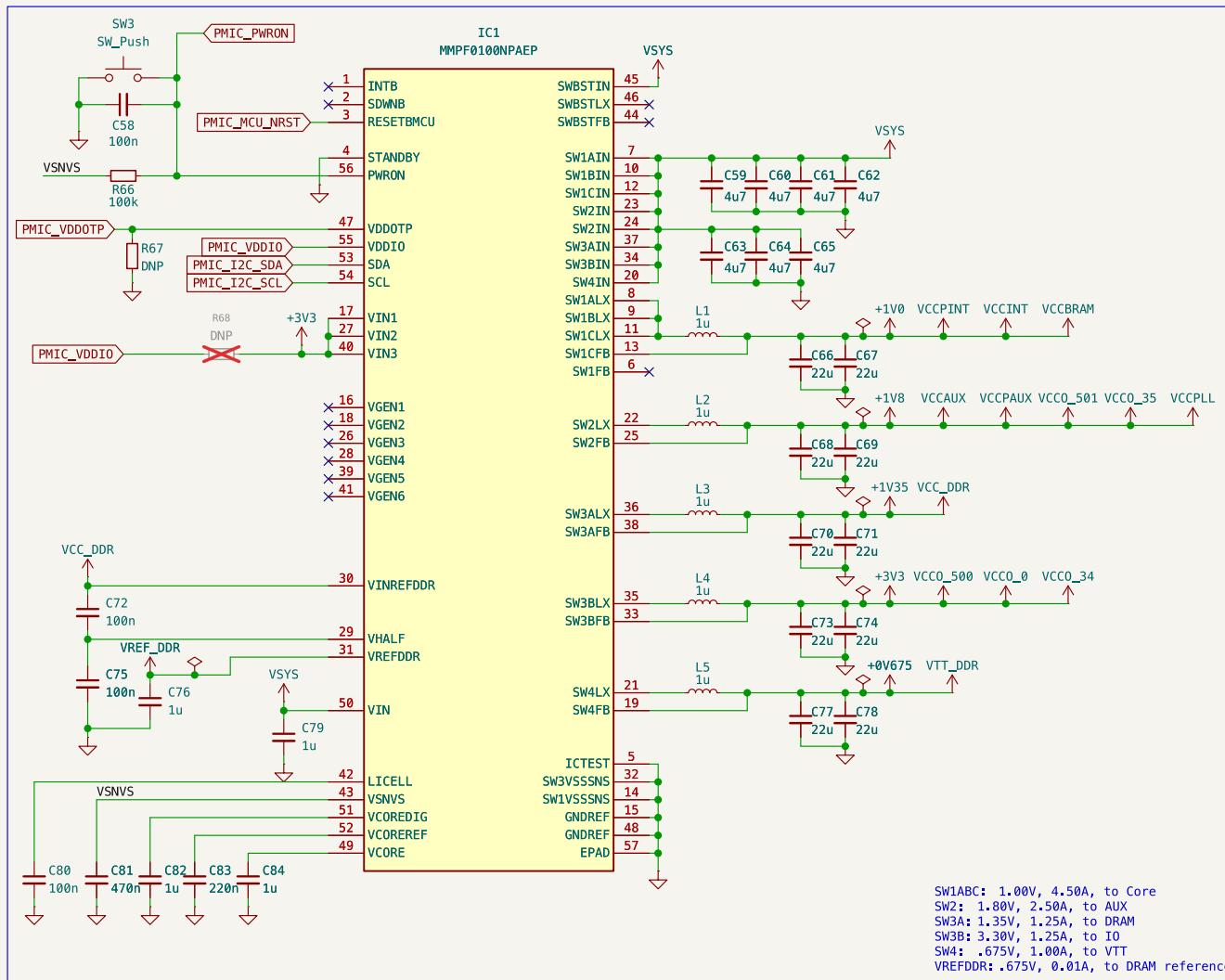
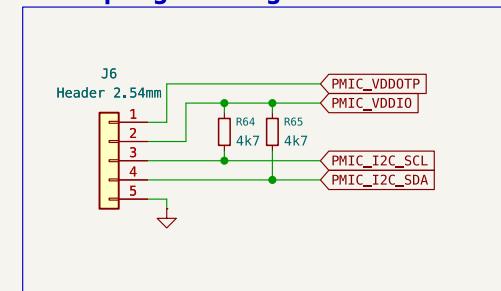
KiCad E,D,A. 9.0.3

Rev: A

Id: 11/17

1 2 3 4 5 6

1 2 3 4 5 6

PMIC**PMIC programming header**

OK INTB, SDWNB: Leave floating
 OK RESETBMU: Pull up to 3.3V (< Vin) with 100k.
 OK STANDBY, ICTEST = GND
 OK SW1ABC single phase mode
 OK SW1FB floating
 OK SW1CFB real feedback
 OK VIN123 connected to V < 3.4V
 OK L1CELL bypass with 0.1u
 OK VSNVS bypass with 0.47u
 OK SWBTFB floating
 OK SWBSTITN to VIN
 OK SWBTLX floating
 N/A VDDOTP connected to VCOREDIG with 100k for default mode
 OK Connect to ground in fuse mode
 OK Connect to 8.0V to program
 OK VCORE 1u
 OK VIN 1u
 OK VCOREDIG 1u
 OK VCOREREF 0.22u
 OK SDA SCL pull to VDDIO
 OK VDDIO = 3.3V. Bypass 0.1u
 OK PWRON. Pull up to VSNVS
 RESETBMU: In its default mode, it is de-asserted 2.0 ms to 4.0 ms after the last regulator in the start-up sequence is enabled;
 OK Power on: PWRON transitions from high to low
 OK Power off: PWRON is held low for longer than 4.0 seconds.

Sheet: /PMIC/
 File: pmic.kicad_sch

Title: FPGA Zynq7000 Dev Board

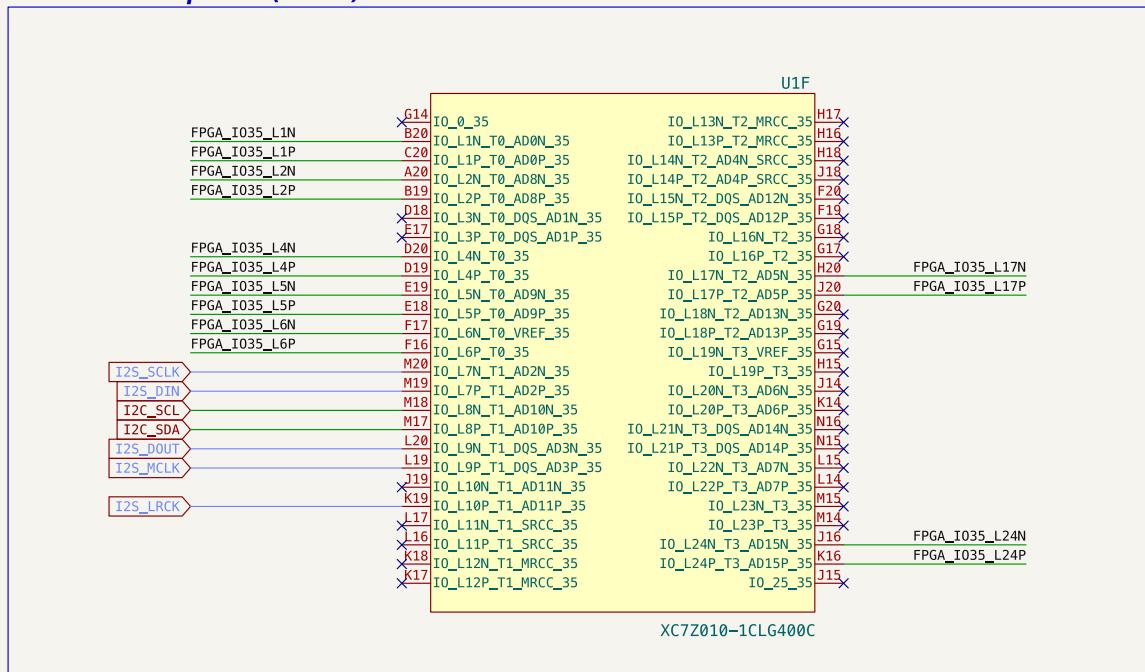
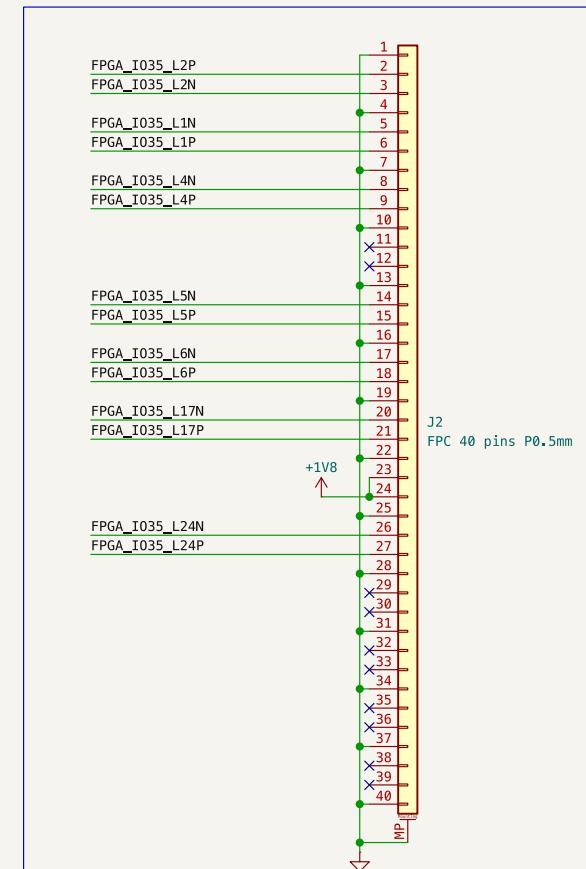
Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 9/17

1 2 3 4 5 6

Bank 35 IO pins (1.8V)**Extended connector**

Sheet: /Bank 35 (1.8V)/
File: pl_bank35.kicad_sch

Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 4/17

A

A

B

B

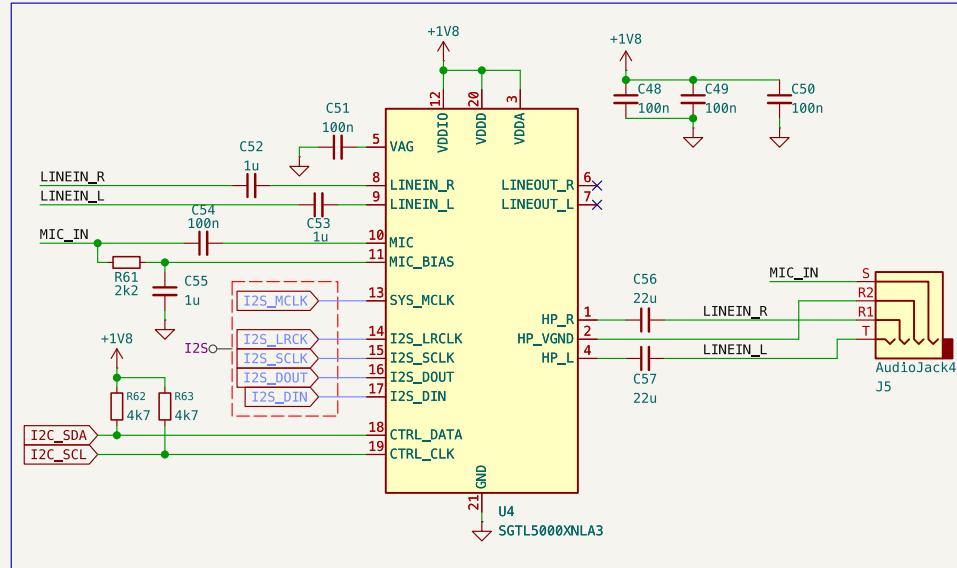
C

C

D

D

Audio CODEC



Sheet: /Audio CODEC/
File: pl_codec.kicad_sch

Title: FPGA Zynq7000 Dev Board

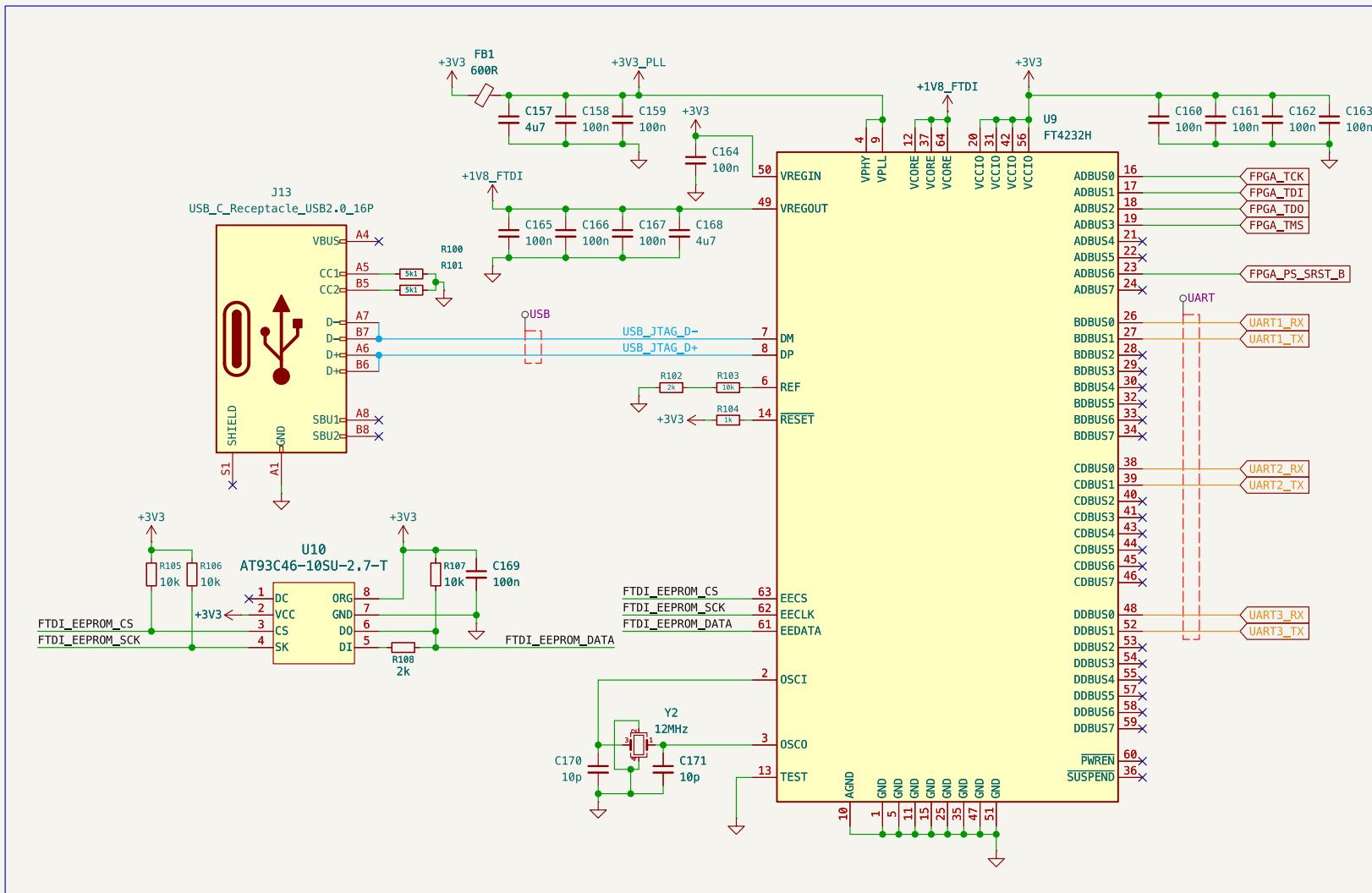
Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 8/17

FTDI USB-JTAG



Sheet: /FTDI/
File: ftdi.kicad_sch

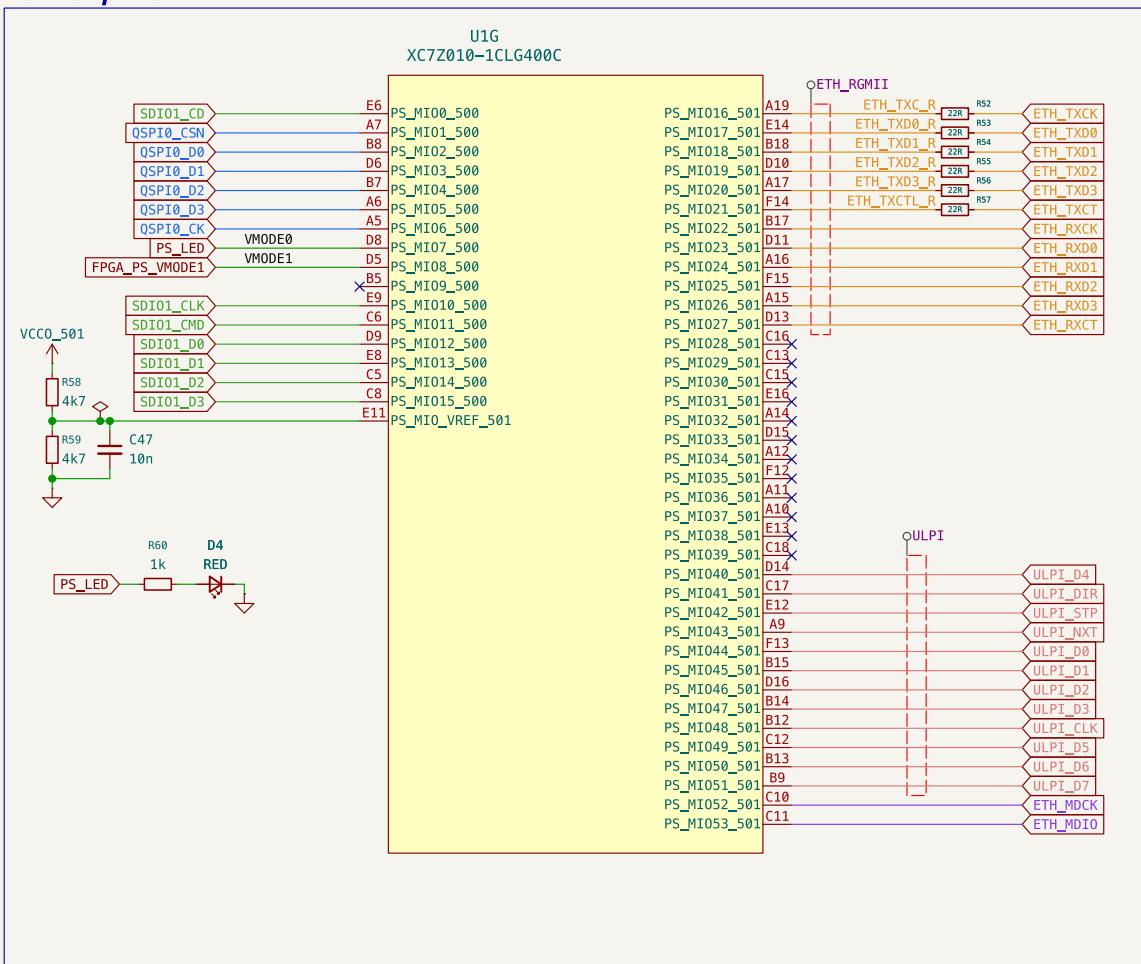
Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 15/17

PS IO pins

Sheet: /PS IO pins/
File: ps_gpio.kicad_sch

Title: **FPGA Zynq7000 Dev Board**

Size: A4 Date: 2025-07-10

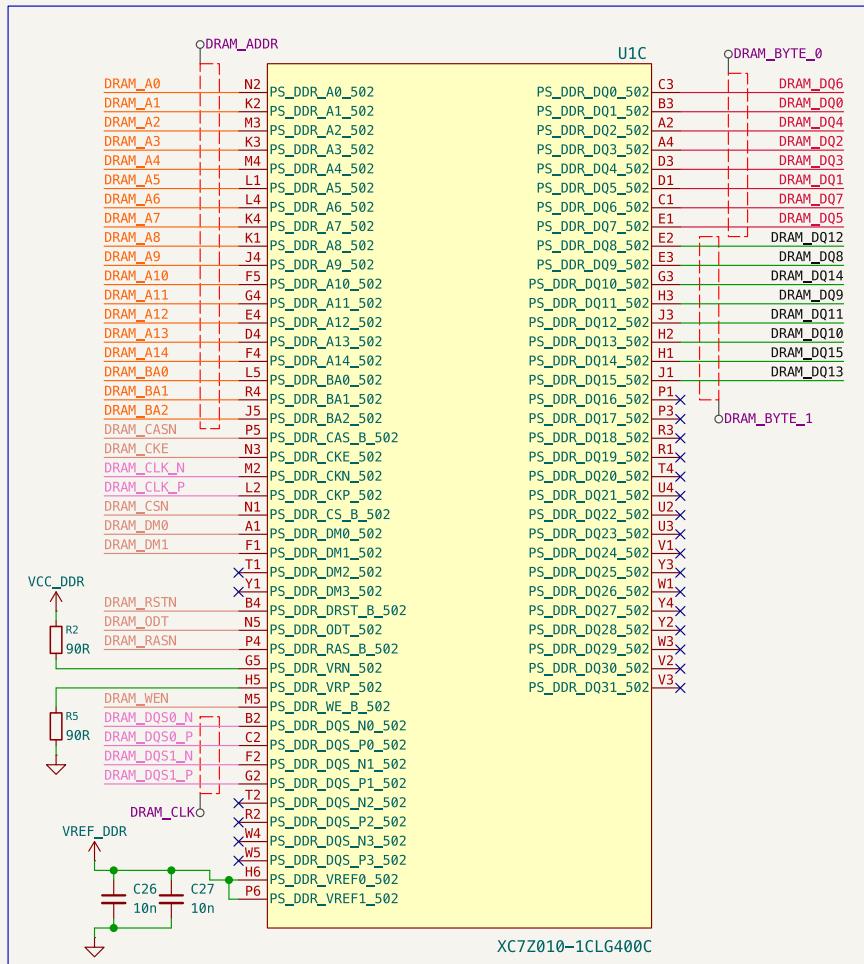
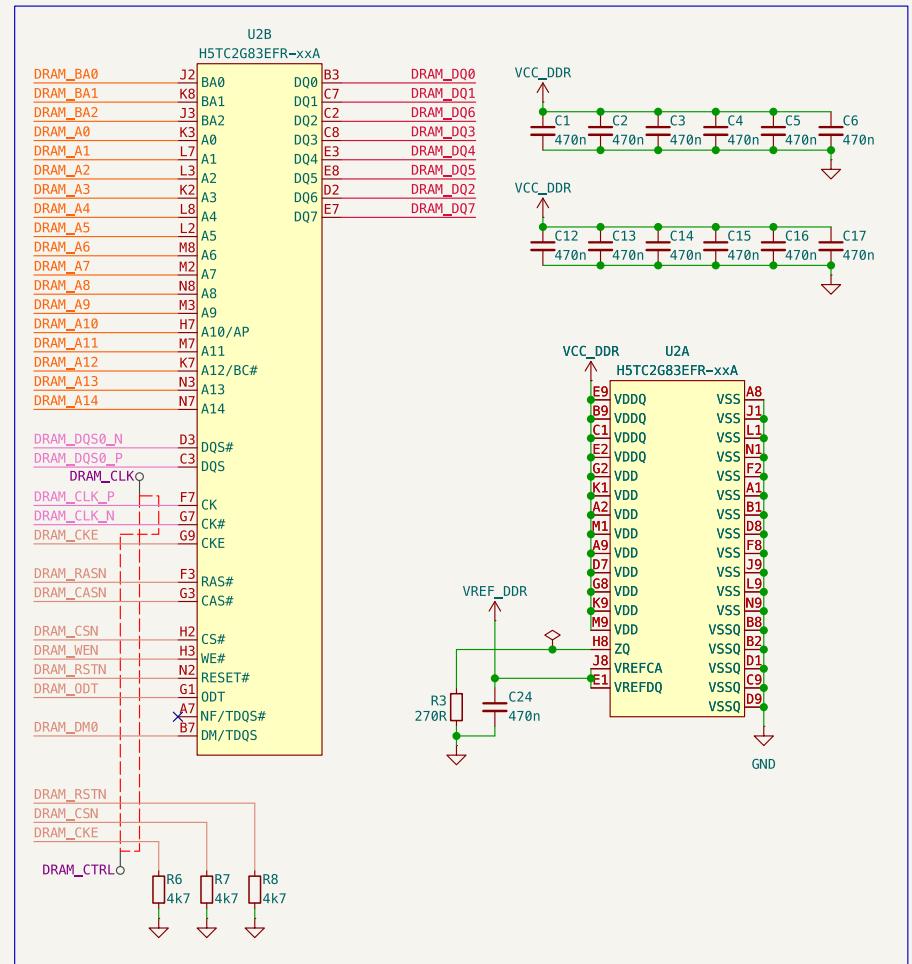
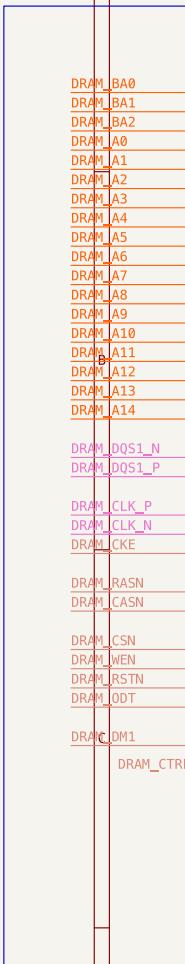
KiCad E,D,A. 9.0.3

Rev: A

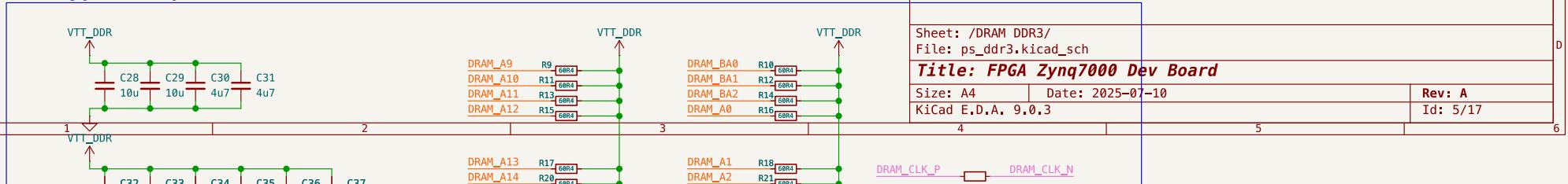
Id: 7/17

1 2 3 4 5 6

A

DRAM Controller**DDR3L-1****DDR3L-2**

D

VTT bypass cap. and termination

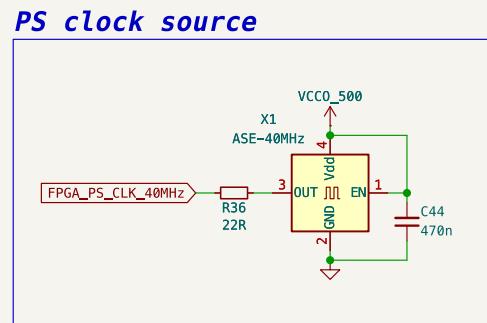
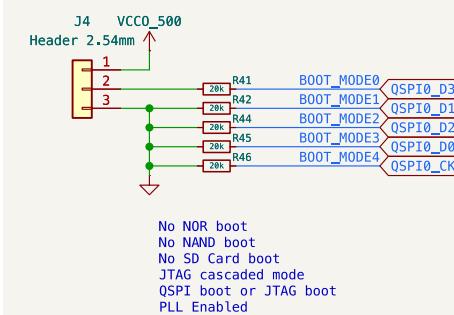
PS Configuration

Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]				
	V MODE[1]	V MODE[0]	BOOT_MODE[4]	BOOT_MODE[0]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[3]				
Boot Devices											
JTAG Boot Mode; cascaded is most common ⁽¹⁾				0	0	0					
NOR Boot ⁽³⁾				0	0	1					
NAND				0	1	0					
Quad-SPI ⁽³⁾				1	0	0					
SD Card				1	1	0					
Mode for all 3 PLLs											
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.							
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.							
MIO Bank Voltage⁽⁴⁾											
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15. Voltage Bank 1 includes MIO pins 16 thru 53.								
2.5 V, 3.3 V	0	0									
1.8 V	1	1									

Notes:

1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.



Sheet: /PS Configuration/
File: ps_config.kicad_sch
Title: FPGA Zynq7000 Dev Board
Size: A4 | Date: 2025-07-10
KiCad E,D,A. 9.0.3 | Rev: A
Id: 17/17

A

A

B

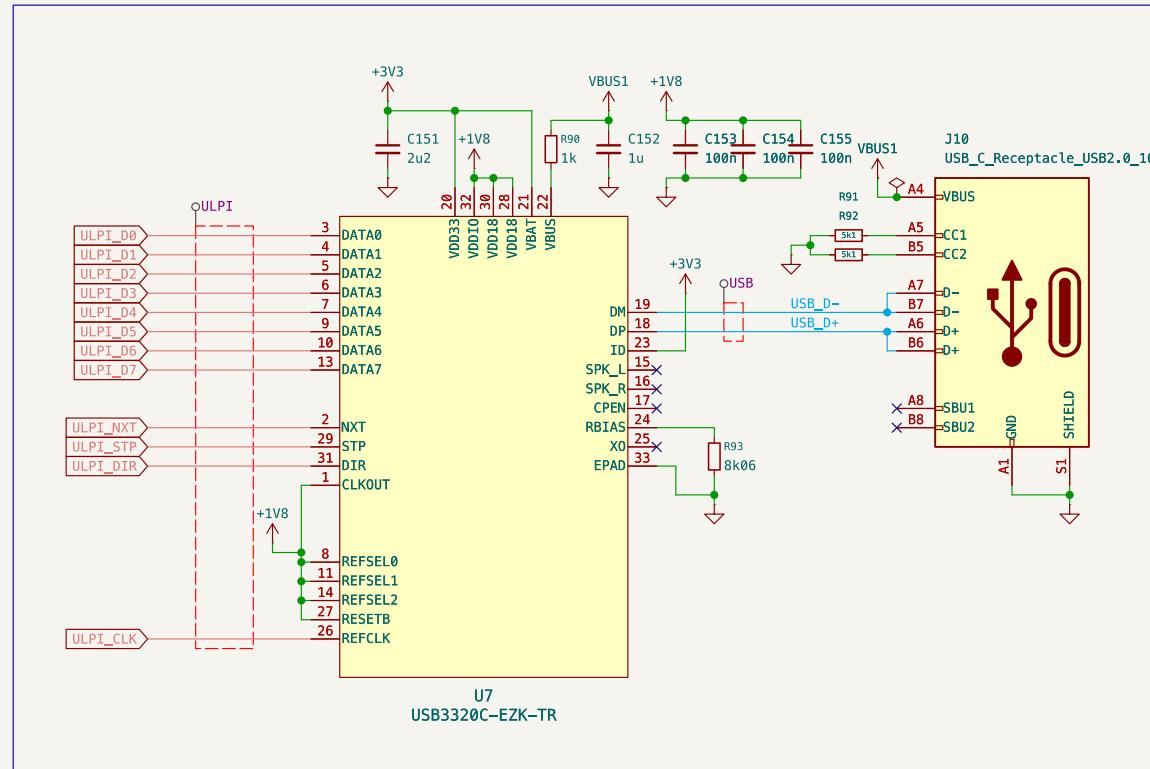
B

C

C

D

D

USB PHY

Sheet: /USB HS PHY/
File: ps_usb.kicad_sch

Title: FPGA Zynq7000 Dev Board

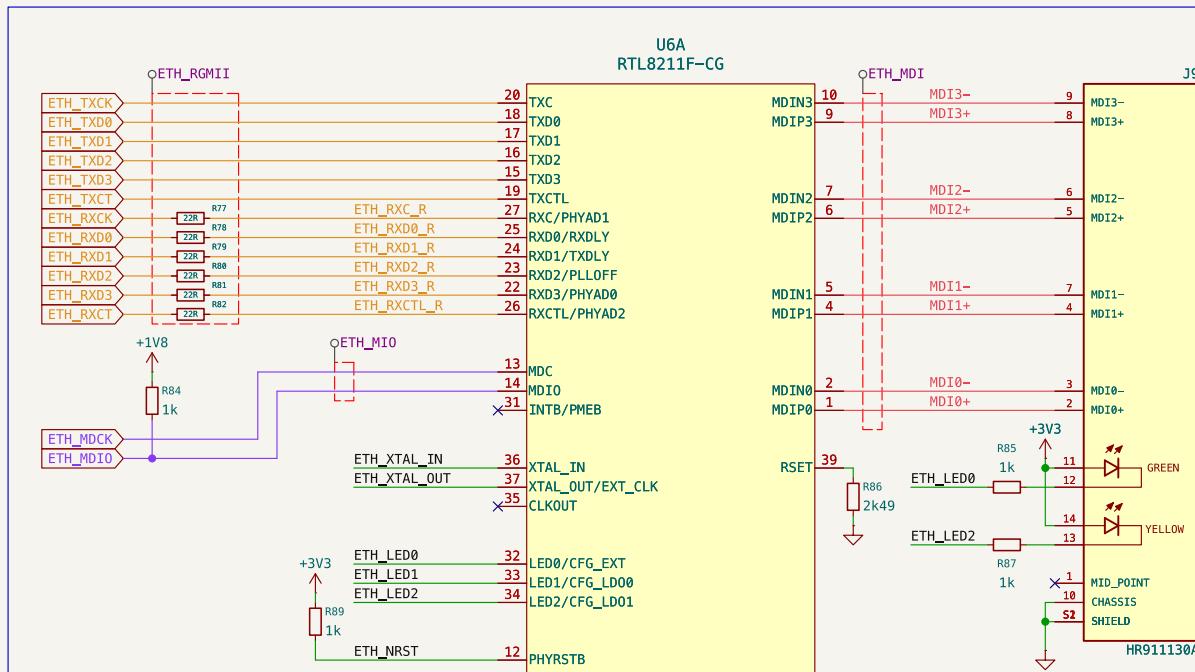
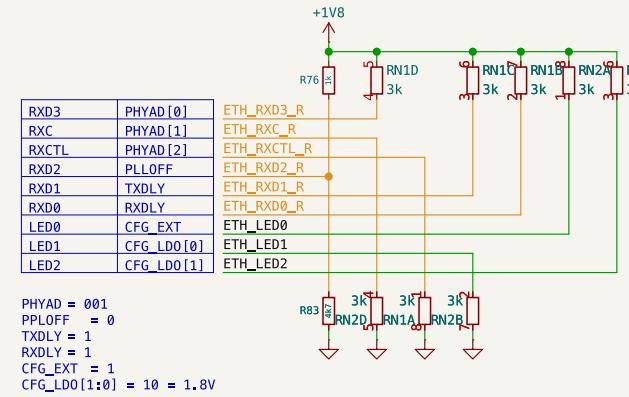
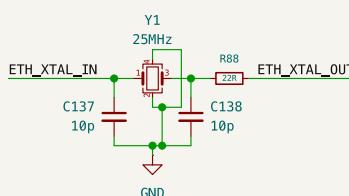
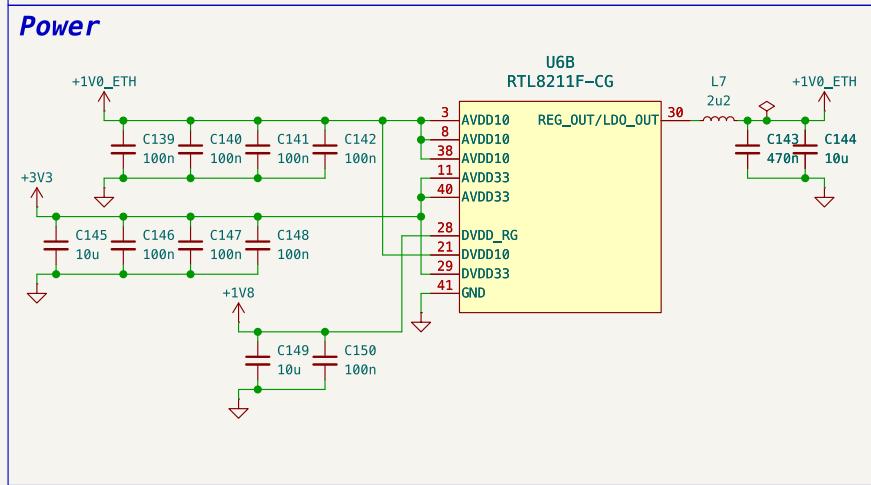
Size: A4 | Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 13/17

1 2 3 4 5 6

Ethernet PHY**PHY Configuration****Crystal****Power**

Sheet: /Gigabit Ethernet PHY/
File: ps_eth.kicad_sch

Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 12/17

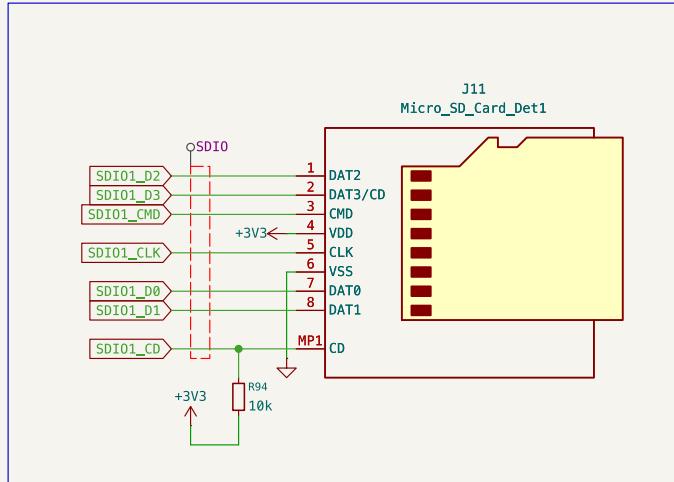
1 2 3 4 5 6

1 2 3 4 5 6

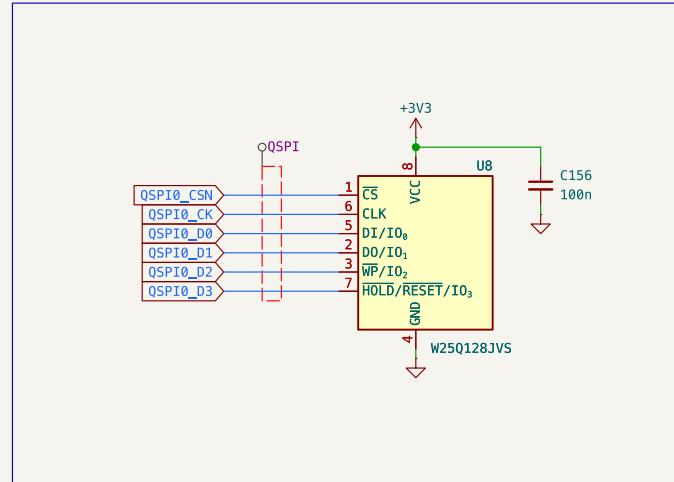
A

A

SD Card



QSPI Flash



B

B

C

C

D

D

Sheet: /SD Card + QSPI Flash/
File: ps_sd_qspi.kicad_sch

Title: FPGA Zynq7000 Dev Board

Size: A4 Date: 2025-07-10

KiCad E,D,A. 9.0.3

Rev: A

Id: 14/17

1 2 3 4 5 6