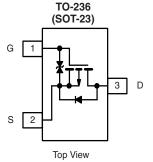




# P-Channel 60 V (D-S) MOSFET

PRODUCT	PRODUCT SUMMARY			
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	V <sub>GS(th)</sub> (V)	I <sub>D</sub> (mA)	
- 60	6 at V <sub>GS</sub> = - 10 V	- 1 to - 3	- 185	



Marking Code: 6Kwll

6K = Part Number Code for TP0610K w = Week Code

II = Lot Traceability

Ordering Information: TP0610K-T1-E3 (Lead (Pb)-free)

TP0610K-T1-GE3 (Lead (Pb)-free and Halogen-free)

### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- High-Side Switching
- Low On-Resistance: 6 Ω
- Low Threshold: 2 V (typ.)
- Fast Swtiching Speed: 20 ns (typ.)
- Low Input Capacitance: 20 pF (typ.)
- 2000 V ESD Protection
- Compliant to RoHS Directive 2002/95/EC

#### **APPLICATIONS**

- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- · Battery Operated Systems
- Power Supply Converter Circuits
- · Solid-State Relays

#### **BENEFITS**

- · Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- · Easily Driven without Buffer

<b>ABSOLUTE MAXIMUM RATINGS</b> T <sub>A</sub> = 25 °C, unless otherwise noted					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	- 60	.,,	
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
0 11	T <sub>A</sub> = 25 °C	I <sub>D</sub>	- 185	mA	
Continuous Drain Current <sup>a</sup>	T <sub>A</sub> = 100 °C		- 115		
Pulsed Drain Current <sup>b</sup>	·	I <sub>DM</sub>	- 800		
Developed to the stand	T <sub>A</sub> = 25 °C	P <sub>D</sub>	350	mW	
Power Dissipation <sup>a</sup>	T <sub>A</sub> = 100 °C	r <sub>D</sub>	140		
Maximum Junction-to-Ambient <sup>a</sup>	<u>.                                      </u>	R <sub>thJA</sub>	350	°C/W	
Operating Junction and Storage Temperature Range		T <sub>J,</sub> T <sub>stg</sub>	- 55 to 150	°C	

#### Notes

- a. Surface mounted on FR4 board.
- b. Pulse width limited by maximum junction temperature.

FREE

# **TP0610K**

# Vishay Siliconix



<b>SPECIFICATIONS</b> T <sub>A</sub> = 25	°C, unless oth	erwise noted					
			Limits				
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_{D} = -10 \mu\text{A}$	- 60			V	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1		- 3	] v	
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 10	μΑ	
Gate-Body Leakage		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}$			± 200		
Gale-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 10 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			± 500		
		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 100	nA	
7 0		V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V			- 25		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 60 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			- 250		
On-State Drain Current <sup>a</sup>	,	V <sub>GS</sub> = - 10 V, V <sub>DS</sub> = - 4.5 V	- 50			4	
	I <sub>D(on)</sub>	V <sub>GS</sub> = - 10 V, V <sub>DS</sub> = - 10 V	- 600			mA	
Drain-Source On-Resistance <sup>a</sup>		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 25 mA			10		
	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 500 mA			6	Ω	
		V <sub>GS</sub> = - 10 V, I <sub>D</sub> = - 500 mA, T <sub>J</sub> =125 °C			9	mA Ω mS V	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 100 mA	80			mS	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 200 mA, V <sub>GS</sub> = 0 V			- 1.4	V	
Dynamic	<u>.</u>						
Total Gate Charge	Qg			1.7			
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -30 \text{ V}, V_{GS} = -15 \text{ V}$ $I_{D} \cong -500 \text{ mA}$		0.26		nC	
Gate-Drain Charge	Q <sub>gd</sub>	1D = 000 m/r		0.46			
Input Capacitance	C <sub>iss</sub>			23		pF	
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -25 \text{ V}, V_{GS} = 0 \text{ V}$ f = 1  MHz		10			
Reverse Transfer Capacitance	C <sub>rss</sub>	1 - 1 1411.12		5			
Switching <sup>b</sup>							
Turn-On Time	t <sub>d(on)</sub>	$V_{DD} = -25 \text{ V}, R_{L} = 150 \Omega$		20			
Turn-Off Time	t <sub>d(off)</sub>	$I_D \cong$ - 200 mA, $V_{GEN} =$ - 10 V, $R_g =$ 10 $\Omega$		35		ns	

#### Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test: PW  $\leq$  300  $\mu s$  duty cycle  $\leq$  2 %.

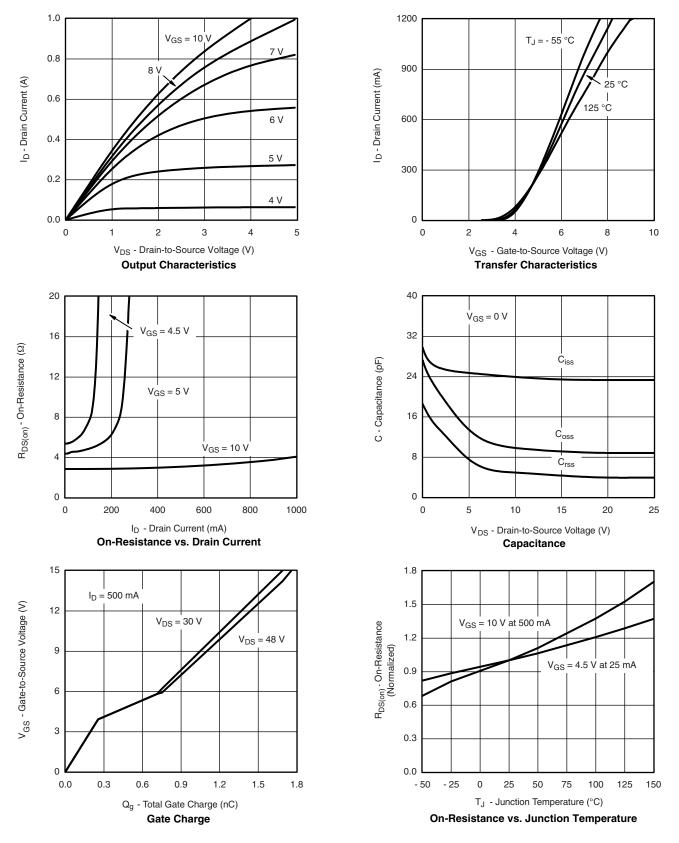
b. Switching time is essentially independent of operating temperature.







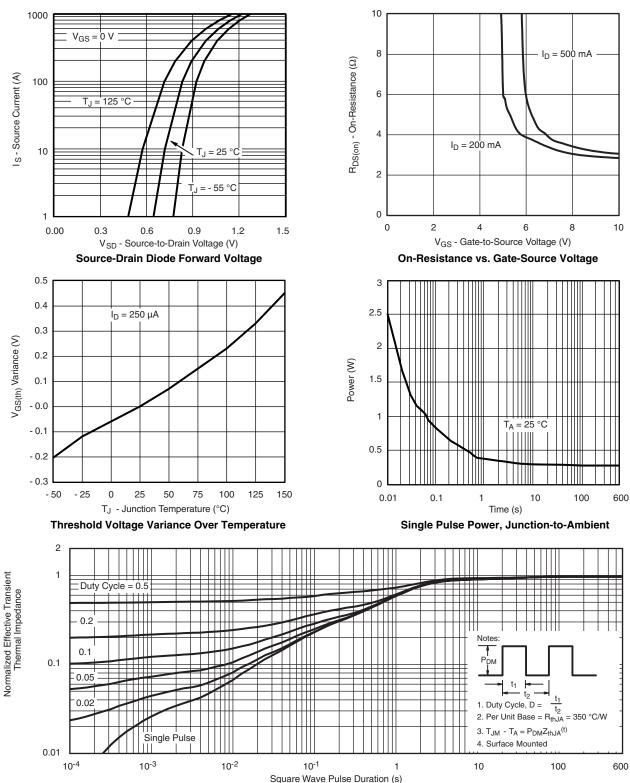
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



# Vishay Siliconix



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?71411">www.vishay.com/ppg?71411</a>.

Normalized Thermal Transient Impedance, Junction-to-Ambient



### SOT-23 (TO-236): 3-LEAD







Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
Α	0.89	1.12	0.035	0.044
A <sub>1</sub>	0.01	0.10	0.0004	0.004
A <sub>2</sub>	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
С	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E <sub>1</sub>	1.20	1.40	0.047	0.055
е	0.95 BSC		0.0374 Ref	
e <sub>1</sub>	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L <sub>1</sub>	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

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# **Mounting LITTLE FOOT® SOT-23 Power MOSFETs**

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint. In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the

ambient air. This pattern uses all the available area underneath the body for this purpose.



FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, "thermal" connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

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26-Nov-03



### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



### **Legal Disclaimer Notice**

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

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