The Basic Circuits for bq77910A Stack Design

Steven Yao BMS-Notebook

ABSTRACT

This application note describes the methodology and circuits for stacking two bq77910As. When two bq77910As are stacked, they work on different potentials. The control signals from two bq77910A parts based on different potentials are combined (ANDed) to control the charge and discharge MOSFETs on the main power path. The level-shift circuit, AND circuit for charge, and discharge control signals are shown and described in this document.

Contents

List of Figures

1 Introduction

The bq77910A is a complete stand-alone battery protection and cell-balancing device for Li-ion/Polymer/Phosphate Battery packs. The overall amount of cell numbers it supports ranges from 4 to 10 for a single device, but for many applications, like E Motor or high-cell-count power tools, the cell number in series can be greater than 10. To support such applications, the bq77910A is stacked up with level-shifting circuits, AND circuits for DSG and CHG signals to facilitate applications with more than 10 cells.

2 bq77910A Stacking Basics

The bq77910A must work on different potential levels if it is to be stacked. In a 12s application, 6 cells are connected to the bottom bq77910A and 6 cells are connected to top bq77910A. The DSG and CHG signals from both the top and bottom devices are combined to control the CHG and DSG MOSFETs in the main power path. The potential of DSG and CHG of the upper device are different from those of the bottom device. Typically, the potentials of DSG and CHG signals are about 11 V to 12 V to its own reference voltage (the potential of the Vss pin). Assuming that the voltage of each cell is averaged to 3.8 V, then with reference to the BAT– point of overall cell stack, the voltage of the DSG and CHG pins of the top devices are about 33.8 V to 34.8 V in normal state and 22.8 V in fault state like UVP, so the potential level of the DSG and CHG signals need to be shifted. Figure 1 is a typical level-shifting circuit for DSG.

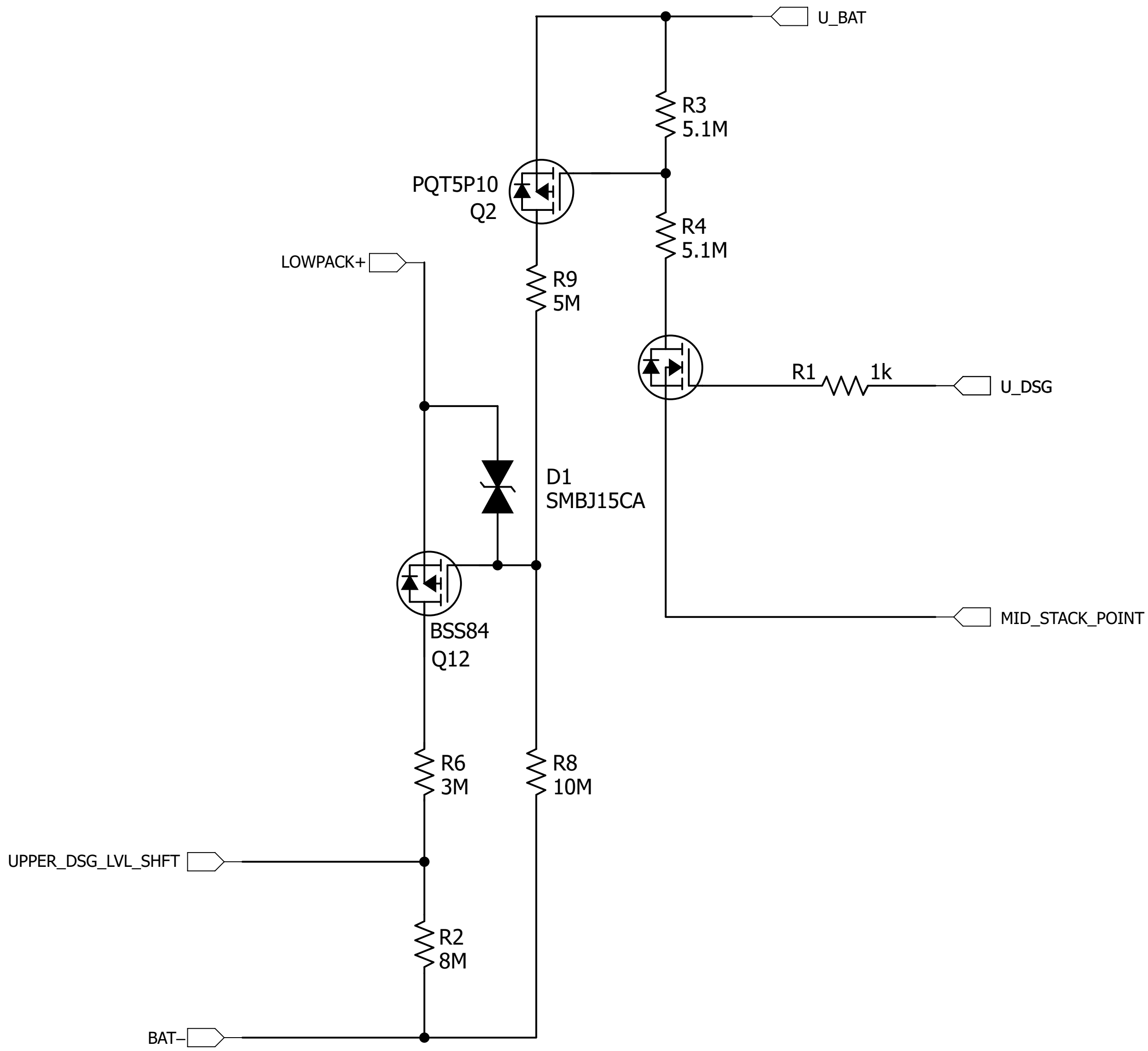

Figure 1. Typical Level-Shifting Circuit for DSG

In Figure 1, U_BAT is the BAT pin of the upper bq77910A, U_DSG is the signal from the DSG pin of the upper device. MID_STACK_POINT is the middle reference point of the cell stack, in a 12s cell stack, it is the voltage of the top of the 6th cell, counted from the bottom up. It is used as a reference point for the top bq77910A device. BAT– is the reference point of the bottom bq77910A, or the point at another side of the current sense resistor. The signal UPPER_DSG_LVL_SHFT is combined (ANDed) with the DSG signal from the bottom bq77910A.

The AND circuit of the DSG signal of the bottom bq77910A and the level-shifted DSG signal from the top device can be implemented as shown in Figure 2.

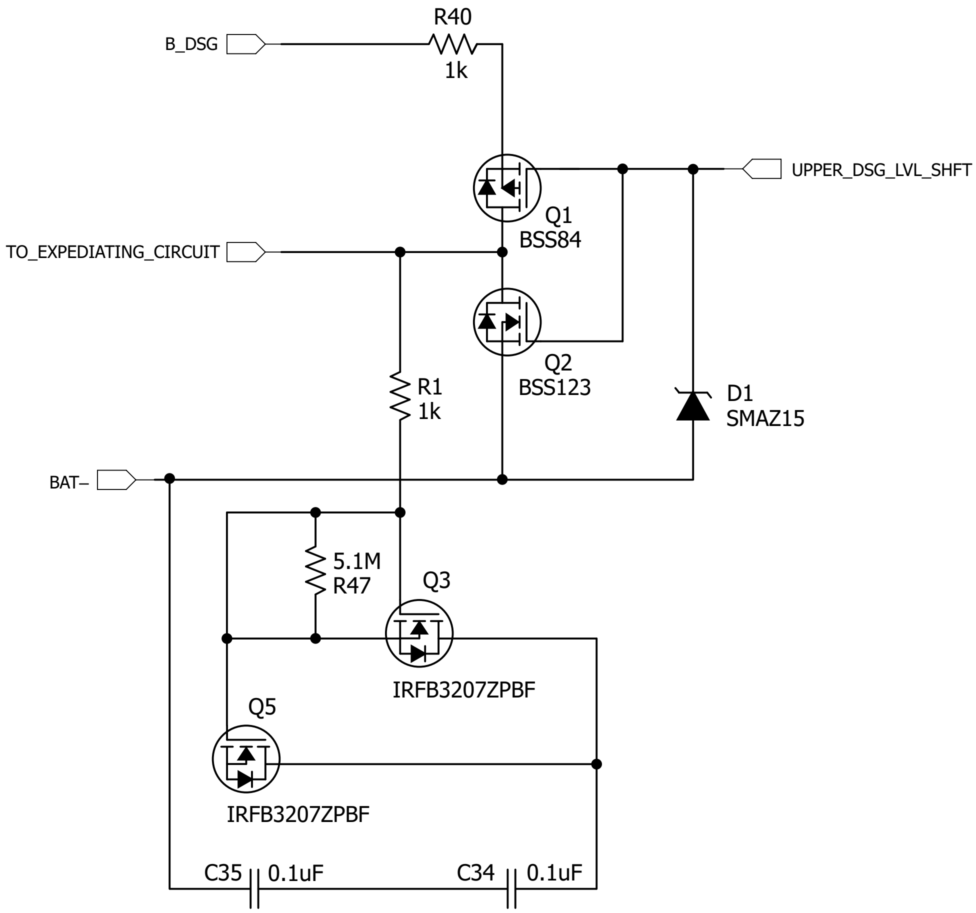

Figure 2. Implementation of the AND Circuit

In Figure 2, B_DSG is the DSG signal from the bottom bq77910A, UPPER_DSG_LVL_SHFT is the level-shifted DSG signal from the upper bq77910A, BAT– is the reference point of the bottom bq77910A or the point at another side of the current sense resistor.

3 Working Principle of the Circuits

3.1 The Working Process of Level-Shifting Circuit

The top bq77910A mainly provides voltage-based protection for the cells connected to its inputs. It is in charge of the fault conditions like over-voltage protection (OVP), under-voltage protection (UVP), and also temperature-based protection. In a normal state, the DSG signal is at about 12 V. While in fault condition, like UVP, it will be at about 0 V. In Figure 1, when U_DSG is low, Q1 is off, then the voltage at the Q2 gate is pulled up to U_BAT, Q2 is turned off, and the Q12 gate is pulled low. Q12 then turns on. The signal UPPER_DSG_LVL_SHFT is high. It is about 3/8 of the voltage on LOWPACK+. In the normal state condition, when U_DSG is high, the signal UPPER_DSG_LVL_SHFT is low.

3.2 The Working Process of the AND Circuit

In Figure 2, the B_DSG signal is from the bottom bq77910A. The UPPER_DSG_LVL_SHFT is the signal derived from the upper bq77910A. The signal, TO_EXPEDIATING_CIRCUIT, drives the gate of discharge MOSFETs, Q3 and Q5 via R1, in the normal state, when both DSG pins from the top and bottom bq77910A are high. The B_DSG is high, and the UPPER_DSG_LVL_SHFT is low. Q1 is on and Q2 is off. The drains of Q1 and Q2 are high, the gates of the Q3 and Q5 are high. When the bottom bq77910A detects a UVP fault, the B_DSG is low, the output of Q1 and Q2 also goes to low. When the top bq77910A is in UVP state, the UPPER_DSG_LVL_SHFT is high, Q1 is off, Q2 is on. This causes the output of Q1 and Q2 to go low. According to the preceeding analysis, the circuit in Figure 2 actually works as an AND gate for the top and bottom bq77910A DSG signals.

4 Test Results

4.1 UVP Detected by Top bq77910A

Figure 3 is the oscilloscope plot of the following test conditions:

- UVP threshold = 2.6 V
- The 7th cell from bottom up is set to 2.4 V
- Delay time = 1 s

Figure 3. UVP in the Top bq77910A

In Figure 3, CELL7_TOP (red) is the top voltage of the 7th cell. The UPPER_910_DSG (blue) is the voltage of the DSG pin of the upper bq77910A. The FET_DSG (yellow) is the voltage on the gate of discharge MOSFET.

4.2 UVP Detected by the Bottom bq77910A

The test conditions represented here are the same as those in the Section 4.1 test. The 1st bottom cell is set to 2.4 V for this test. Figure 4 is the plot of the test.

Figure 4. UVP in the Bottom bq77910A

In Figure 4, BOTTOM_910_DSG (blue) is the DSG pin signal of the bottom bq77910A, CELL1_TOP (red) is the top voltage of the bottom cell. The FET_DSG (yellow) is the voltage of the gate of discharge MOSFET. Due to the low sample rate, the falling edge is distorted. Figure 5 captures the real falling edge using a smaller time grid.

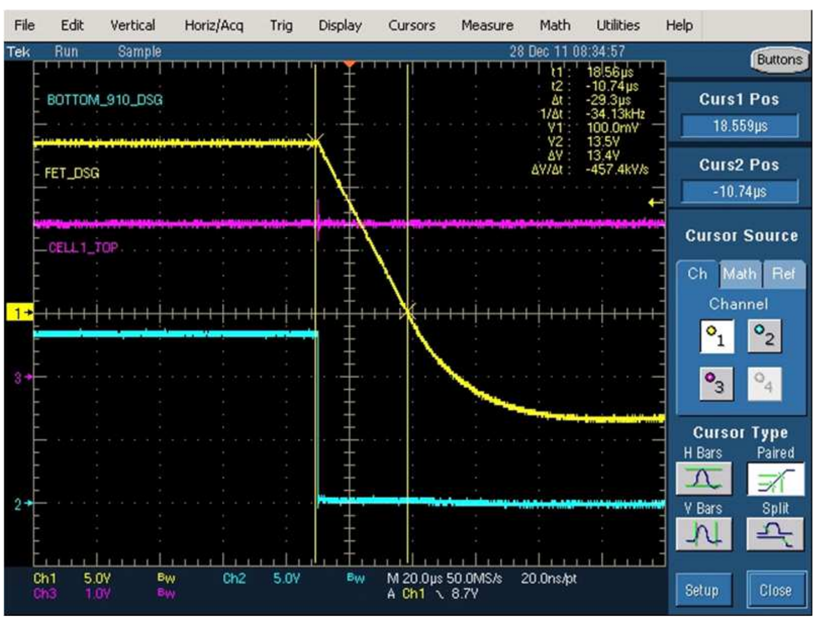

Figure 5. UVP in the Bottom bq77910A at a Smaller Time Grid

The meaning of the signal in Figure 5 is the same as those in Figure 4.

5 Schematics

This design uses high-impedance circuits. High-impedance circuits are subject to effects from leakage paths on the circuit board, electromagnetic field effects, and deviation of switching FET leakage from typical values approaching datasheet I_{DSS} limits. Designers must trade off circuit impedance with operating current in their design implementation to ensure a robust system in their environment. Thorough testing is necessary to be sure the system meets the system requirements with production variations.

Figure 6 shows the schematic for a bq77910A stack design, for additional information, contact your local TI office.

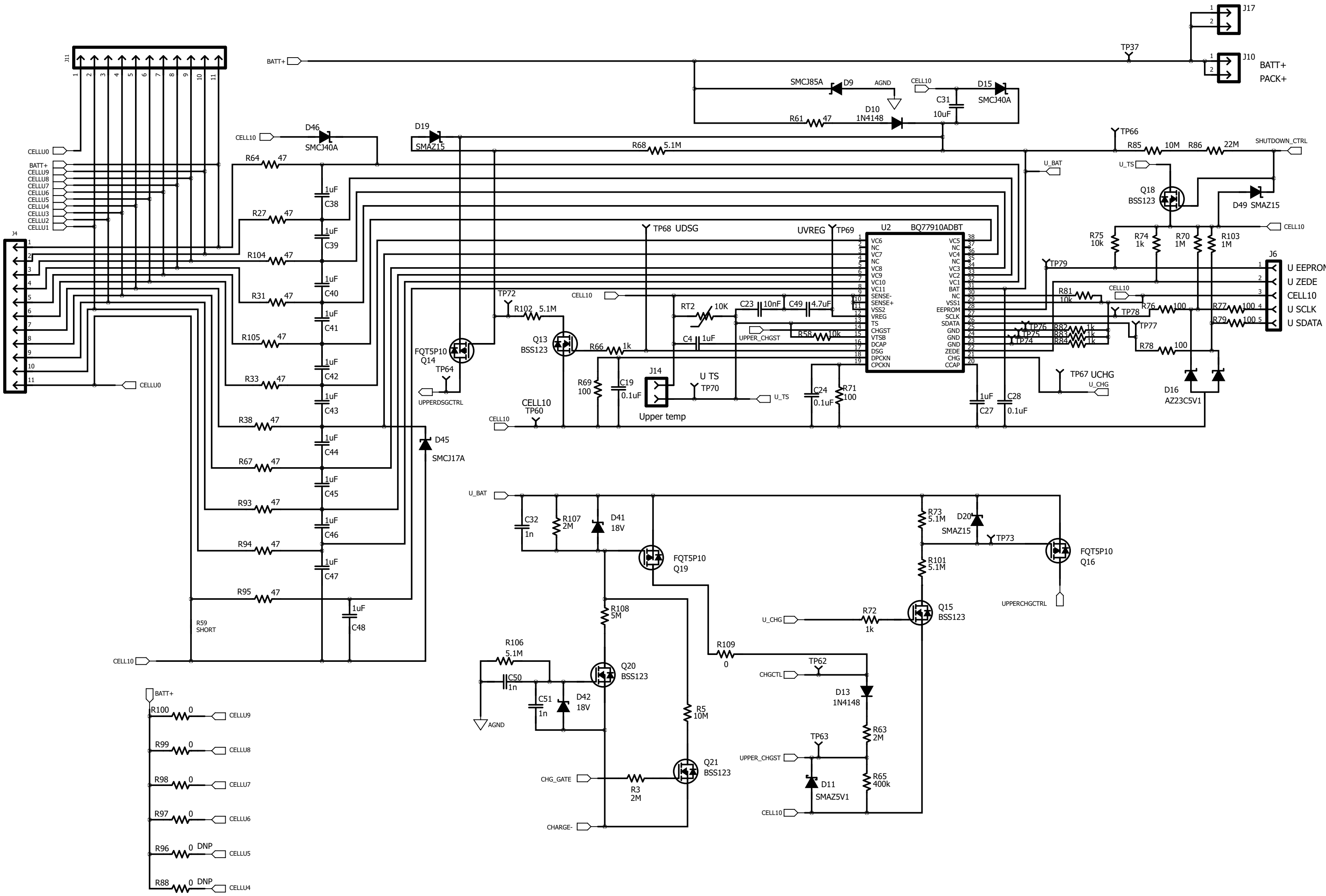

Figure 6. Top bq77910A Circuit

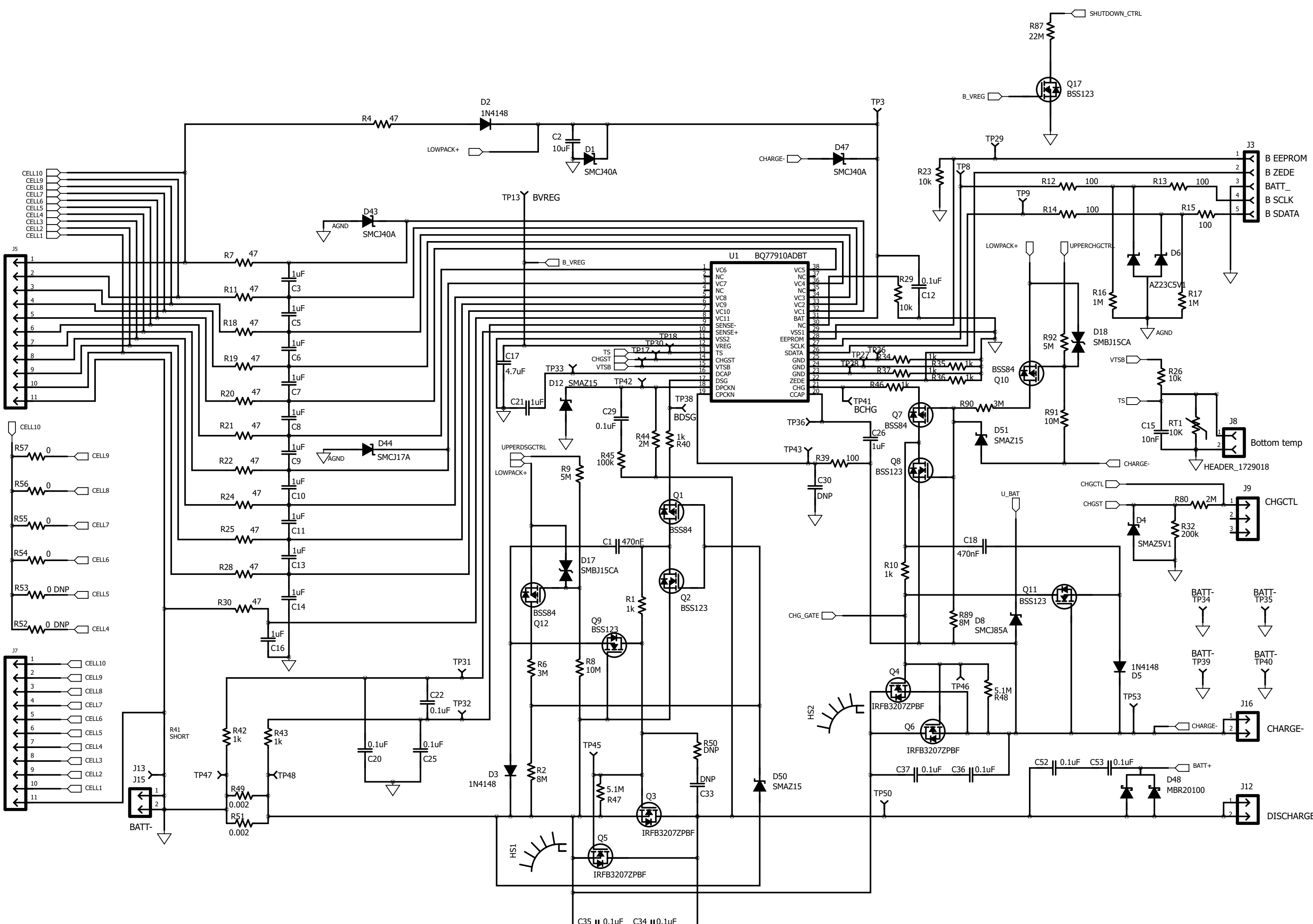

Figure 7. Bottom bq77910A Circuit

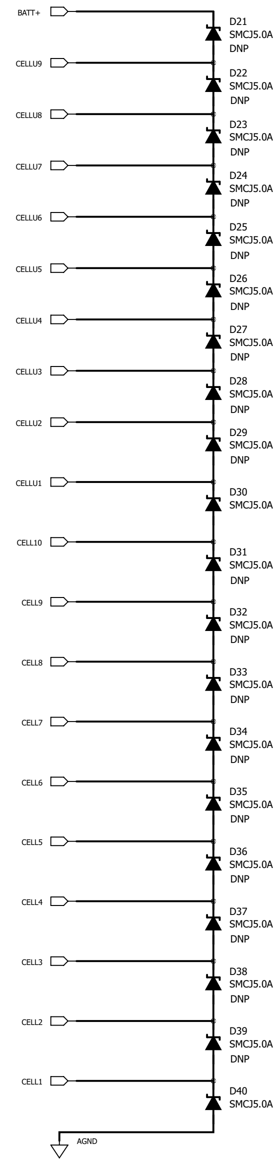

Figure 8. Input Protection Circuit