

The screenshot displays the 'Timing' tab in the Vivado IDE. The left-hand navigation pane shows a tree structure with 'Clock Summary (1)' selected. The main workspace area contains a table with the following data:

Name	Waveform	Period (ns)	Frequency (MHz)
axis_clk	{0.000 6.000}	12.000	83.333

Gener	Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock
Timer	↳ Path 1	0.586	10	11	129	ctrl_tap/ffen_r_reg/C	sm_tdata_r_reg[29]/D	11.309	8.452	2.857	12.0	axis_clk	axis_clk
Design	↳ Path 2	0.592	10	11	129	ctrl_tap/ffen_r_reg/C	sm_tdata_r_reg[31]/D	11.303	8.446	2.857	12.0	axis_clk	axis_clk
Clock	↳ Path 3	0.667	10	11	129	ctrl_tap/ffen_r_reg/C	sm_tdata_r_reg[30]/D	11.228	8.371	2.857	12.0	axis_clk	axis_clk
Metho	↳ Path 4	0.691	10	11	129	ctrl_tap/ffen_r_reg/C	sm_tdata_r_reg[28]/D	11.204	8.347	2.857	12.0	axis_clk	axis_clk
Check	↳ Path 5	0.703	9	10	129	ctrl_tap/ffen_r_reg/C	sm_tdata_r_reg[25]/D	11.192	8.335	2.857	12.0	axis_clk	axis_clk
Intra- Clock	↳ Path 6	0.706	9	10	129	ctrl_tap/ffen_r_reg/C	sm_tdata_r_reg[27]/D	11.186	8.329	2.857	12.0	axis_clk	axis_clk

The screenshot shows the Xilinx ISE Timing Summary window. The 'Timing' tab is selected, and the search criteria are 'Intra-Clock Paths - axis_clk - Pulse Width'. The table below lists the timing results:

Check Type	Corner	Lib Pin	Reference Pin	Required	Actual	Slack	Location	Pin
Low Pulse Width	Slow	FDSE/C	n/a	0.500	6.000	5.500		FSM_oneh...eg[0]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	6.000	5.500		FSM_oneh...eg[1]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	6.000	5.500		FSM_oneh...eg[2]/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	6.000	5.500		ap_start_sig_reg/C
Low Pulse Width	Slow	FDRE/C	n/a	0.500	6.000	5.500		arready_r_reg/C
High Pulse Width	Fast	FDSE/C	n/a	0.500	6.000	5.500		FSM_oneh...eg[0]/C

The 'Timing Summary - timing_1' window is also visible at the bottom of the screenshot.