1. Resource usage

```
27
28  1. Slice Logic
29  --------------
30
31  +-----------------------+------+-------+------------+-----------+-------+
32  |       Site Type       | Used | Fixed | Prohibited | Available | Util% |
33  +-----------------------+------+-------+------------+-----------+-------+
34  | Slice LUTs*           |  297 |     0 |          0 |     53200 |  0.56 |
35  |   LUT as Logic        |  297 |     0 |          0 |     53200 |  0.56 |
36  |   LUT as Memory       |    0 |     0 |          0 |     17400 |  0.00 |
37  | Slice Registers       |  200 |     0 |          0 |    106400 |  0.19 |
38  |   Register as Flip Flop|  200 |    0 |          0 |    106400 |  0.19 |
39  |   Register as Latch   |    0 |     0 |          0 |    106400 |  0.00 |
40  | F7 Muxes              |    0 |     0 |          0 |     26600 |  0.00 |
41  | F8 Muxes              |    0 |     0 |          0 |     13300 |  0.00 |
42  +-----------------------+------+-------+------------+-----------+-------+
43  * Warning! The Final LUT count, after physical optimizations and full implementation, i
```

```
------------------------------------------------------------------------------
Start RTL Component Statistics
------------------------------------------------------------------------------
Detailed RTL Component Info :
+---Adders :
         2 Input   12 Bit       Adders := 5
         2 Input    4 Bit       Adders := 2
+---Registers :
                   32 Bit    Registers := 3
                   12 Bit    Registers := 3
                    4 Bit    Registers := 3
                    1 Bit    Registers := 18
+---Multipliers :
                   32x32  Multipliers := 1
+---Muxes :
         2 Input   32 Bit        Muxes := 8
         3 Input   32 Bit        Muxes := 1
         2 Input   12 Bit        Muxes := 11
         2 Input    4 Bit        Muxes := 7
         2 Input    1 Bit        Muxes := 37
         3 Input    1 Bit        Muxes := 3
------------------------------------------------------------------------------
Finished RTL Component Statistics
------------------------------------------------------------------------------
```

因為使用很多 reg 來儲存，尤其是 12bits addr 的部分，所以可能 flip flop 使用比較多，是可以減少的。