	RF	PC_counter		Arith				Logical		comprator		Shifter		ALU_operation		Data Mem		prossesor							
	Reg Write	JALR	Branch	signal of add	signal of sub	signal select Arith_op(1)	signal select Arith_op(0)	signal select logical_op(1)	signal select logical_op(0)	Signal select SLT.SEQ.SLTU(1)	Signal select SLT.SEQ.SLTU(0)	Signal select shifter_op(1)	Signal select shifter_op(0)	ALU_operation(1)	ALU_operation(0)	MEM_Read	MEM_Write	Mux_Extender	Mux_RD_1(1)	Mux_RD_1(0)	Mux_RD_2	Mux_S2_Imm16(1)	Mux_S2_Irim16(0)	Mux_SA_RS2	ALU_crtl
SLL	1	0	0	0	0	*	*	*	*	*	*	0	0	1	0	0	0	*	0	0	0	*	*	1	0
SRL	1	0	0	0	0	*	*	*	*	*	*	0	1	1	0	0	0	*	0	0	0	*	*	1	0
SRA	1	0	0	0	0	*	*	*	*	*	*	1	0	1	0	0	0	*	0	0	0	*	*	1	0
ROR	1	0	0	0	0	*	*	*	*	*	*	1	1	1	0	0	0	*	0	0	0	*	*	1	0
ADD	1	0	0	1	0	0	0	*	*	*	*	*	*	0	0	0	0	*	0	0	0	0	0	*	0
SUB	1	0	0	0	1	0	1	*	*	*	*	*	*	0	0	0	0	*	0	0	0	0	0	*	0
SLT	1	0	0	0	0	*	*	*	*	0	0	*	*	1	1	0	0	*	0	0	0	0	0	*	0
SLTU	1	0	0	0	0	*	*	*	*	1	0	*	*	1	1	0	0	*	0	0	0	0	0	*	0
SEQ	1	0	0	0	0	*	*	*	*	0	1	*	*	1	1	0	0	*	0	0	0	0	0	*	0
XOR	1	0	0	0	0	*	*	1	1	*	*	*	*	0	1	0	0	*	0	0	0	0	0	*	0
OR	1	0	0	0	0	*	*	0	1	*	*	*	*	0	1	0	0	*	0	0	0	0	0	*	0
AND	1	0	0	0	0	*	*	0	0	*	*	*	*	0	1	0	0	*	0	0	0	0	0	*	0
NOR	1	0	0	0	0	*	*	1	0	*	*	*	*	0	1	0	0	*	0	0	0	0	0	*	0
MUL	1	0	0	0	0	1	0	*	*	*	*	*	*	0	0	0	0	*	0	0	0	0	0	*	0
MULU	1	0	0	0	0	1	1	*	*	*	*	*	*	0	0	0	0	*	0	0	0	0	0	*	0
SLLI	1	0	0	0	0	*	*	*	*	*	*	0	0	1	0	0	0	*	0	0	0	*	*	0	1
SRLI	1	0	0	0	0	*	*	*	*	*	*	0	1	1	0	0	0	*	0	0	0	*	*	0	1
SRAI	1	0	0	0	0	*	*	*	*	*	*	1	0	1	0	0	0	*	0	0	0	*	*	0	1
RORI	1	0	0	0	0	*	*	*	*	*	*	1	1	1	0	0	0	*	0	0	0	*	*	0	1
ADDI	1	0	0	1	0	0	0	*	*	*	*	*	*	0	0	0	0	0	0	0	0	0	1	*	1
SLTI	1	0	0	0	0	*	*	*	*	0	0	*	*	1	1	0	0	0	0	0	0	0	1	*	1
SLTIU	1	0	0	0	0	*	*	*	*	1	0	*	*	1	1	0	0	1	0	0	0	0	1	*	1
SEQI	1	0	0	0	0	*	*	*	*	0	1	*	*	1	1	0	0	0	0	0	0	0	1	*	1
XORI	1	0	0	0	0	*	*	1	1	*	*	*	*	0	1	0	0	1	0	0	0	0	1	*	1
ORI	1	0	0	0	0	*	*	0	1	*	*	*	*	0	1	0	0	1	0	0	0	0	1	*	1
ANDI	1	0	0	0	0	*	*	0	0	*	*	*	*	0	1	0	0	1	0	0	0	0	1	*	1
NORI	1	0	0	0	0	*	*	1	0	*	*	*	*	0	1	0	0	1	0	0	0	0	1	*	1
SET	1	0	0	0	0	*	*	*	*	*	*	*	*	*	*	0	0	0	1	0	0	*	*	*	1
SSET	1	0	0	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	1	1	0	*	*	*	1
JALR	1	1	0	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	*	*	1	*	*	*	1
LW	1	0	0	0	0	0	0	*	*	*	*	*	*	0	0	1	0	0	0	1	0	0	1	*	1
		0	0																						
SW	0	0	0	0	0	0	0	*	*	*	*	*	*	0	0	0	1	*	*	*	*	1	0	*	1
BEQ	0	0	1	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	*	*	*	0	0	*	1
BNQ	0	0	1	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	*	*	*	0	0	*	1
BLT	0	0	1	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	*	*	*	0	0	*	1
BGE	0	0	1	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	*	*	*	0	0	*	1
BLTU	0	0	1	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	*	*	*	0	0	*	1
BGEU	0	0	1	0	0	*	*	*	*	*	*	*	*	*	*	0	0	*	*	*	*	0	0	*	1