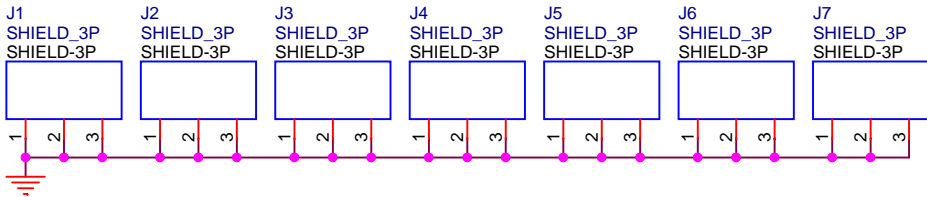
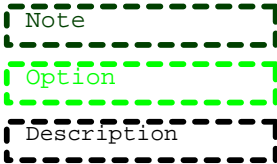


ROCKPro64_V2.1

CONTENT INDEXING

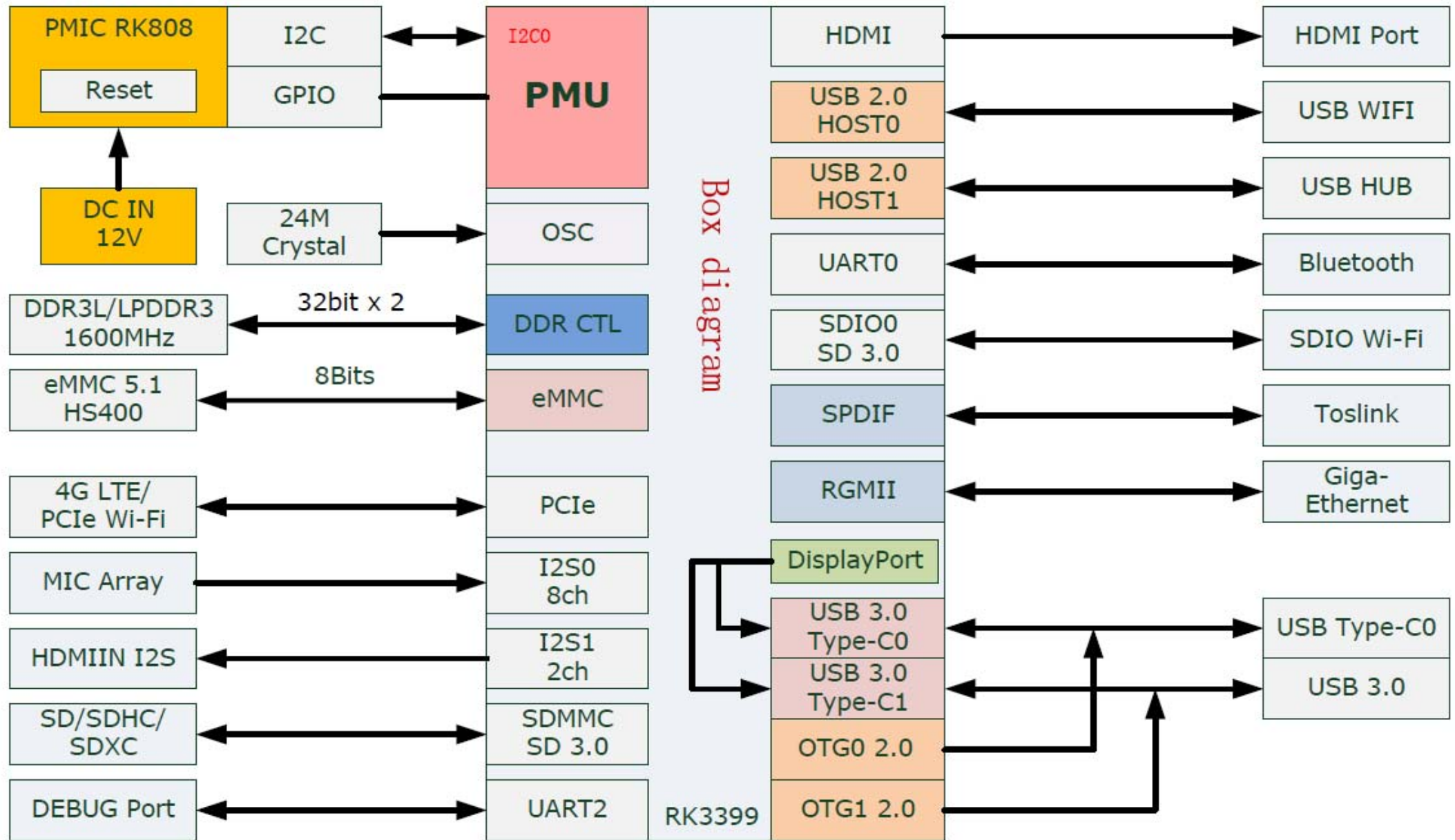
- 01.Index
- 02.Change List
- 03.Block Diagram
- 04.Power Tree
- 05.I2C Map
- 06.Power Domain Map
- 09.IR Receiver
- 10.RK3399 Power
- 11.RK3399 PMU Controler
- 12.RK3399 DDR Controler
- 13.RK3399 Flash&SDMMC Controler
- 14.RK3399 USB/USIC Controler
- 15.RK3399 SARADC/Key
- 16.RK3399 DVP Interface
- 17.RK3399 Display Interface
- 18.RK3399 GPIO
- 19.RK3399 PCIE
- 20.Power-DC IN
- 21.Power-PMIC RK808-D
- 25.USB OTG/HOST Port
- 26.USB Type-C Port
- 27.USB HUB
- 32.RAM-DDR3 4x16bit(option)
- 36.RAM-LPDDR3(178P)
- 40.Memory-eMMC
- 60.WIFI-USB(option)
- 61.WIFI/BT-AP6xxx(option)
- 63.WIFI/BTMIMO-AP6354
- 65.RJ45-1000M-RTL8211E
- 66.RJ45-100M-DP83848N(option)
- 67.RJ45-1000M-ZX2AA500(option)
- 74.MIC Array
- 81.TF Card
- 82.Digital Video Output
- 83.Digital Video Input
- 84.SPDIF Output
- 85.PCie NGFF/M.2
- 86.PCie x4 (option)
- 90.FAN(option)
- 91.eFUSE(option)

Note:
1: If the Value or option of the component properties is DNP, indicating do not mounted

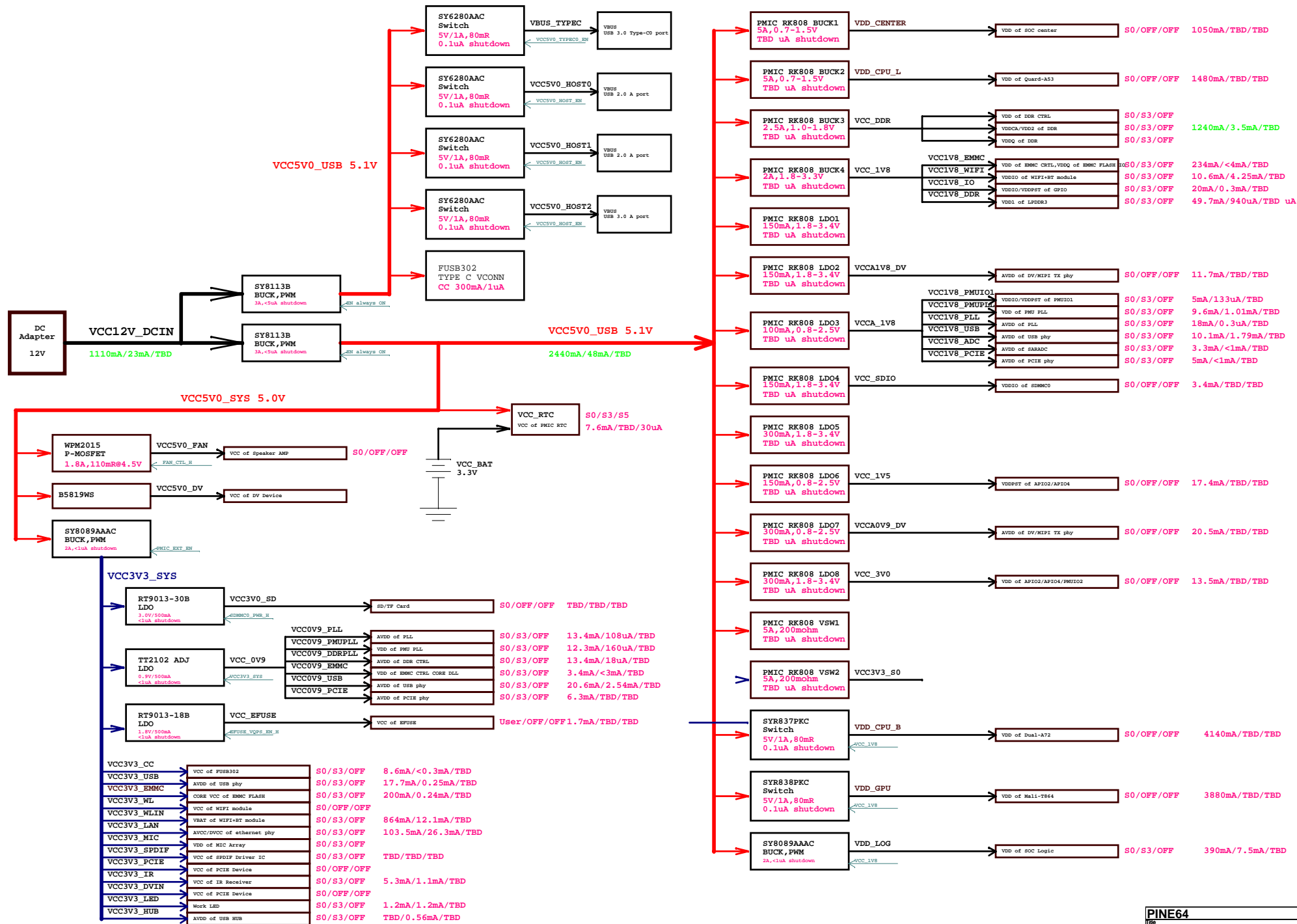


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Block Diagram



RK3399 POWER DIAGRAM



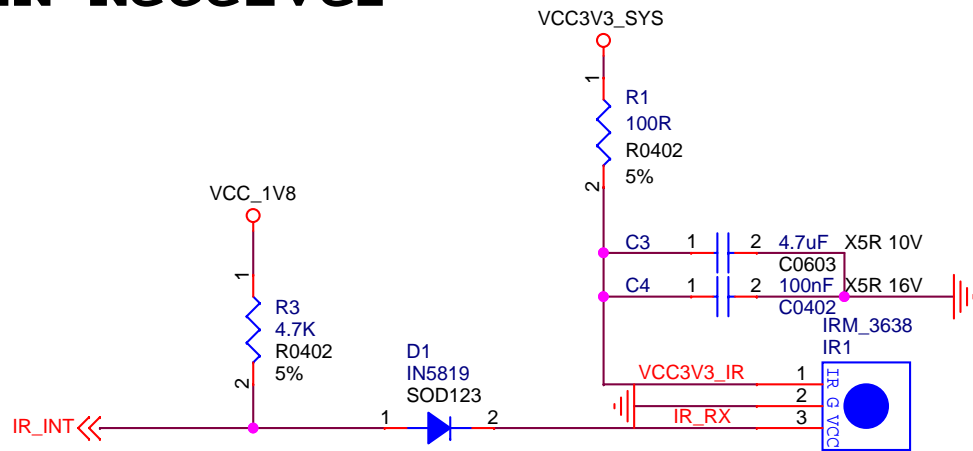
RK3399 Power Domain Map

Part Port	Domain	Pin name in datasheet	I/O type	Power supply	Power source
Part C	PMUI01	pmui01_gpio0ab	1.8V only	VCC1V8_PMU	RK808 VLD03
Part E	PMUI02	pmu1830_gpio1abcd	1.8V(Default) 3.0V	VCC1V8_PMU	RK808 VLD03
Part I	API01	gmac_gpio3abc	3.3V only	VCC1V8_IO VCC3V3_IO	RK808 Buck4 RK808 VSW2
Part L	API02	bt656_gpio2ab	1.8V(Default) 3.0V	VCC1V8_DVP	RK808 VLD01
Part G	API03	wifi/bt_gpio2cd	1.8V only	VCC1V8_WIFI	RK808 Buck4
Part K	API04	gpio1830_gpio4cd	1.8V 3.0V(Default)	VCC_1V5 VCC3V0_IO	RK808 VLD06 RK808 VLD08
Part J	API05	audio_gpio3d_gpio4a	1.8V(Default) 3.0V	VCCA1V8_CODEC	RK808 VLD07
Part F	SDMMC0	sdmmc_gpio4b	1.8V 3.0V(Default)	VCC_SDIO	RK808 VLD04

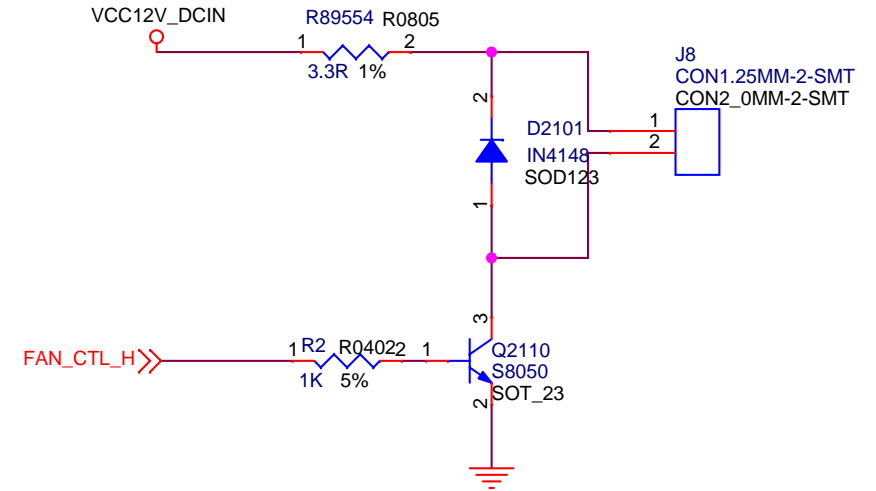
I2C MAP

Port	Pin name	Domain	Bus name	Pull-up voltage	Slave Device	Slave Addr (MS 7Bits)	Note	Slave Bus Capability
I2C0	GPIO1_B7/SPI3_RXD/I2C0_SDA GPIO1_C0/SPI3_TXD/I2C0_SCL	PMUIO2	I2C_SDA_PMIC I2C_SCL_PMIC	VCC_1V8	Rockchip RK808	0x1b	PMIC	100kHz,400KHz
					SYR837PKC	0x40	DC-DC BUCK	100kHz,400KHz,3.4MHz
					SYR838PKC	0x41	DC-DC BUCK	100kHz,400KHz,3.4MHz
I2C1	GPIO4_A1/I2C1_SDA GPIO4_A2/I2C1_SCL	APIO5	I2C_SDA_VIDEO I2C_SCL_VIDEO	VCC_1V8	TC358749XBG		DV Transmit	
I2C2	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	APIO2	RESERVE					
I2C3	GPIO4_C0/I2C3_SDA/UART2B_RX GPIO4_C1/I2C3_SCL/UART2B_TX	APIO4	I2C_SDA_DV I2C_SCL_DV	VCC_3V0				
I2C4	GPIO1_B3/I2C4_SDA GPIO1_B4/I2C4_SCL	PMUIO2	I2C_SDA_MEMS I2C_SCL_MEMS	VCC_1V8	Fairchild FUSB302B	0x44,0x46	USB-TypeC Mux	100kHz,400KHz,1MHz
I2C5	GPIO3_B2/MAC_RXER/I2C5_SDA GPIO3_B3/MAC_CLK/I2C5_SCL	APIO1	Other pin function					
I2C6	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	APIO2	RESERVE					
I2C7	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	APIO2	RESERVE					

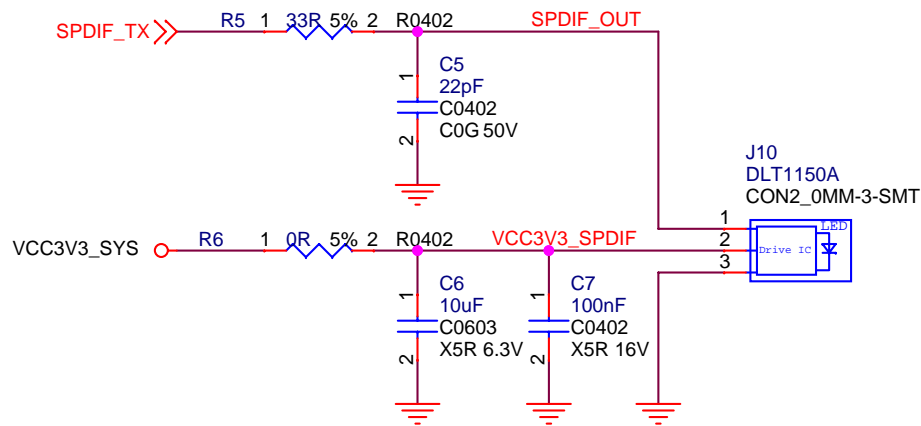
IR Receiver



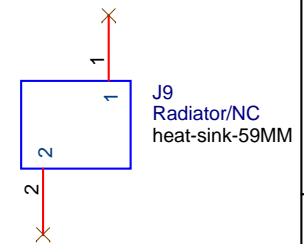
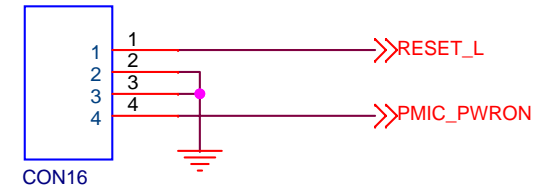
HEATSINK/FAN (option)



SPDIF OUT

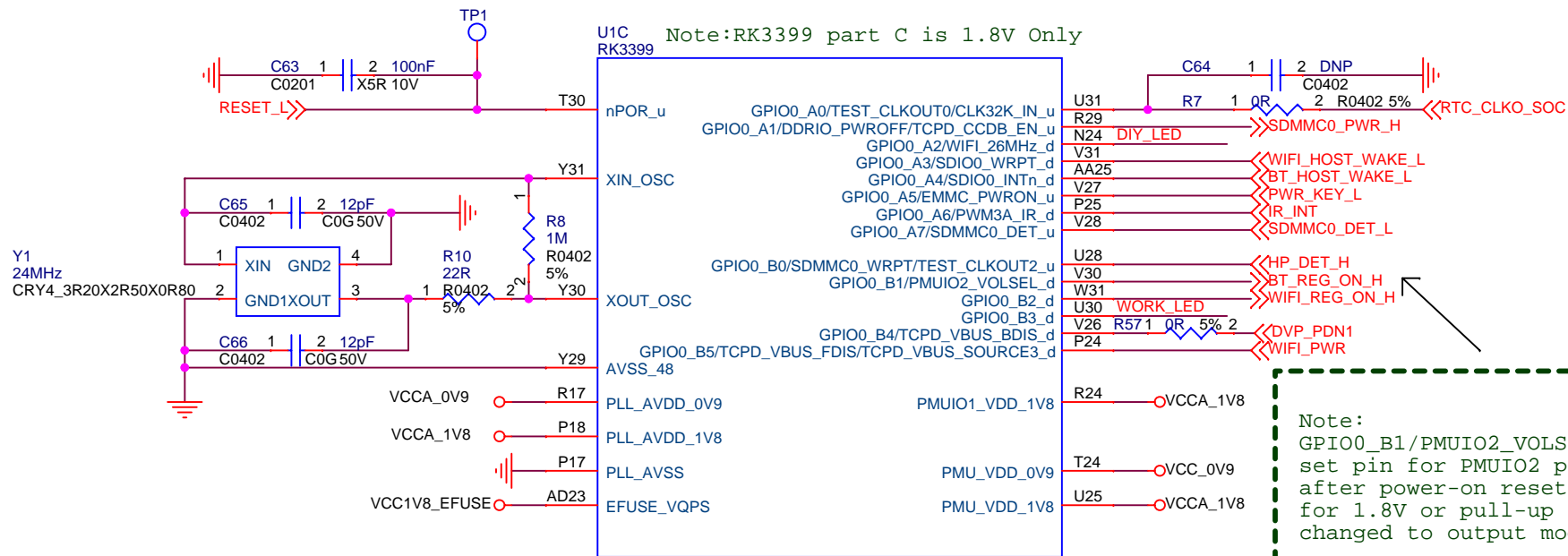


预留复位，开机键扩展连接座
XH_2.5mm/NC



PINE64

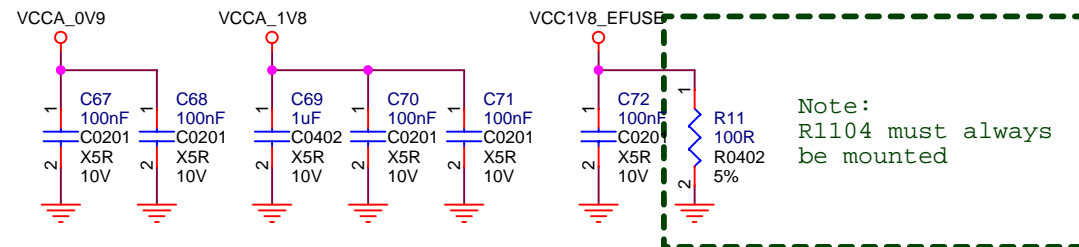
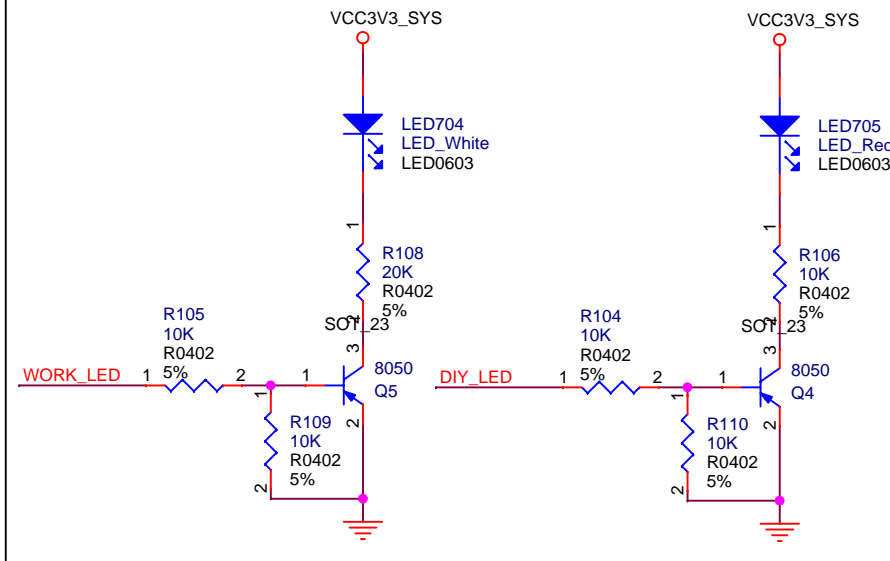
Title		
RockPro64_RK3399		
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Cristal selection requirements:

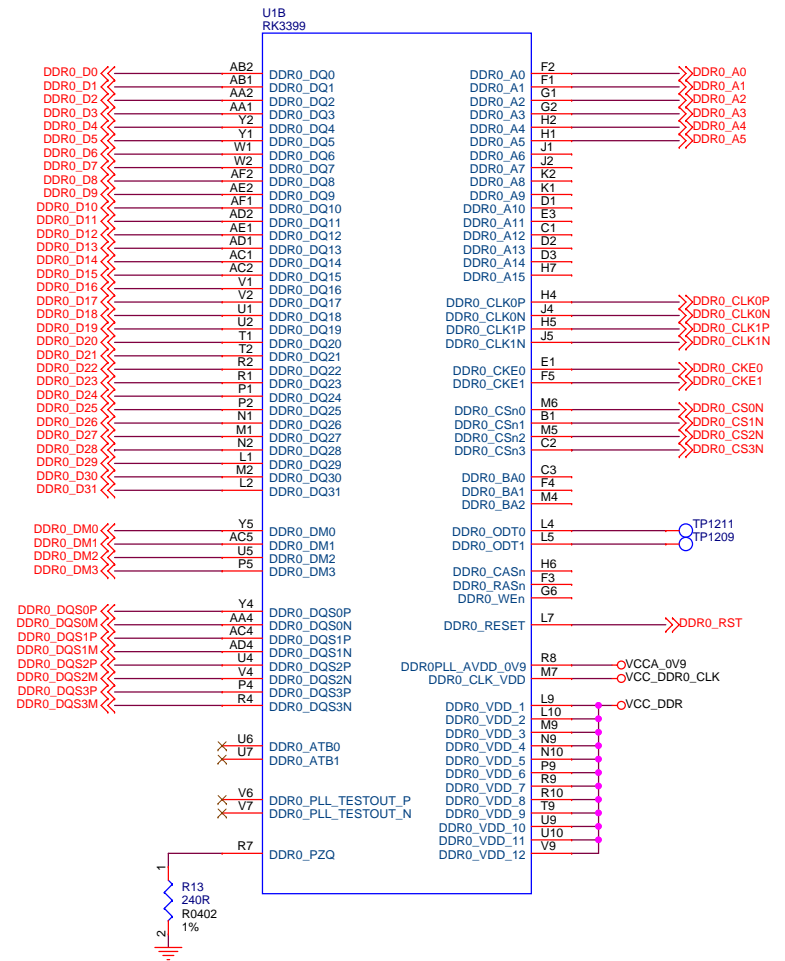
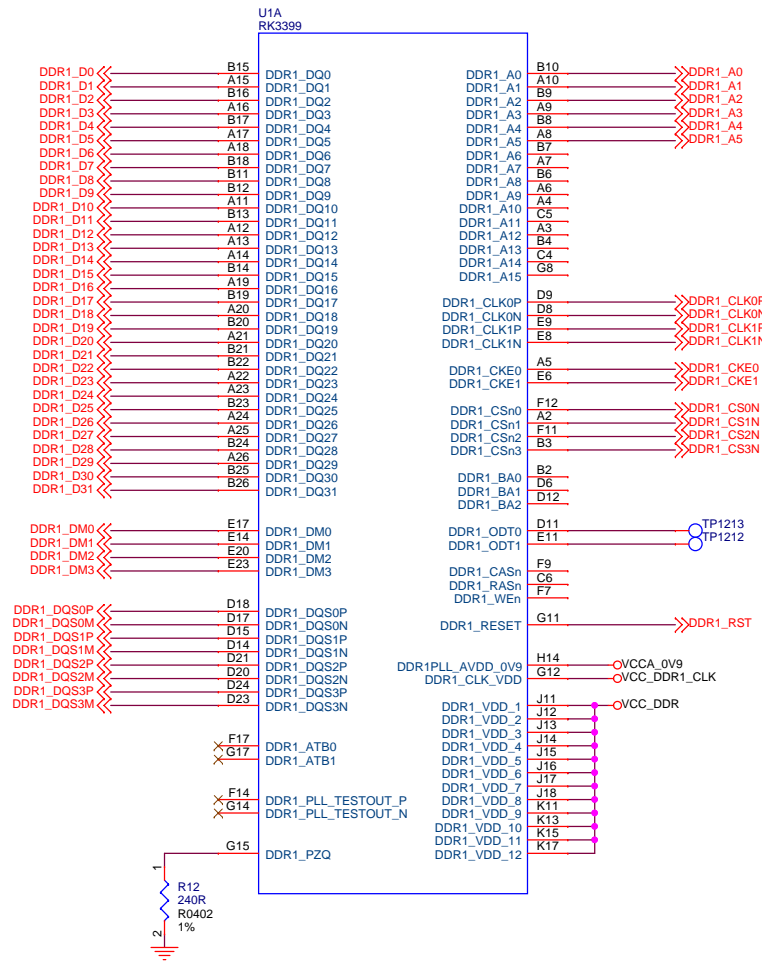
- 1.Nominal Frequency is 24MHz;
- 2.Frequency tolerance is +/-20ppm;
- 3.Operating Temperature range is -20~70°C;
- 4.Equivalent resistance < 60ohm;

LED



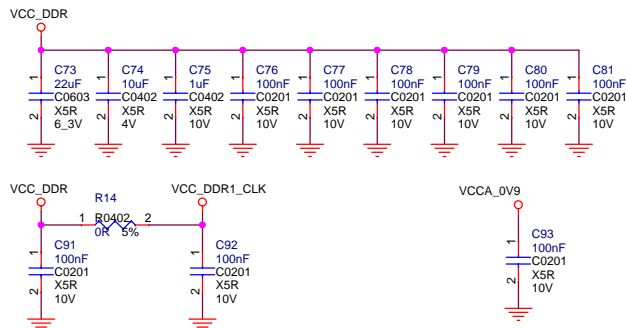
PINE64

Title		
RockPro64_RK3399		
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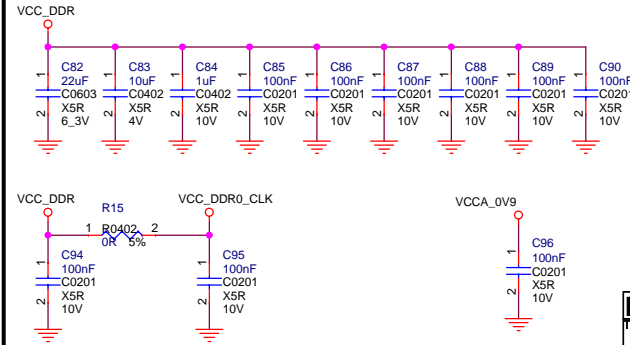
DDR FILTER

Note:R1202 cannot be deleted



DDR FILTER

Note:R1203 cannot be deleted



PINE64

RockPro64_RK3399

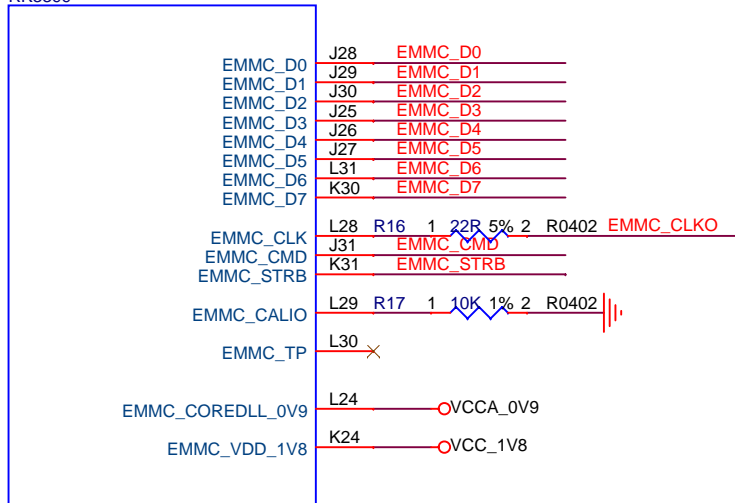
Size A3 Document Number RK3399 DDR Controller

Date: Tuesday, MAR 6, 2018

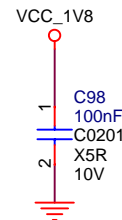
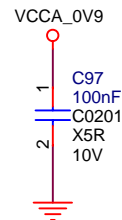
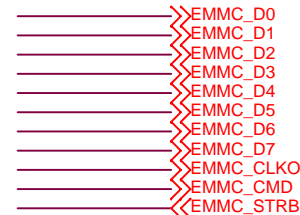
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Rev V2.0

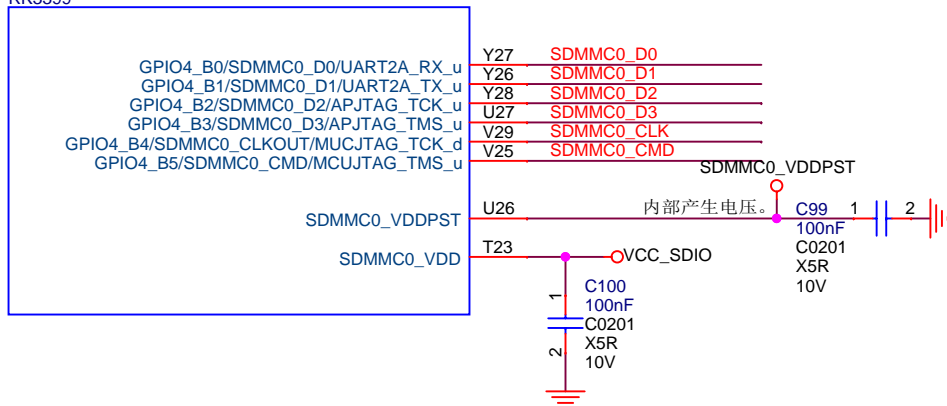
U1H
RK3399



EMMC design rule:
1.Data[0:7]、cmd、strobe走线做为一组，
并行走线并整组包地，组内等长要求为 $\pm 100\text{mil}$;
2.Clk需要单独走线并包地处理，与data间的
延时小于 20ps ;
3.Max trace length < 3.93 inches;
4.Trace impedance $50\text{ohm} \pm 10\%$;
5.与其他信号间距遵循3W原则;
6.R1300靠近SOC放置;



U1F
RK3399



SDMMC design rule:
1.Data[0:3]、cmd走线做为一组，
并行走线并整组包地，组内等长要求为 $\pm 100\text{mil}$;
2.Clk需要单独走线并包地处理，与data间的
延时小于 20ps ;
4.Max trace length < 3.93 inches;
5.Trace impedance $50\text{ohm} \pm 10\%$;
6.与其他信号间距遵循3W原则;

PINE64

Title

RockPro64_RK3399

Size

Document Number

Rev

RK3399 FLASH&SDMMC

V2.0

Date:

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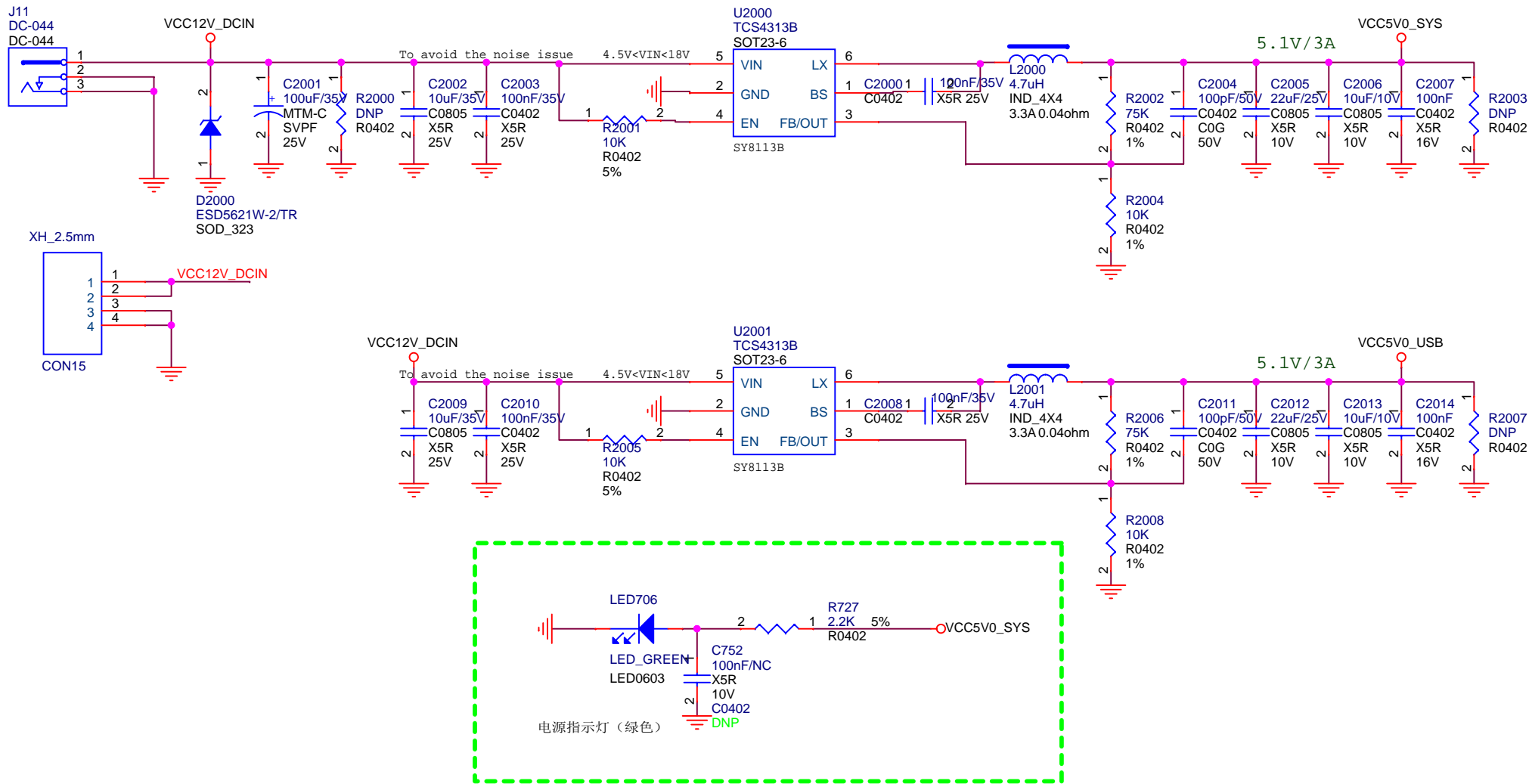
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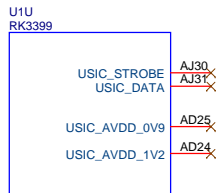
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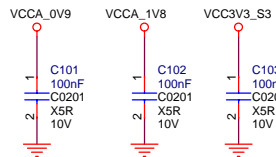
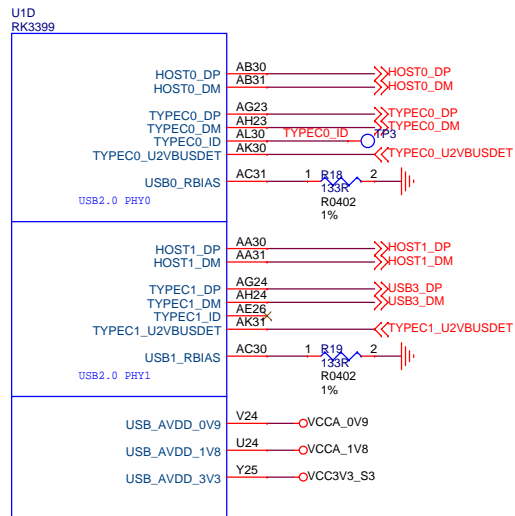
DC IN&SYSTEM Power



PINE64		
Title		
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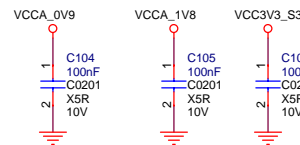
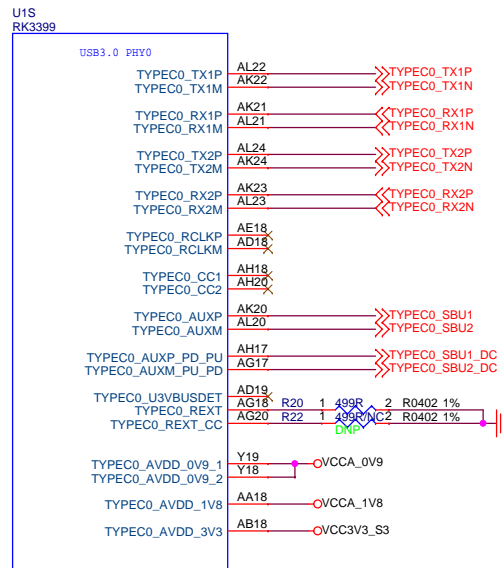


USB2.0

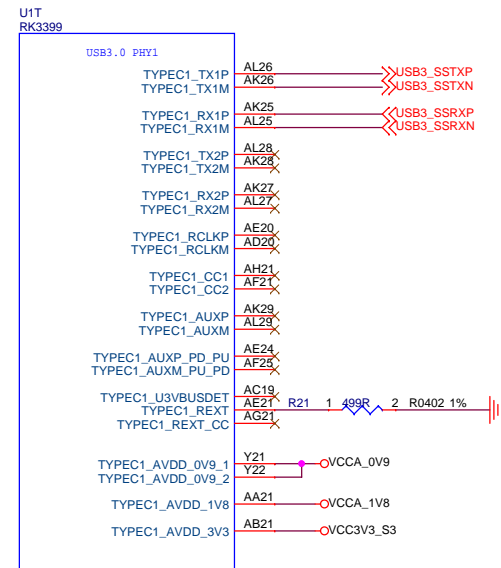


USB2.0 design rule:
 1.Max intra-pair skew < 4 ps;
 2.Max trace length < 6 inchs;
 3.Max allowed via < 6;
 4.Trace impedance 90ohm+/-10%;
 5.与其他信号间距遵循3W原则;

USB3.0

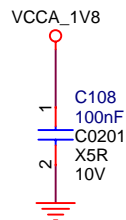
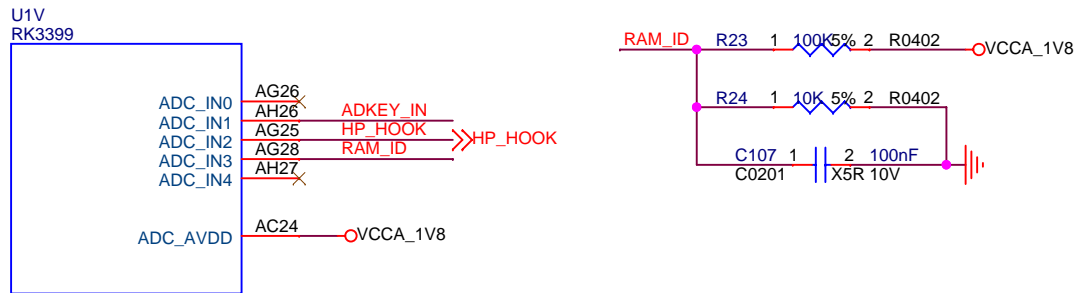


USB3.0 design rule:
 1.Max intra-pair skew < 4 ps;
 2.Max length skew between TX and RX < 1.6 ns;
 3.Max trace length < 6 inchs;
 4.Max allowed via < 4;
 5.Trace impedance 90ohm+/-10%;
 6.与其他信号间距遵循3W原则;



DP design rule:
 1.Max intra-pair skew < 4 ps;
 2.Max trace length < 6 inchs;
 3.Max allowed via < 4;
 4.Trace impedance 90ohm+/-10%;
 5.与其他信号间距遵循3W原则;

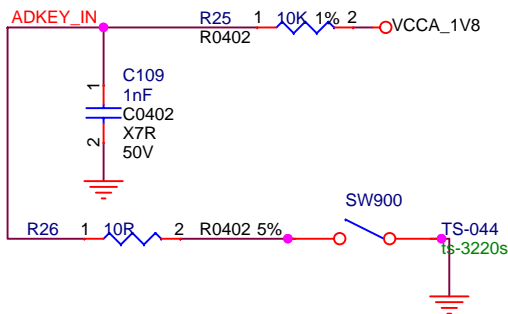
PINE64		
Title		
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	RAM ID	R1501 PU	R1502 PD
DDR3/DDR3L	0.6V	200K	100K
LPDDR3	0.112V	150K	10K
LPDDR4	1.5V	100K	499K

调试升级按键

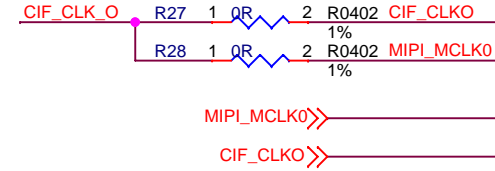
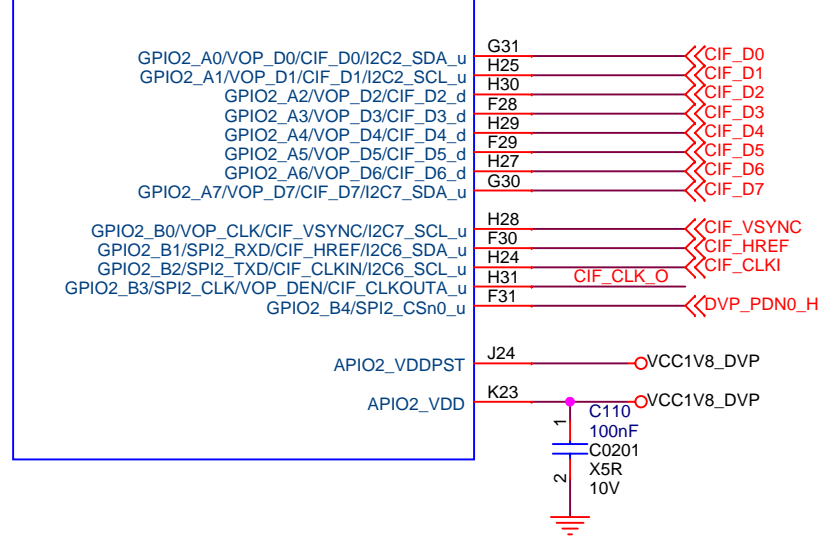
Note:
系统上电时，如果ADKEY_IN电平为0V，
则RK3399进入Recovery模式；



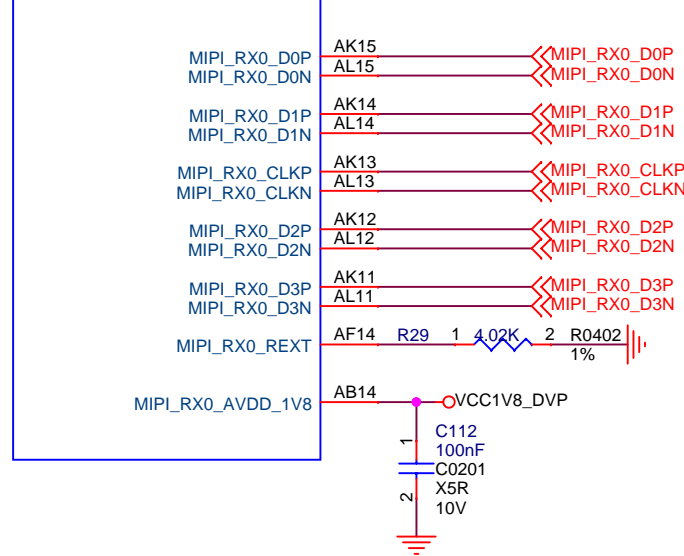
PINE64

Title			RockPro64_RK3399		
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A4	RK3399 SARADC/KEY				V2.0
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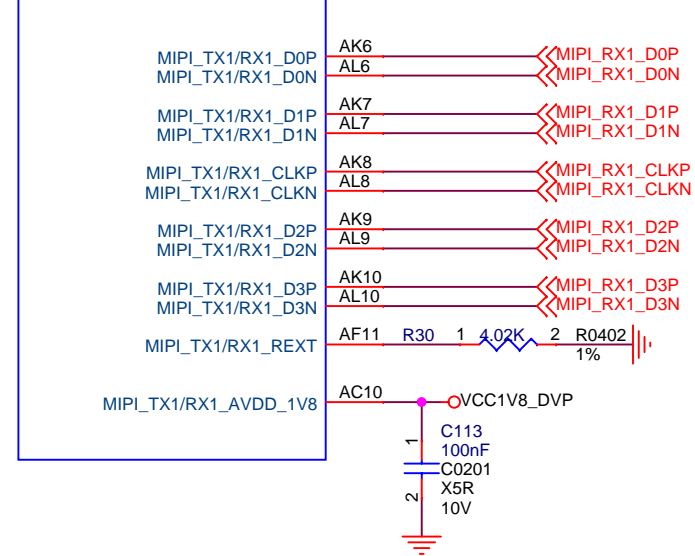
U1L
RK3399



U1R
RK3399



U1P
RK3399



PINE64

Title

RockPro64_RK3399

Size

Document Number

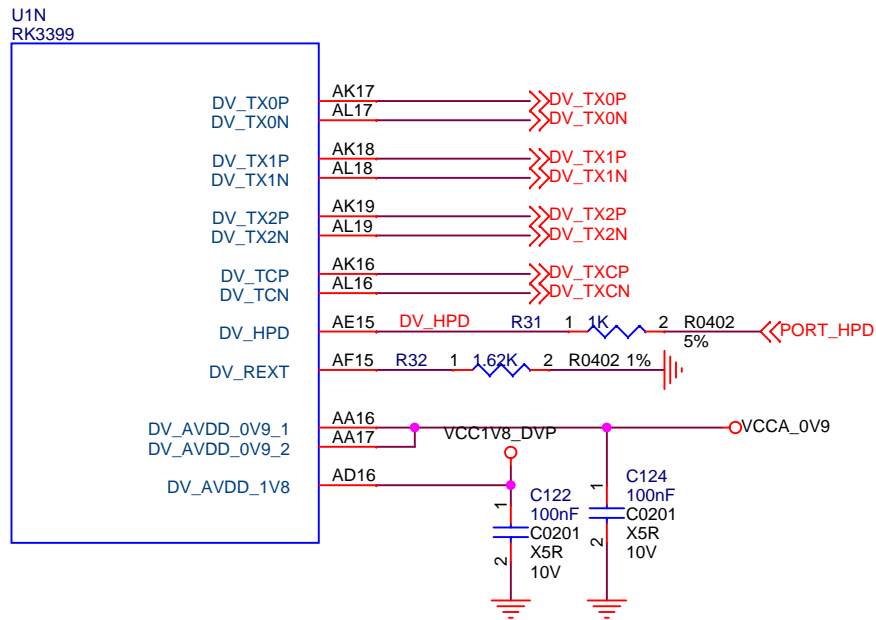
Rev

RK3399 DVP Interface

V2.0

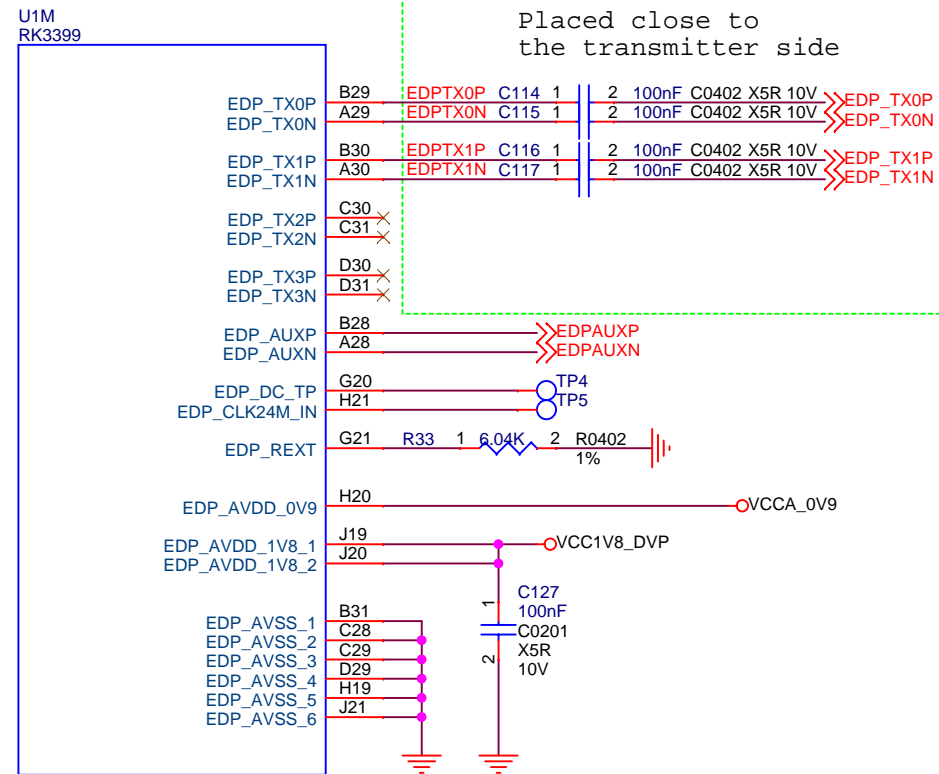
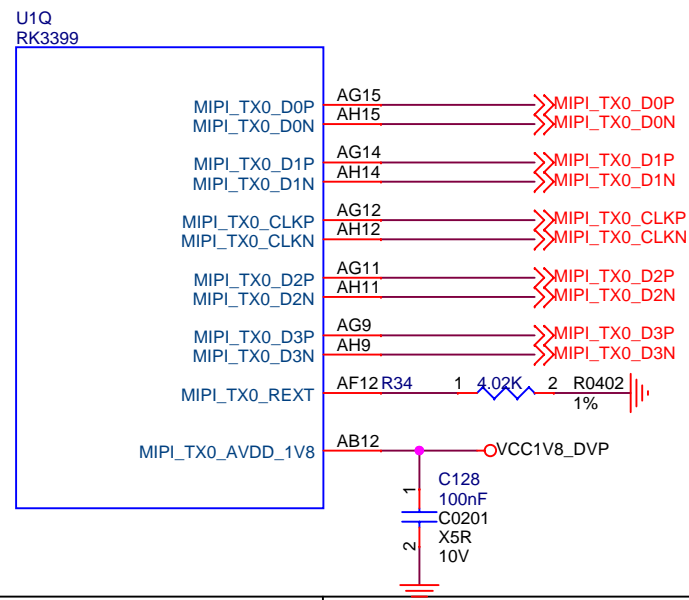
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Digital Video design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 80 ps;
- 3.Max trace length < 9.8 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.与其他信号间距遵循3W原则;



eDP design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max trace length < 6 inches;
- 3.Max allowed via < 4;
- 4.Trace impedance 90ohm+/-10%;
- 5.与其他信号间距遵循3W原则;

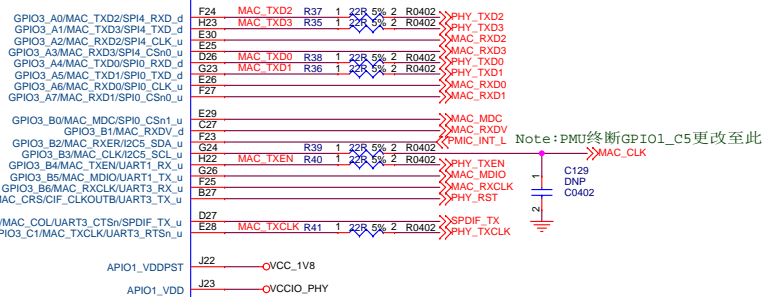
MIPI design rule:

- 1.Max intra-pair skew < 4 ps;
- 2.Max length skew between clk and data < 7ps;
- 3.Max trace length < 7.2 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.与其他信号间距遵循3W原则;

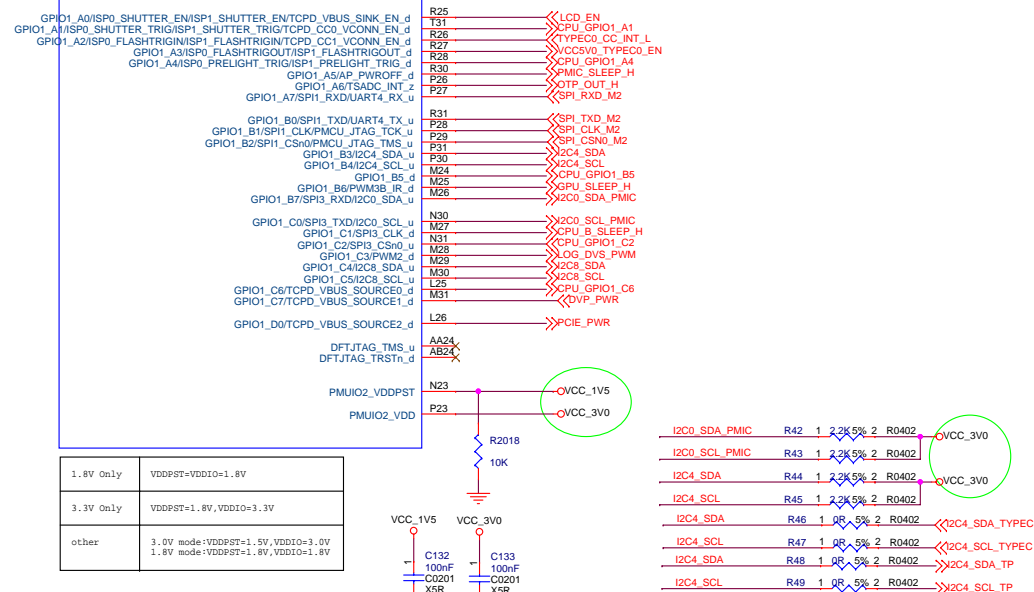
PINE64

Title		
RockPro64_RK3399		
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A4	RK3399 Display Interface	V2.0
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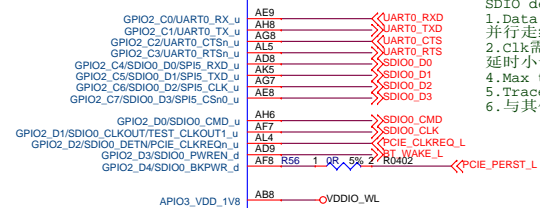
U1I
RK3399 Note:RK3399 part I is 3.3V only



U1E
RK3399 Note:RK3399 part E is 1.8V/3.0V mode

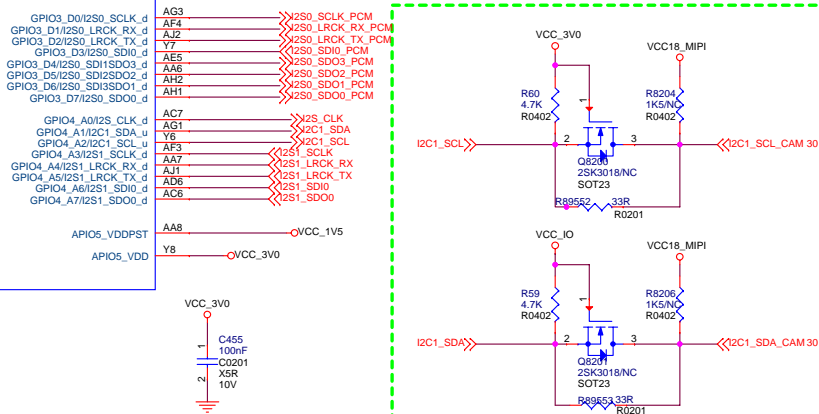


U1G
RK3399 Note:RK3399 part G is 1.8V only

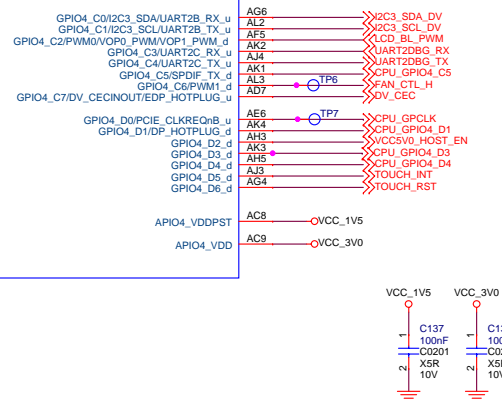


SDIO design rule:
1.Data[0:3]、cmd走线做为一组，并行走线并整组包地，组内等长要求为+/-100mil；
2.CLK需要单独走线并包地处理，与data间的延时小于20ps；
4.Max trace length < 3.93 inches；
5.Trace impedance 50ohm/-10%；
6.与其他信号间距遵循3W原则；

U1J
RK3399 Note:RK3399 part J is 1.8V/3.0V mode



U1K
RK3399 Note:RK3399 part J is 1.8V/3.0V mode

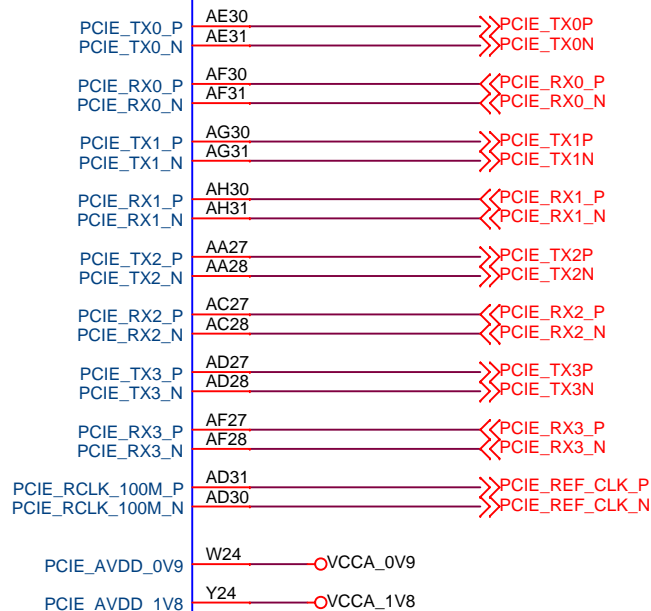


PINE64

RockPro64_RK3399

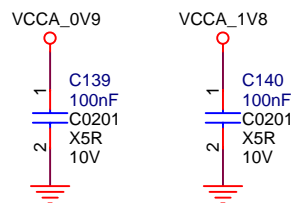
Size Document Number
Custom RK3399 GPIO
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U10
RK3399



PCIE design rule:

- 1.Max intra-pair skew < 4ps;
- 2.Max inter-pair skew < 1.6 ns;
- 3.Max trace length < 14 inches;
- 4.Max allowed via < 4;
- 5.Trace impedance 100ohm+/-10%;
- 6.与其他信号间距遵循3W原则;



PINE64

Title

RockPro64_RK3399

Size

A4

Document Number

RK3399 PCIE

Rev

V2.0

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Tuesday, MAR 6, 2018

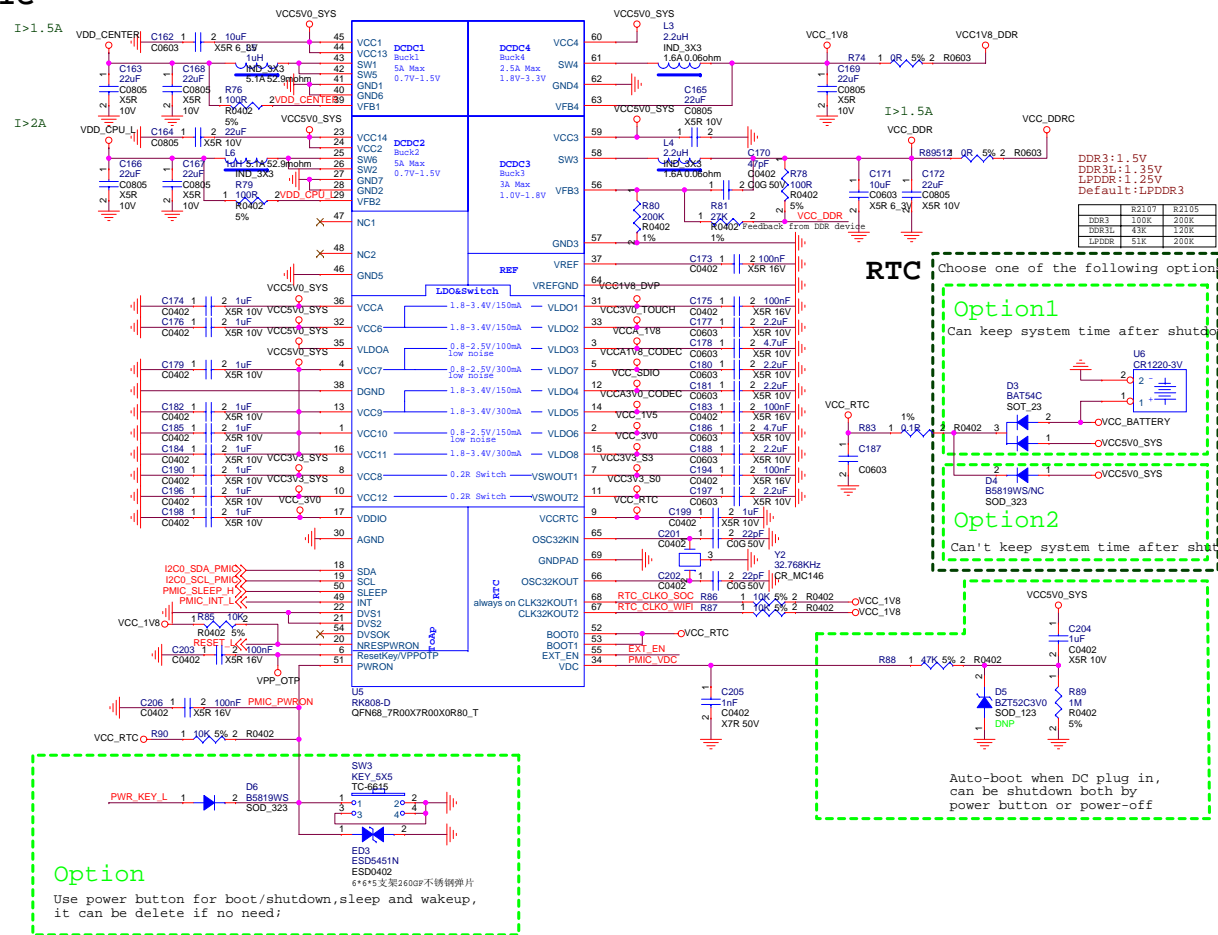
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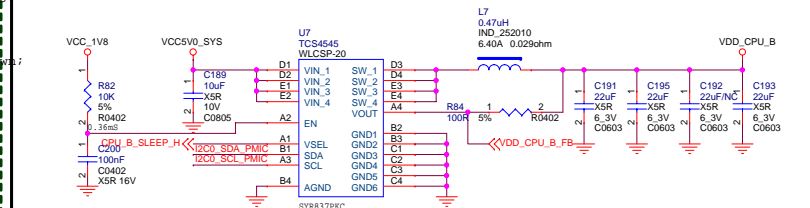
PMIC



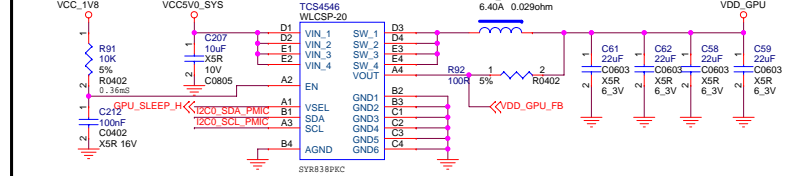
Over-temperature Protection

复位电路修改

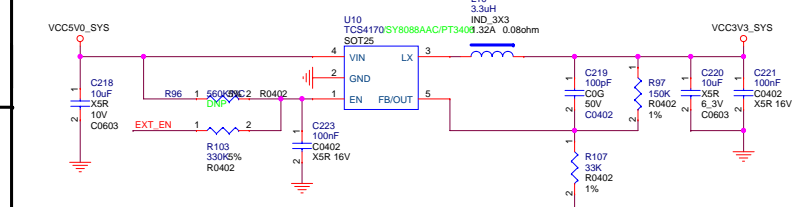
VDD_CPU_B power



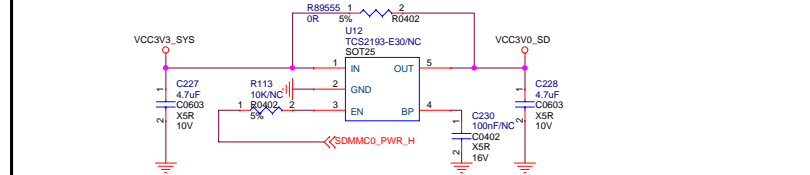
VDD_GPU power



VCC3V3_SYS power



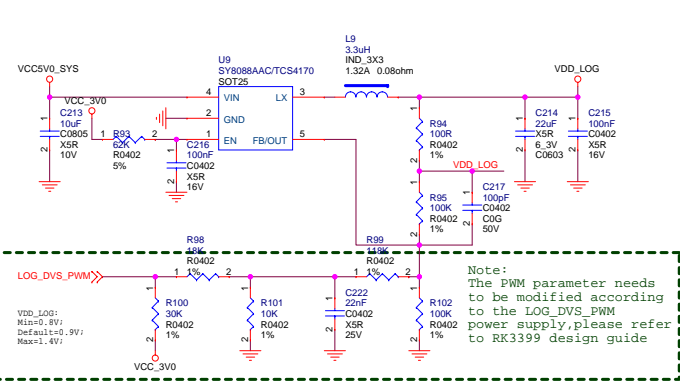
VCC3V0_SD power



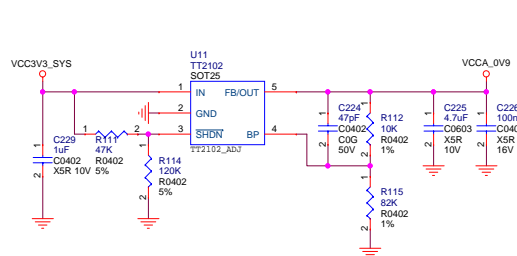
PINE64

File	RockPro64_RK3399	Rev	V2.0
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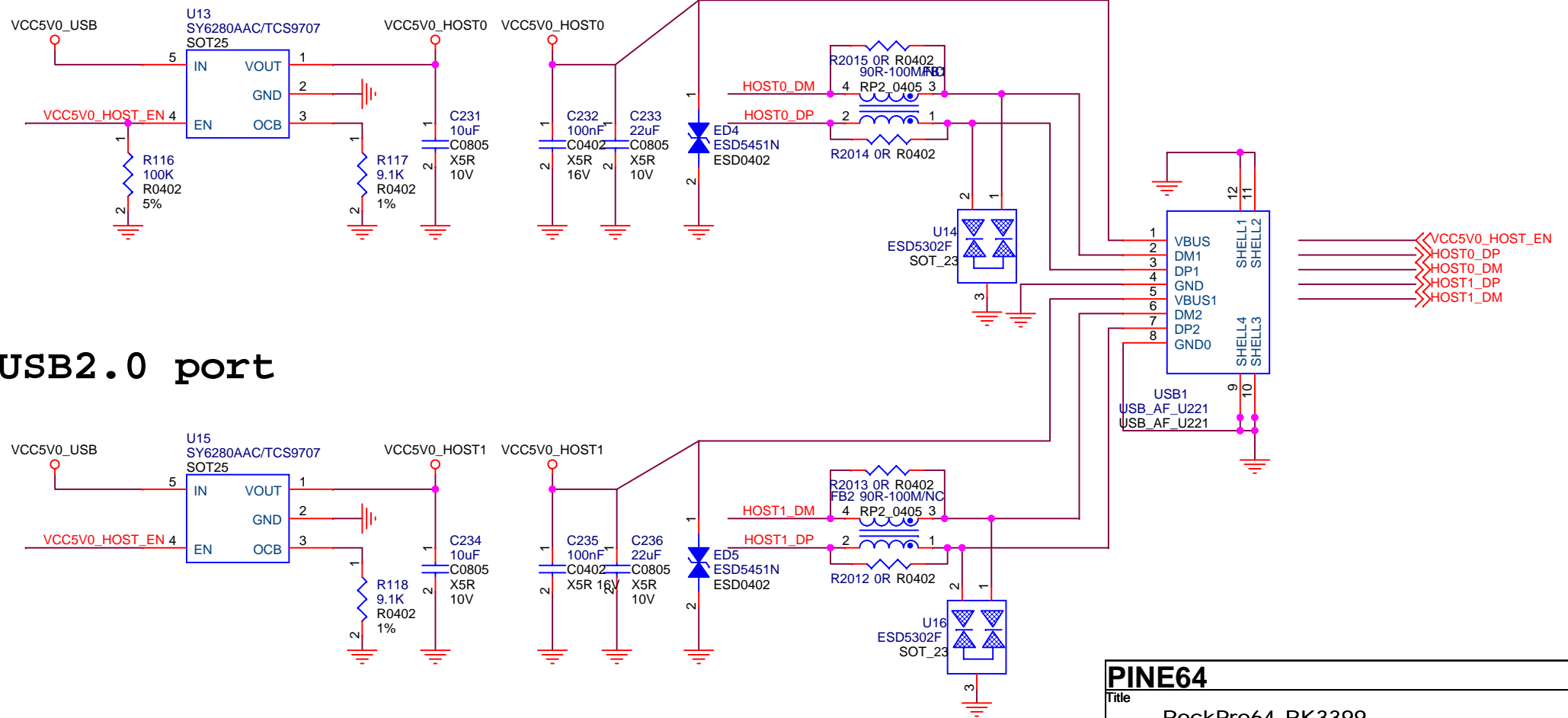
VDD_LOG power



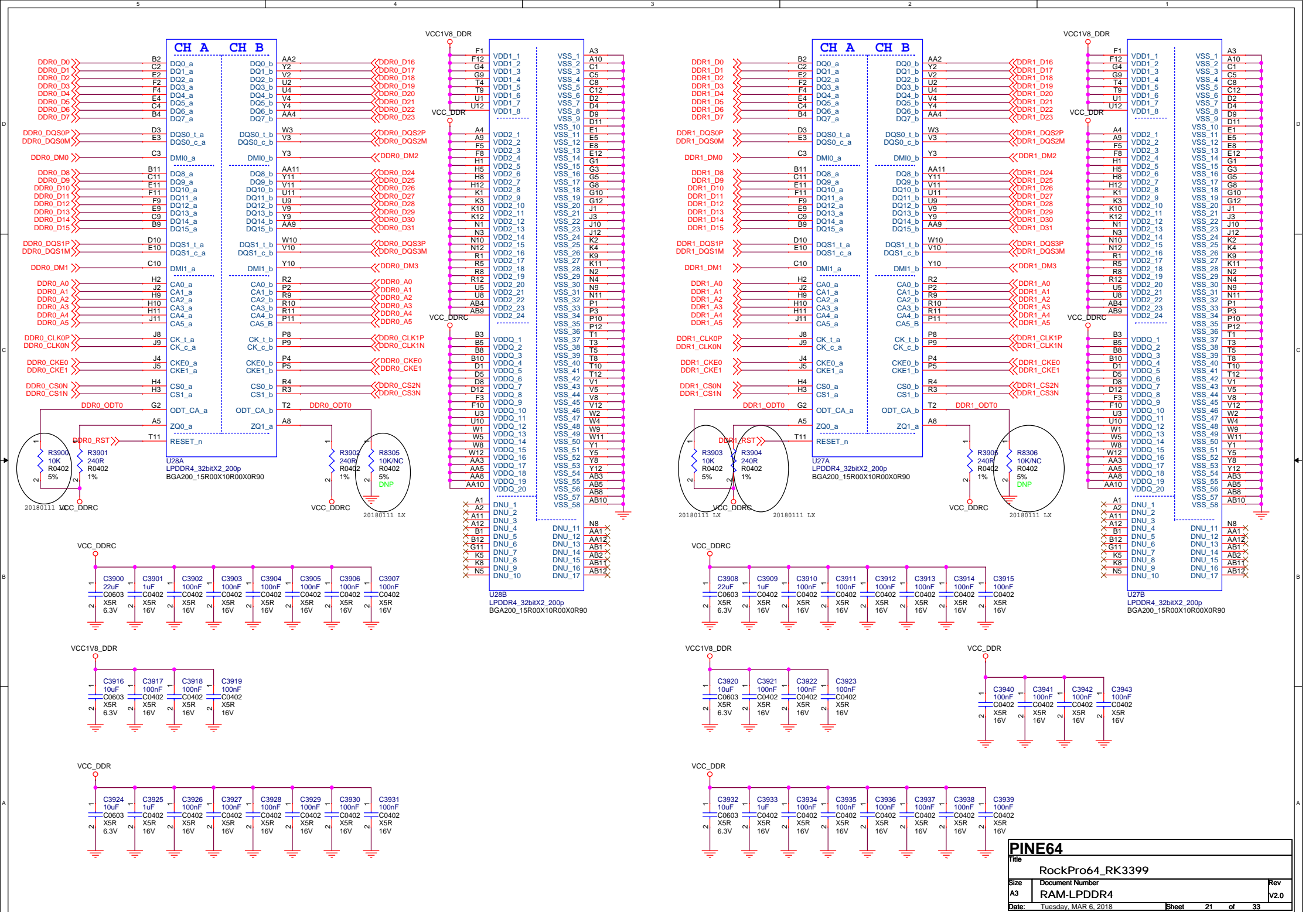
VCC0V9 power



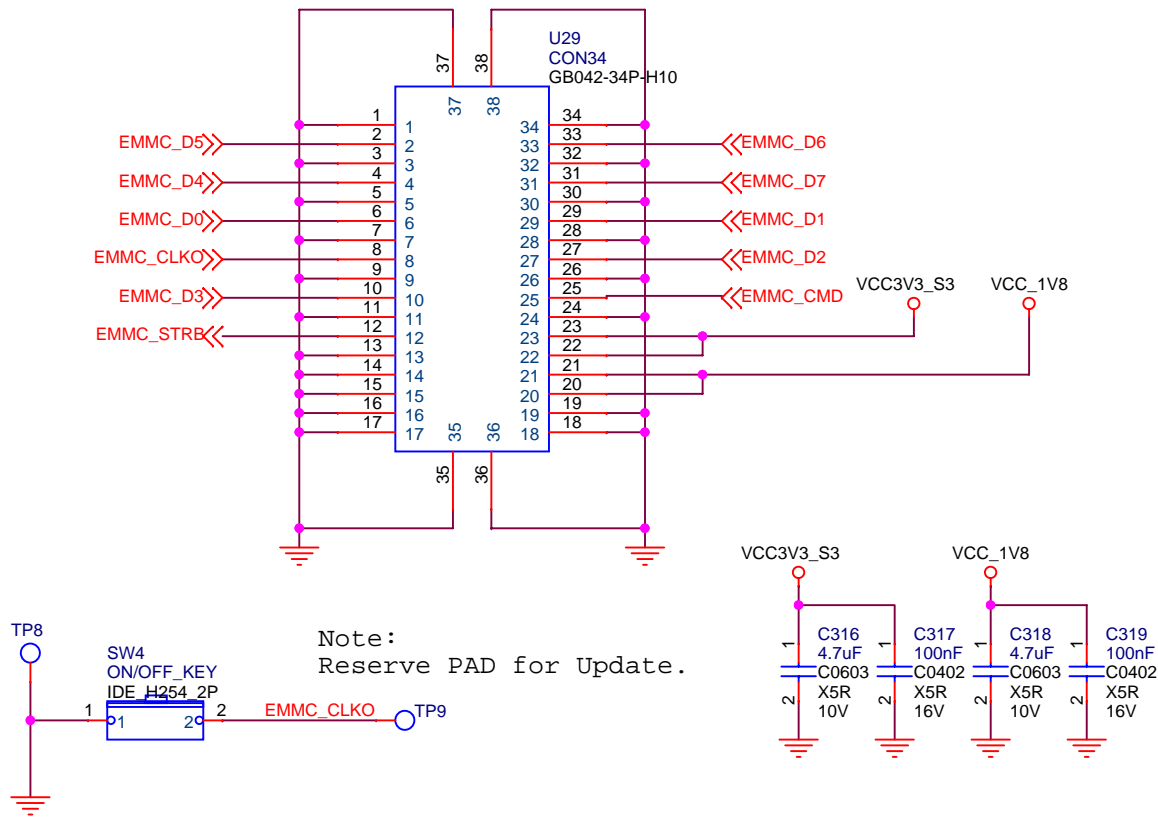
USB2.0 port



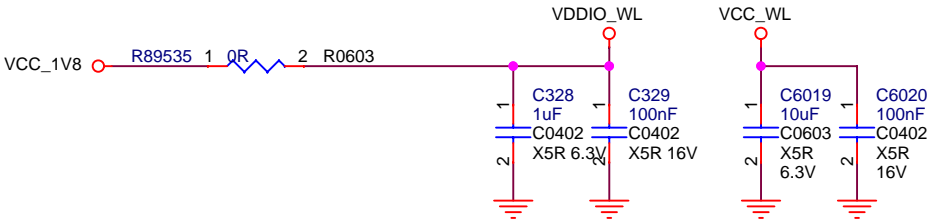
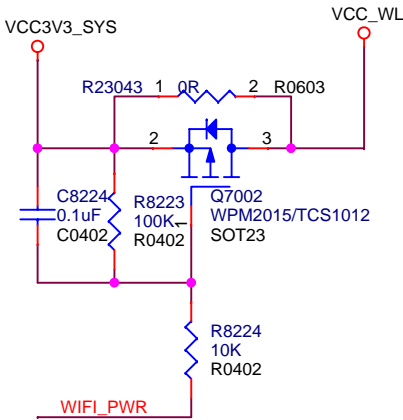
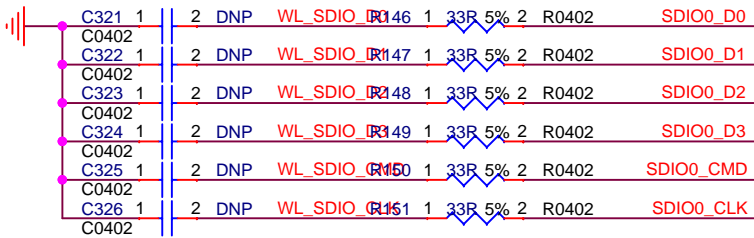
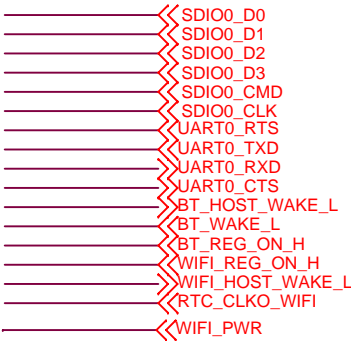
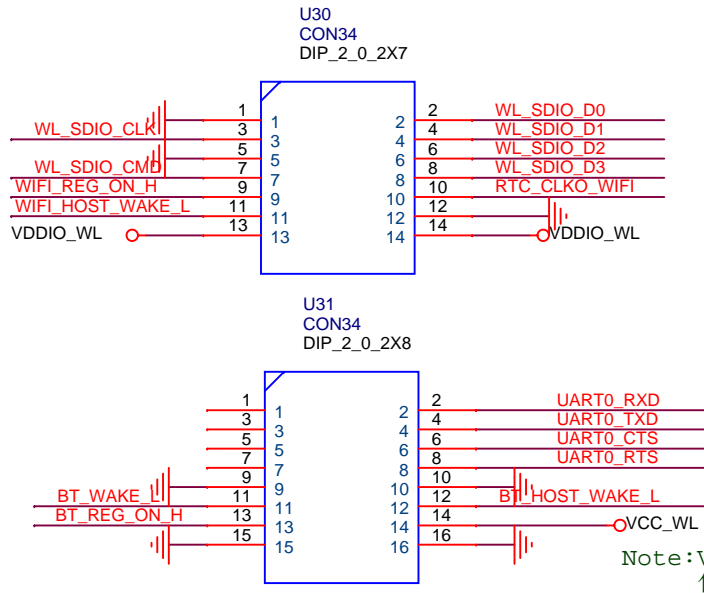
PINE64		
Title		
RockPro64_RK3399		
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eMMC Port

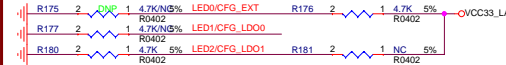
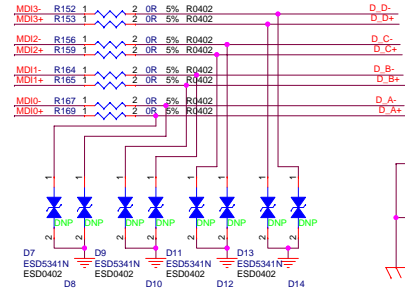


SDIO WIFI/BT MODULE-MIMO



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Title		
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J32



VCCIO_PHY Voltage Config

PHY_RXD3/PHYAD0 R182 2 1 4.7K 5% R0402 VCCIO_P1

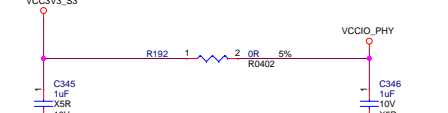
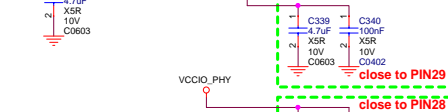
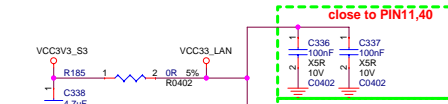
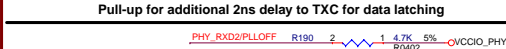
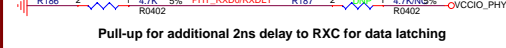
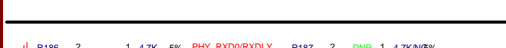
R183 2 1 4.7K 5% PHY_RXCLX/PHYAD1

R184 2 1 4.7K 5% PHY_RXD0/PHYAD2

PHY Address Config

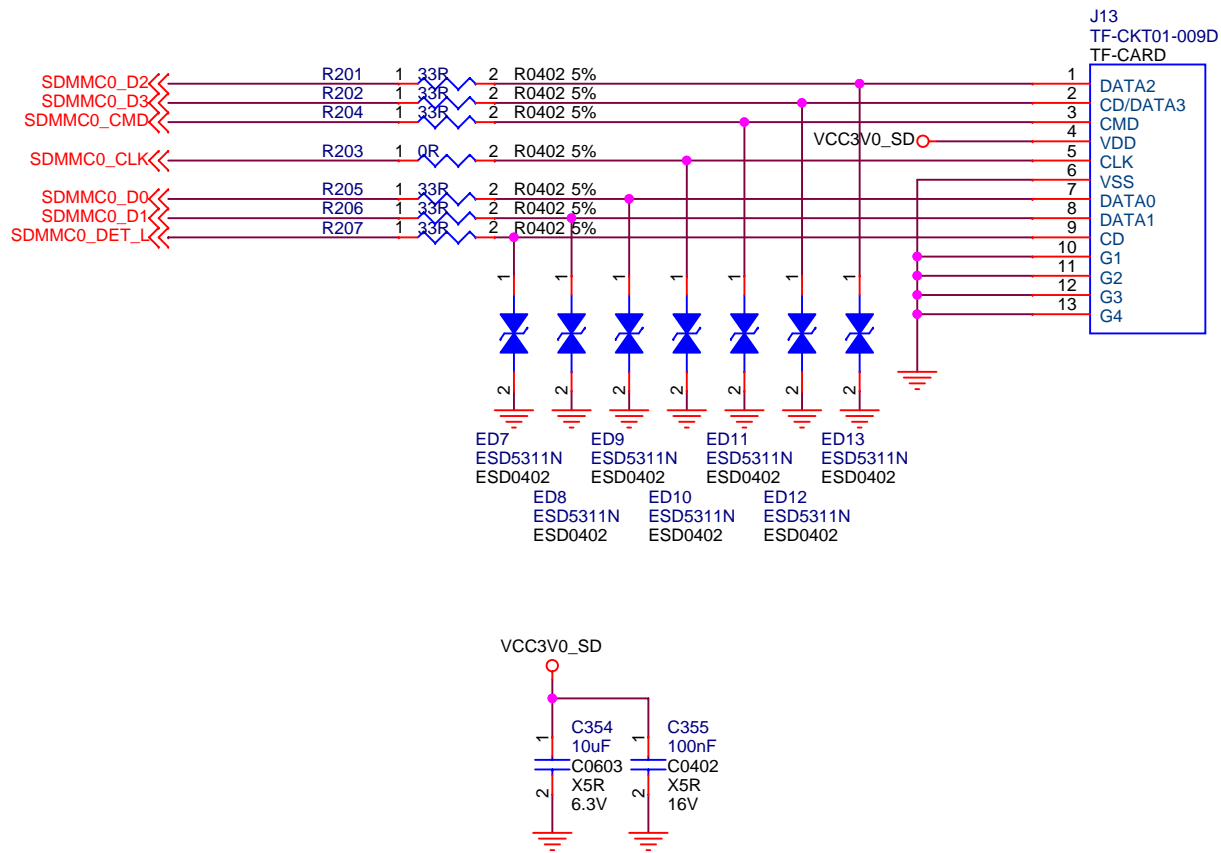
PHY Address PHYAD[2:0]

(default) 3'b001



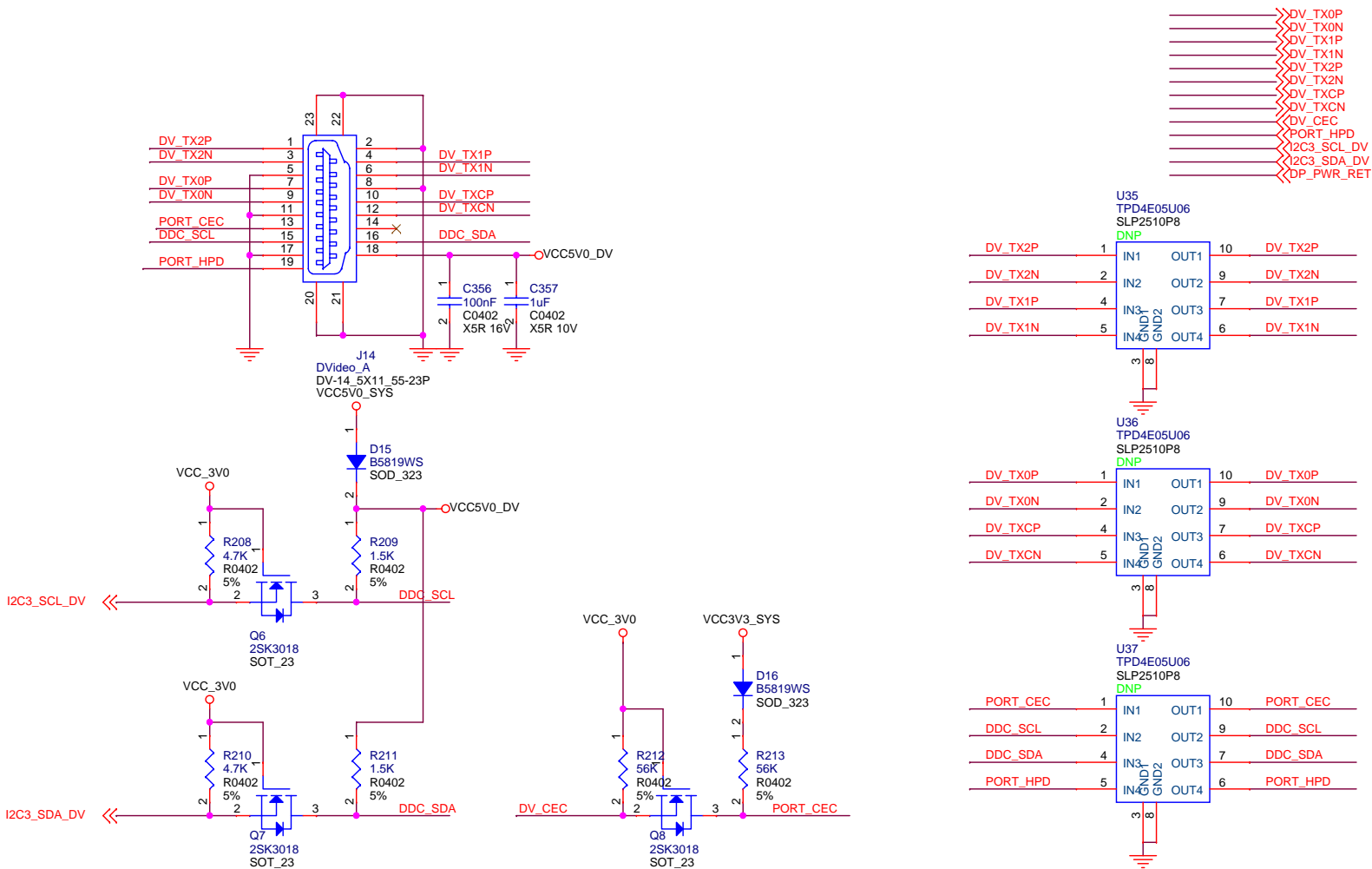
PINE64			
Title RockPro64_RK3399			
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TF CARD



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Digital Video Output



PINE64

RockPro64_RK3399

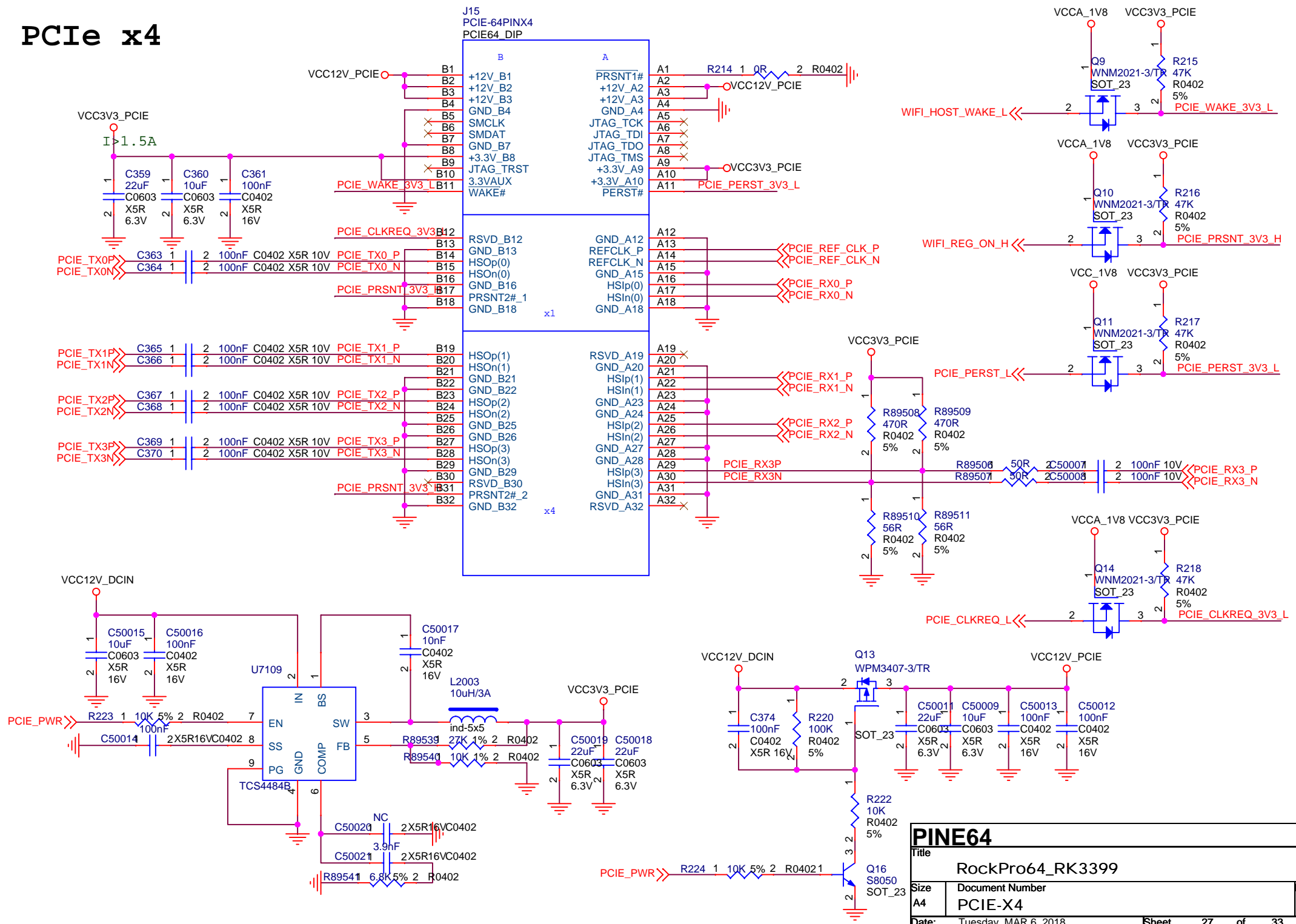
Document Number
CUSTOMER
DIGITAL VIDEO PORT

Rev
V2.0

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PCIe x4

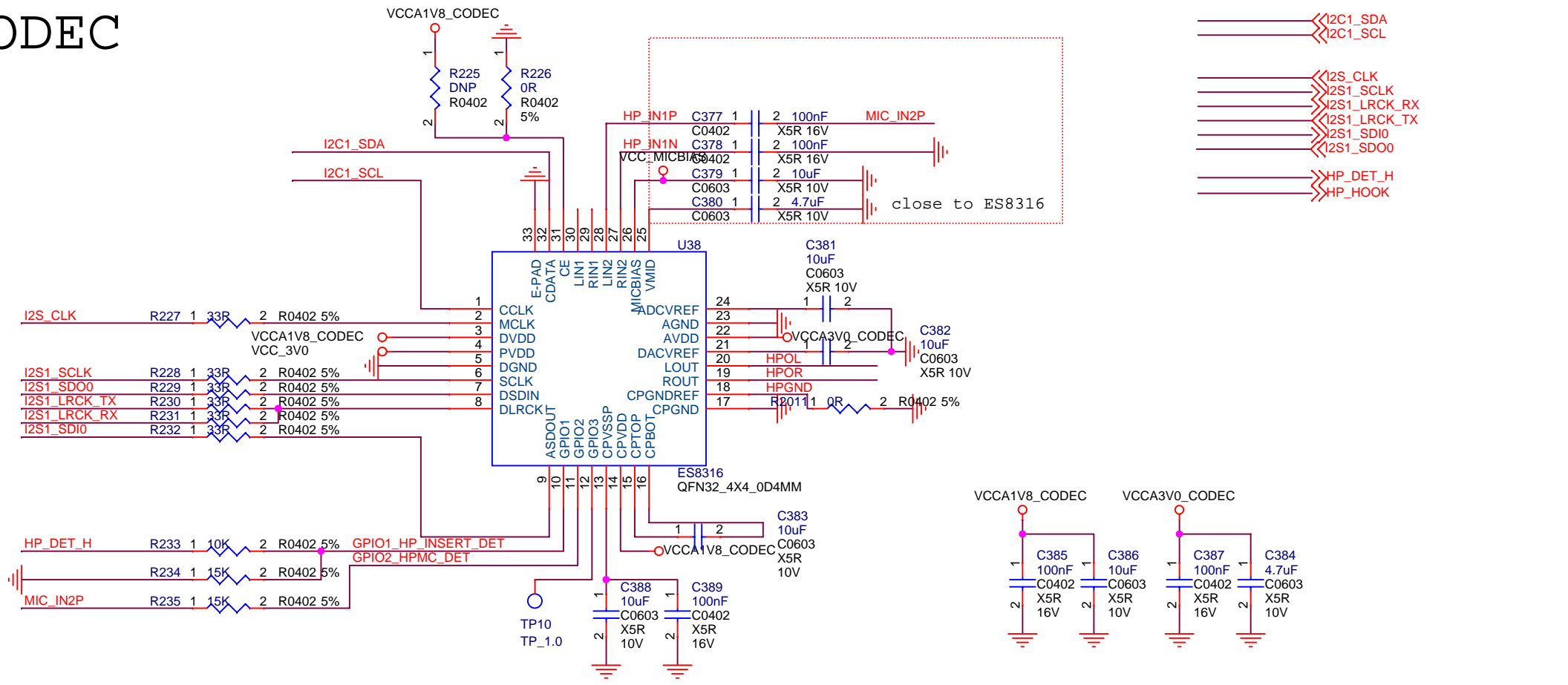
**PINE64**

Title	RockPro64_RK3399
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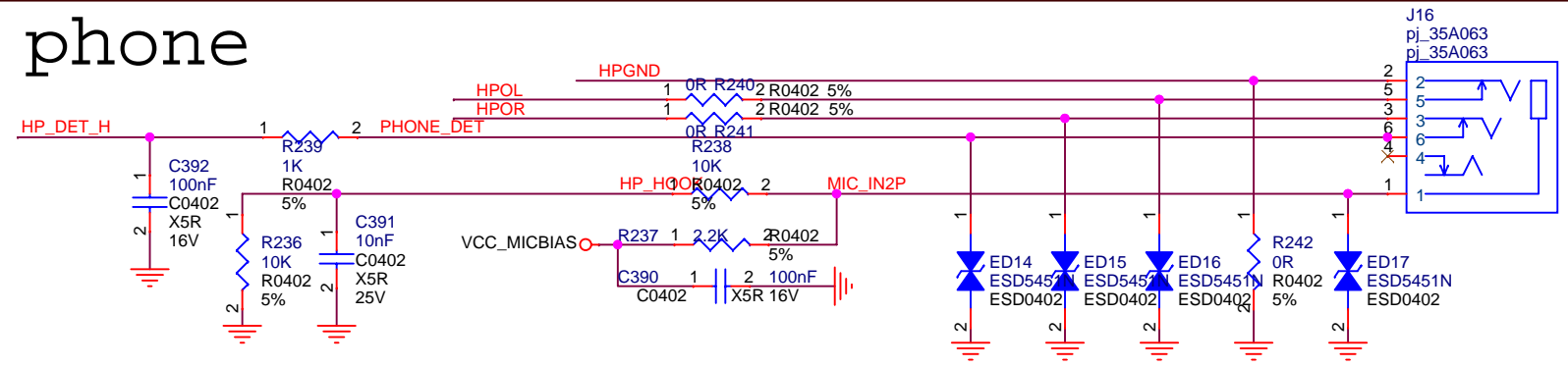
Size	Document Number
A4	PCIE-X4

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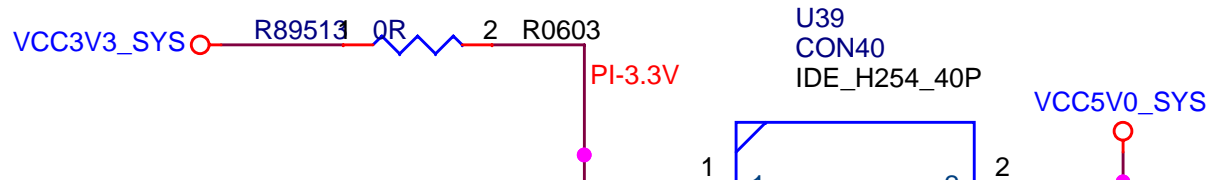
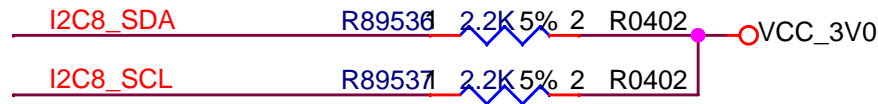
CODEC



Head phone

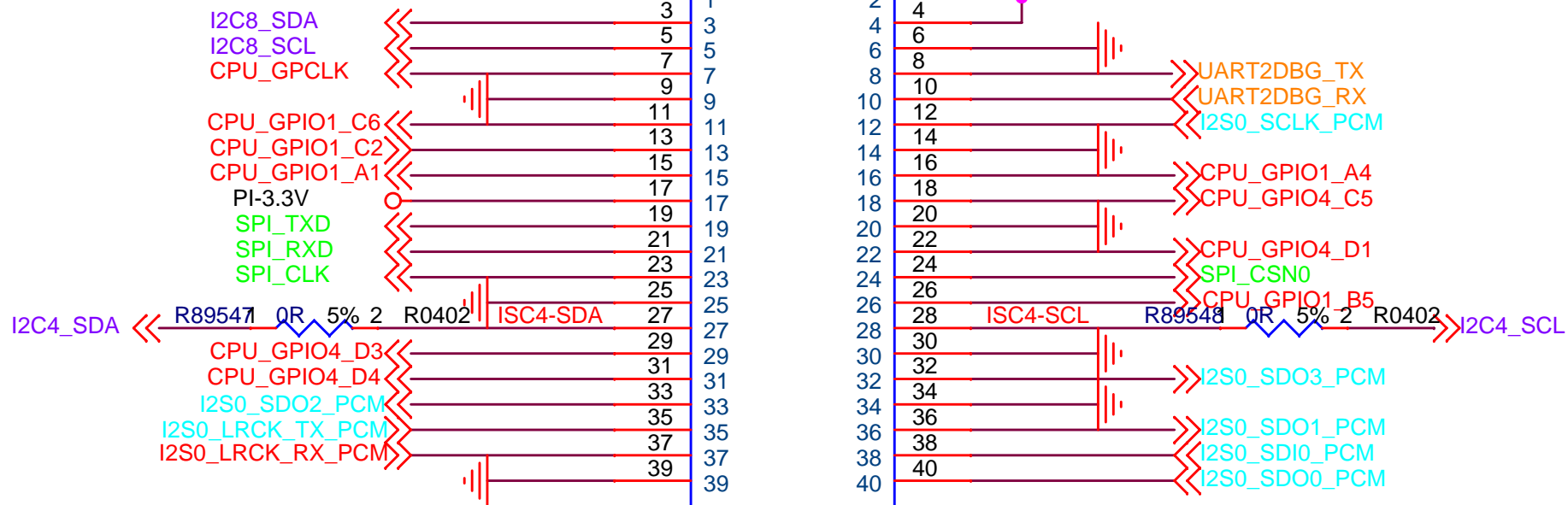


PINE64		
Title		
RockPro64_RK3399		
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U39
CON40
IDE_H254_40P

VCC5V0_SYS



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Diagram illustrating the eDP Panel connection and power supply circuitry for the PINE64 RockPro64_RK3399.

Panel Connections:

- EDP_TX0N, EDP_TX0P, EDP_TX1N, EDP_TX1P
- EDPAUXN, EDPAUXP, LCD_BL_PWM, LCD_EN, LCD_RST

Power Supply and Control Circuits:

- VCC12V_DCIN:** Input to the main power regulator.
- VCC_12V:** Output of the main power regulator.
- VCC3V3_S0:** Output of the 3.3V regulator.
- VCC12V:** Output of the 12V regulator.
- LCD_EN:** Input to the LCD enable driver.
- LCD_RST:** Input to the LCD reset driver.

Components:

- Q2109: WPM3407-3/TR (Main Power Regulator)
- Q2108: S8050 (LCD Enable Driver)
- Q2107: S8050 (LCD Reset Driver)
- R89542, R89543, R89544: Resistors
- C50022, C0402, C2015, C460, C2017, C429, C430, C0603, C0402: Capacitors

Pin Header Connections:

- 1: NC
- 2: H_GND
- 3: ML1-
- 4: ML1+
- 5: H_GND1
- 6: ML0-
- 7: ML0+
- 8: H_GND2
- 9: AUX+
- 10: AUX-
- 11: H_GND3
- 12: VCCS
- 13: VCCS1
- 14: NC0
- 15: GND1
- 16: GND2
- 17: HPD
- 18: BL_GND
- 19: BL_GND1
- 20: BL_GND2
- 21: BL_GND3
- 22: LED_EN
- 23: LED_PWM
- 24: NC1
- 25: NC2
- 26: LED_VCCS
- 27: LED_VCCS1
- 28: LED_VCCS2
- 29: LED_VCCS3
- 30: NC3

Legend:

- EDP_TX0N, EDP_TX0P, EDP_TX1N, EDP_TX1P
- EDPAUXN, EDPAUXP, LCD_BL_PWM, LCD_EN, LCD_RST

Table:

PINE64		
Title		
RockPro64_RK3399		
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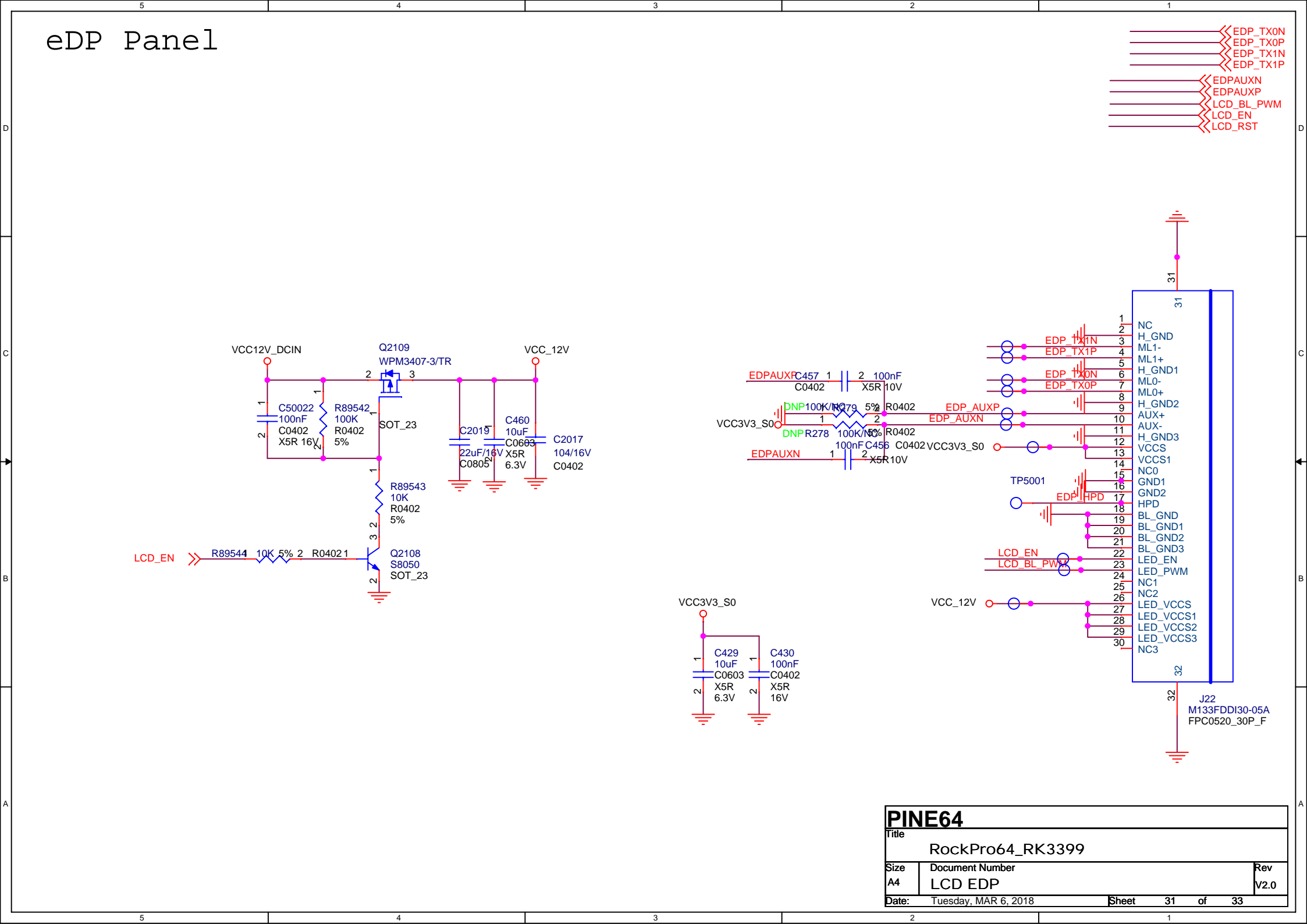
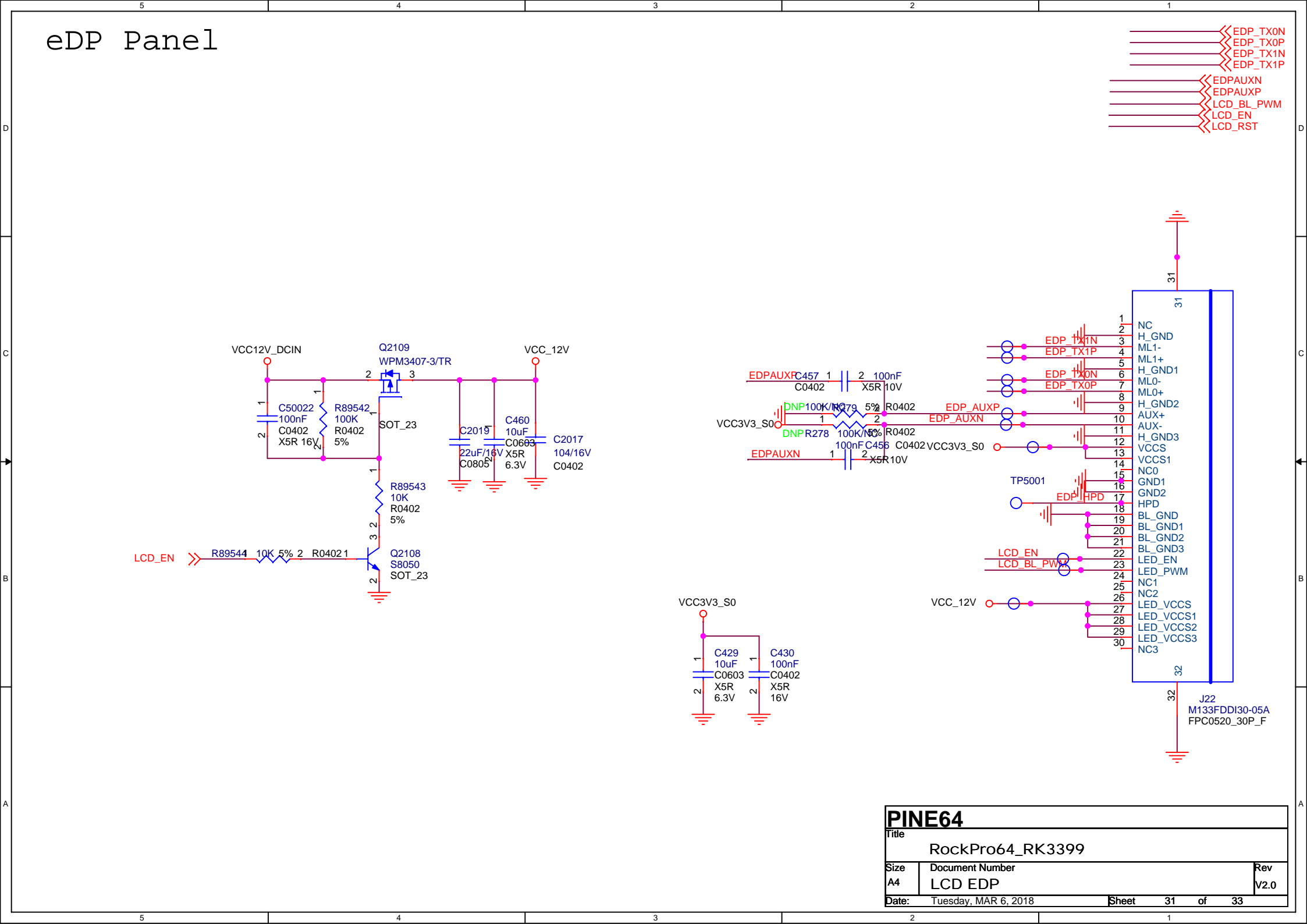


Diagram illustrating the eDP Panel connection and power supply circuitry for the PINE64 RockPro64_RK3399.

Panel Connections:

- EDP_TX0N, EDP_TX0P, EDP_TX1N, EDP_TX1P
- EDPAUXN, EDPAUXP, LCD_BL_PWM, LCD_EN, LCD_RST

Power Supply and Control Circuits:

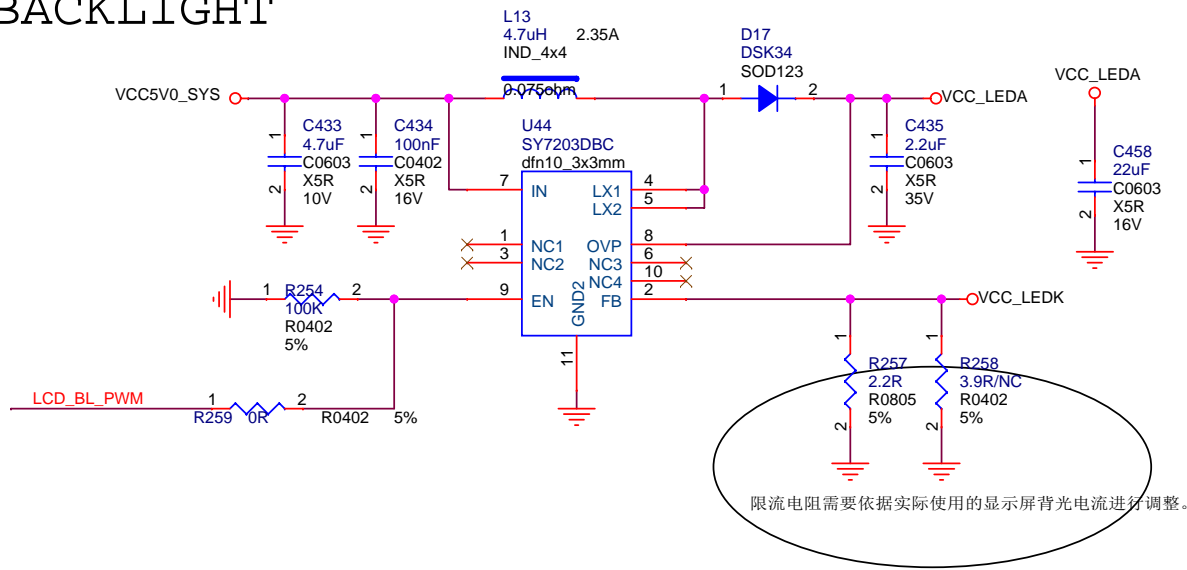
- VCC12V_DCIN:** Input to the main power supply.
- VCC_12V:** Output of the main power supply.
- VCC3V3_S0:** Output of the 3.3V regulator.
- VCC12V:** Output of the 12V regulator.
- LCD_EN:** Input to the LCD enable driver.
- LCD_RST:** Input to the LCD reset driver.

Components:

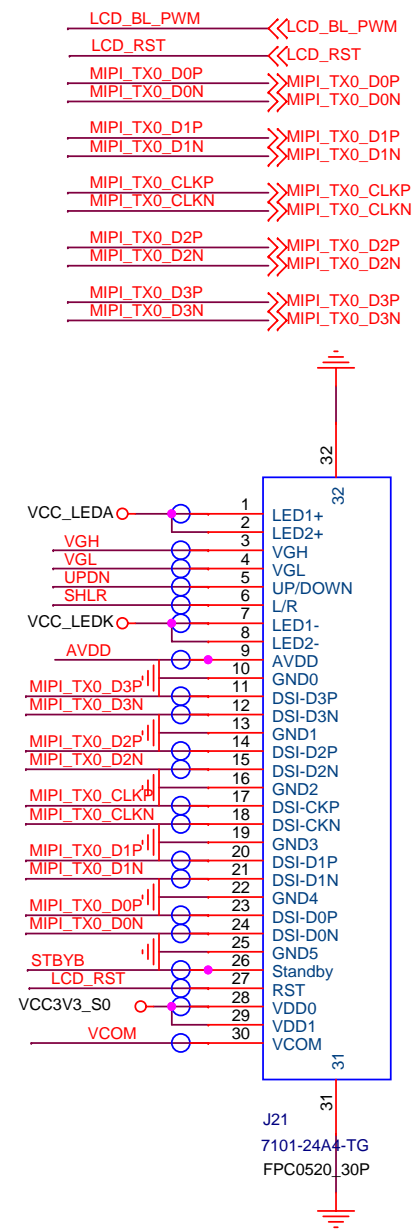
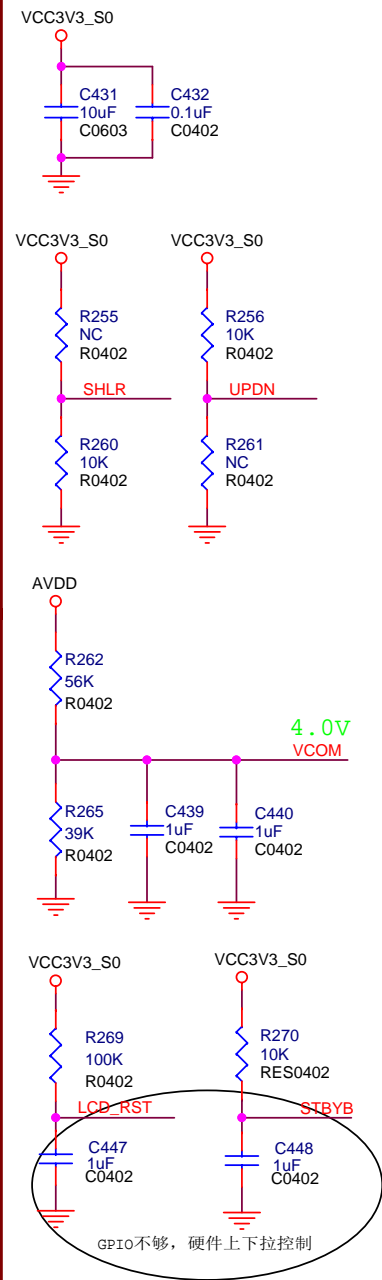
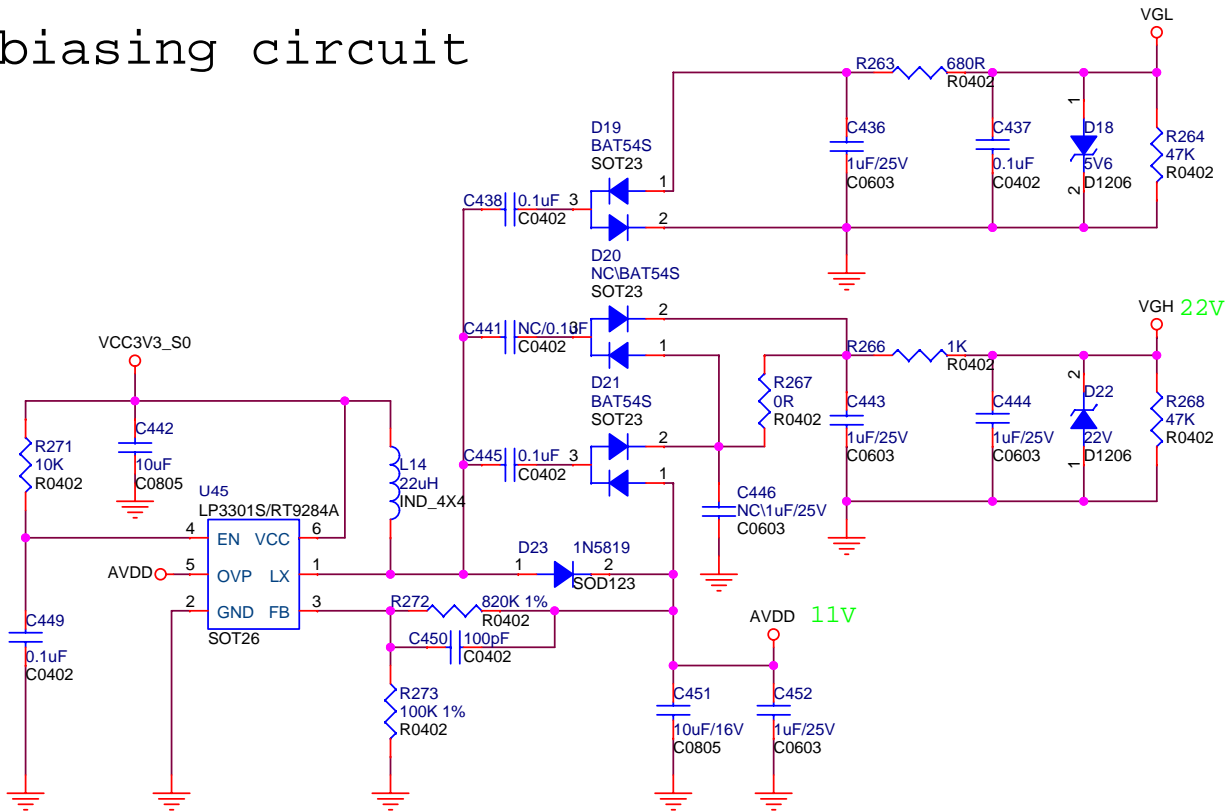
- Q2109: WPM3407-3/TR (MOSFET)
- Q2108: S8050 (BJT)
- Q2107: S8050 (BJT)
- Q2106: S8050 (BJT)
- Q2105: S8050 (BJT)
- Q2104: S8050 (BJT)
- Q2103: S8050 (BJT)
- Q2102: S8050 (BJT)
- Q2101: S8050 (BJT)
- Q2100: S8050 (BJT)
- Q2099: S8050 (BJT)
- Q2098: S8050 (BJT)
- Q2097: S8050 (BJT)
- Q2096: S8050 (BJT)
- Q2095: S8050 (BJT)
- Q2094: S8050 (BJT)
- Q2093: S8050 (BJT)
- Q2092: S8050 (BJT)
- Q2091: S8050 (BJT)
- Q2090: S8050 (BJT)
- Q2089: S8050 (BJT)
- Q2088: S8050 (BJT)
- Q2087: S8050 (BJT)
- Q2086: S8050 (BJT)
- Q2085: S8050 (BJT)
- Q2084: S8050 (BJT)
- Q2083: S8050 (BJT)
- Q2082: S8050 (BJT)
- Q2081: S8050 (BJT)
- Q2080: S8050 (BJT)
- Q2079: S8050 (BJT)
- Q2078: S8050 (BJT)
- Q2077: S8050 (BJT)
- Q2076: S8050 (BJT)
- Q2075: S8050 (BJT)
- Q2074: S8050 (BJT)
- Q2073: S8050 (BJT)
- Q2072: S8050 (BJT)
- Q2071: S8050 (BJT)
- Q2070: S8050 (BJT)
- Q2069: S8050 (BJT)
- Q2068: S8050 (BJT)
- Q2067: S8050 (BJT)
- Q2066: S8050 (BJT)
- Q2065: S8050 (BJT)
- Q2064: S8050 (BJT)
- Q2063: S8050 (BJT)
- Q2062: S8050 (BJT)
- Q2061: S8050 (BJT)
- Q2060: S8050 (BJT)
- Q2059: S8050 (BJT)
- Q2058: S8050 (BJT)
- Q2057: S8050 (BJT)
- Q2056: S8050 (BJT)
- Q2055: S8050 (BJT)
- Q2054: S8050 (BJT)
- Q2053: S8050 (BJT)
- Q2052: S8050 (BJT)
- Q2051: S8050 (BJT)
- Q2050: S8050 (BJT)
- Q2049: S8050 (BJT)
- Q2048: S8050 (BJT)
- Q2047: S8050 (BJT)
- Q2046: S8050 (BJT)
- Q2045: S8050 (BJT)
- Q2044: S8050 (BJT)
- Q2043: S8050 (BJT)
- Q2042: S8050 (BJT)
- Q2041: S8050 (BJT)
- Q2040: S8050 (BJT)
- Q2039: S8050 (BJT)
- Q2038: S8050 (BJT)
- Q2037: S8050 (BJT)
- Q2036: S8050 (BJT)
- Q2035: S8050 (BJT)
- Q2034: S8050 (BJT)
- Q2033: S8050 (BJT)
- Q2032: S8050 (BJT)
- Q2031: S8050 (BJT)
- Q2030: S8050 (BJT)
- Q2029: S8050 (BJT)
- Q2028: S8050 (BJT)
- Q2027: S8050 (BJT)
- Q2026: S8050 (BJT)
- Q2025: S8050 (BJT)
- Q2024: S8050 (BJT)
- Q2023: S8050 (BJT)
- Q2022: S8050 (BJT)
- Q2021: S8050 (BJT)
- Q2020: S8050 (BJT)
- Q2019: S8050 (BJT)
- Q2018: S8050 (BJT)
- Q2017: S8050 (BJT)
- Q2016: S8050 (BJT)
- Q2015: S8050 (BJT)
- Q2014: S8050 (BJT)
- Q2013: S8050 (BJT)
- Q2012: S8050 (BJT)
- Q2011: S8050 (BJT)
- Q2010: S8050 (BJT)
- Q2009: S8050 (BJT)
- Q2008: S8050 (BJT)
- Q2007: S8050 (BJT)
- Q2006: S8050 (BJT)
- Q2005: S8050 (BJT)
- Q2004: S8050 (BJT)
- Q2003: S8050 (BJT)
- Q2002: S8050 (BJT)
- Q2001: S8050 (BJT)
- Q2000: S8050 (BJT)
- Q1999: S8050 (BJT)
- Q1998: S8050 (BJT)
- Q1997: S8050 (BJT)
- Q1996: S8050 (BJT)
- Q1995: S8050 (BJT)
- Q1994: S8050 (BJT)
- Q1993: S8050 (BJT)
- Q1992: S8050 (BJT)
- Q1991: S8050 (BJT)
- Q1990: S8050 (BJT)
- Q1989: S8050 (BJT)
- Q1988: S8050 (BJT)
- Q1987: S8050 (BJT)
- Q1986: S8050 (BJT)
- Q1985: S8050 (BJT)
- Q1984: S8050 (BJT)
- Q1983: S8050 (BJT)
- Q1982: S8050 (BJT)
- Q1981: S8050 (BJT)
- Q1980: S8050 (BJT)
- Q1979: S8050 (BJT)
- Q1978: S8050 (BJT)
- Q1977: S8050 (BJT)
- Q1976: S8050 (BJT)
- Q1975: S8050 (BJT)
- Q1974: S8050 (BJT)
- Q1973: S8050 (BJT)
- Q1972: S8050 (BJT)
- Q1971: S8050 (BJT)
- Q1970: S8050 (BJT)
- Q1969: S8050 (BJT)
- Q1968: S8050 (BJT)
- Q1967: S8050 (BJT)
- Q1966: S8050 (BJT)
- Q1965: S8050 (BJT)
- Q1964: S8050 (BJT)
- Q1963: S8050 (BJT)
- Q1962: S8050 (BJT)
- Q1961: S8050 (BJT)
- Q1960: S8050 (BJT)
- Q1959: S8050 (BJT)
- Q1958: S8050 (BJT)
- Q1957: S8050 (BJT)
- Q1956: S8050 (BJT)
- Q1955: S8050 (BJT)
- Q1954: S8050 (BJT)
- Q1953: S8050 (BJT)
- Q1952: S8050 (BJT)
- Q1951: S8050 (BJT)
- Q1950: S8050 (BJT)
- Q1949: S8050 (BJT)
- Q1948: S8050 (BJT)
- Q1947: S8050 (BJT)
- Q1946: S8050 (BJT)
- Q1945: S8050 (BJT)
- Q1944: S8050 (BJT)
- Q1943: S8050 (BJT)
- Q1942: S8050 (BJT)
- Q1941: S8050 (BJT)
- Q1940: S8050 (BJT)
- Q1939: S8050 (BJT)
- Q1938: S8050 (BJT)
- Q1937: S8050 (BJT)
- Q1936: S8050 (BJT)
- Q1935: S8050 (BJT)
- Q1934: S8050 (BJT)
- Q1933: S8050 (BJT)
- Q1932: S8050 (BJT)
- Q1931: S8050 (BJT)
- Q1930: S8050 (BJT)
- Q1929: S8050 (BJT)
- Q1928: S8050 (BJT)
- Q1927: S8050 (BJT)
- Q1926: S8050 (BJT)
- Q1925: S8050 (BJT)
- Q1924: S8050 (BJT)
- Q1923: S8050 (BJT)
- Q1922: S8050 (BJT)
- Q1921: S8050 (BJT)
- Q1920: S8050 (BJT)
- Q1919: S8050 (BJT)
- Q1918: S8050 (BJT)
- Q1917: S8050 (BJT)
- Q1916: S8050 (BJT)
- Q1915: S8050 (BJT)
- Q1914: S8050 (BJT)
- Q1913: S8050 (BJT)
- Q1912: S8050 (BJT)
- Q1911: S8050 (BJT)
- Q1910: S8050 (BJT)
- Q1909: S

MIPI Panel

BACKLIGHT

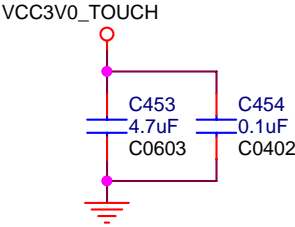
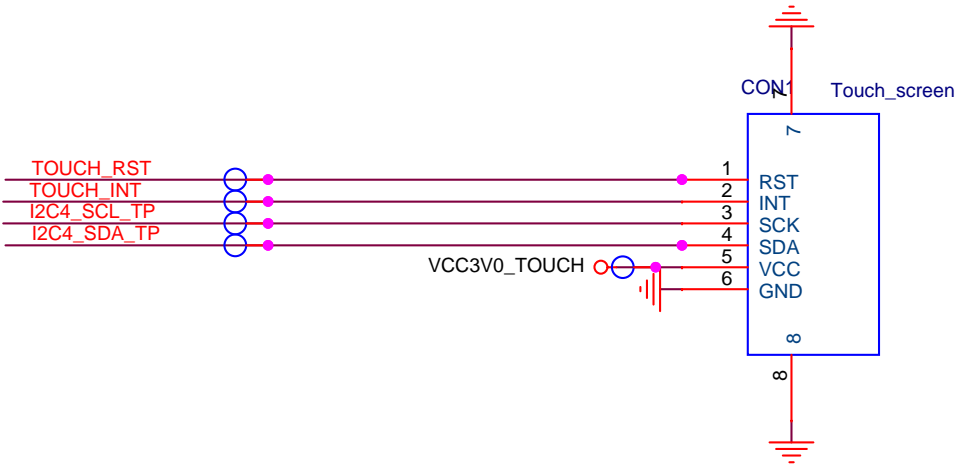


biasing circuit



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Title			
RockPro64_RK3399			
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Touch Panel connector



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A	TP PORT	V2.0
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