BBM233: Logic Design Lab
2022 Fall
Lab Experiment #3 Report

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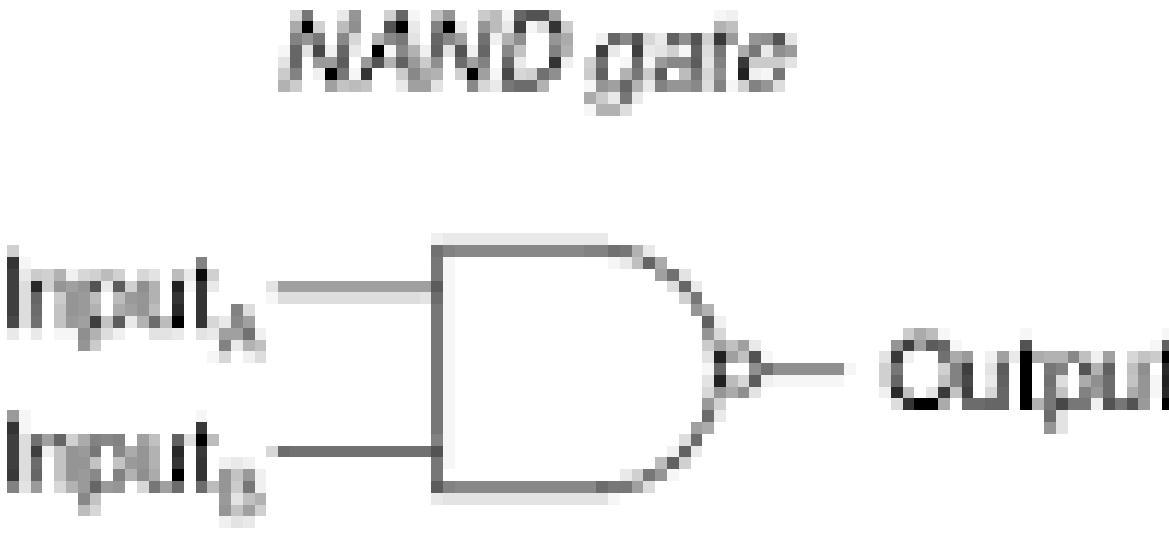
1 Universal Logic Gates

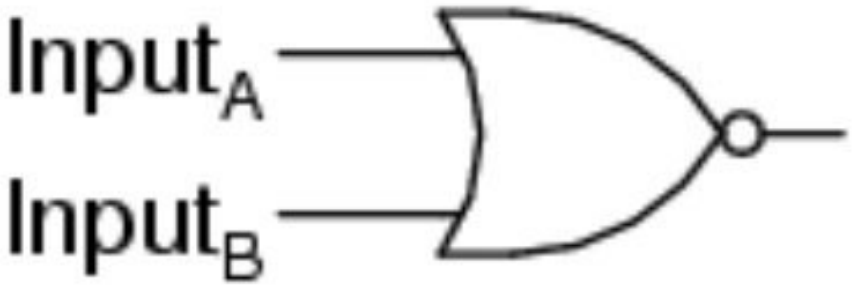
A "universal gate" in digital logic refers to a gate that can be used to implement any other type of gate, such as AND, OR, and NOT gates. Universal gates are versatile components in digital circuit design because you can use them to build more complex circuits without the need for multiple types of gates. There are two main universal gates: NAND and NOR gates. 3.

1



A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

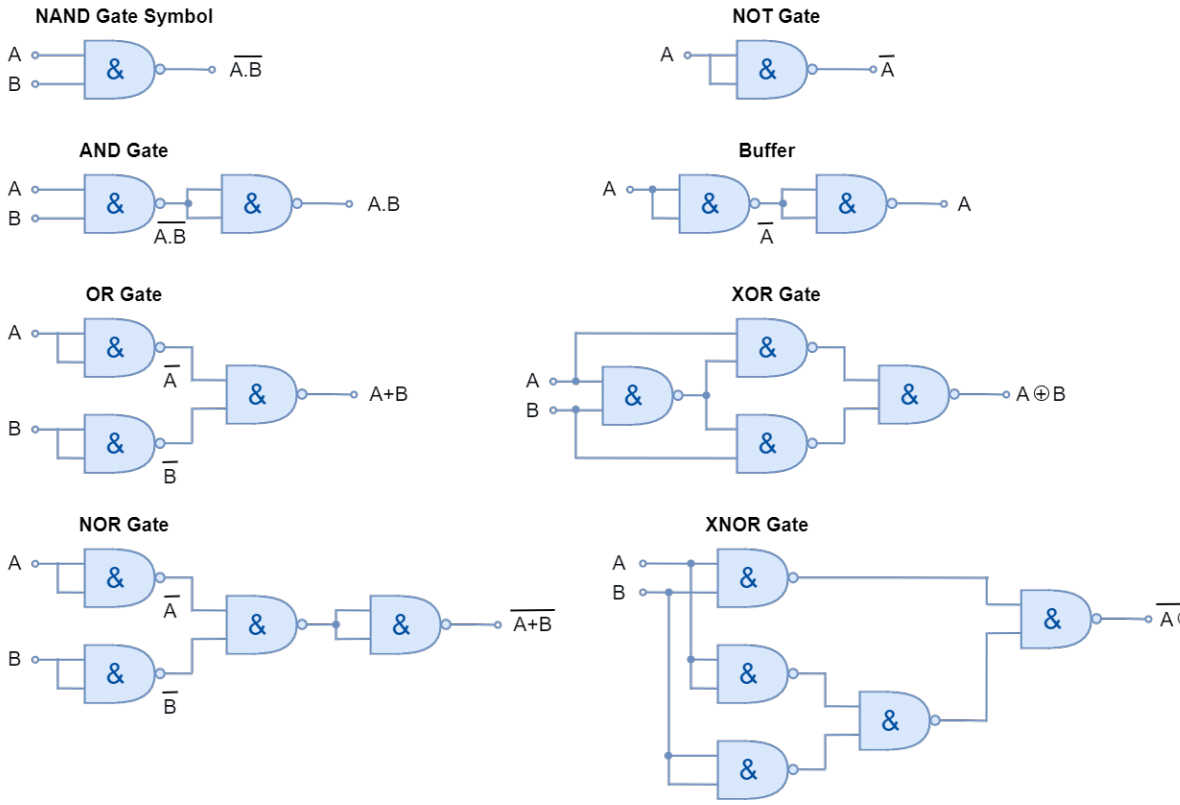
NOR gate



A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

3

Other logic gates using universal logic gate(NAND):



4

EXPERIMENT 3

2 Questions

A 7-segment display is a device with seven LEDs that can show numbers and some letters by lighting up specific segments.

There are two types: common cathode and common anode. Common cathode needs a positive voltage to turn on a segment, while common anode requires a negative voltage.

To use a 7-segment display, you need a decoder. It converts binary input into the right segments to display a digit. It simplifies the circuit and reduces the wires needed.

If you designed for a common anode display, the truth table would change. A 0 would mean the segment is on, and 1 would mean it's

off due to the opposite voltage requirement.

Using 'don't care' inputs (X) like 10-15 can result in random segment patterns. This happens because the decoder doesn't define the output for these inputs. To prevent this, use a decoder with an enable input to disable the output for invalid inputs.

3 Truth Table and Karnaugh Maps for each function

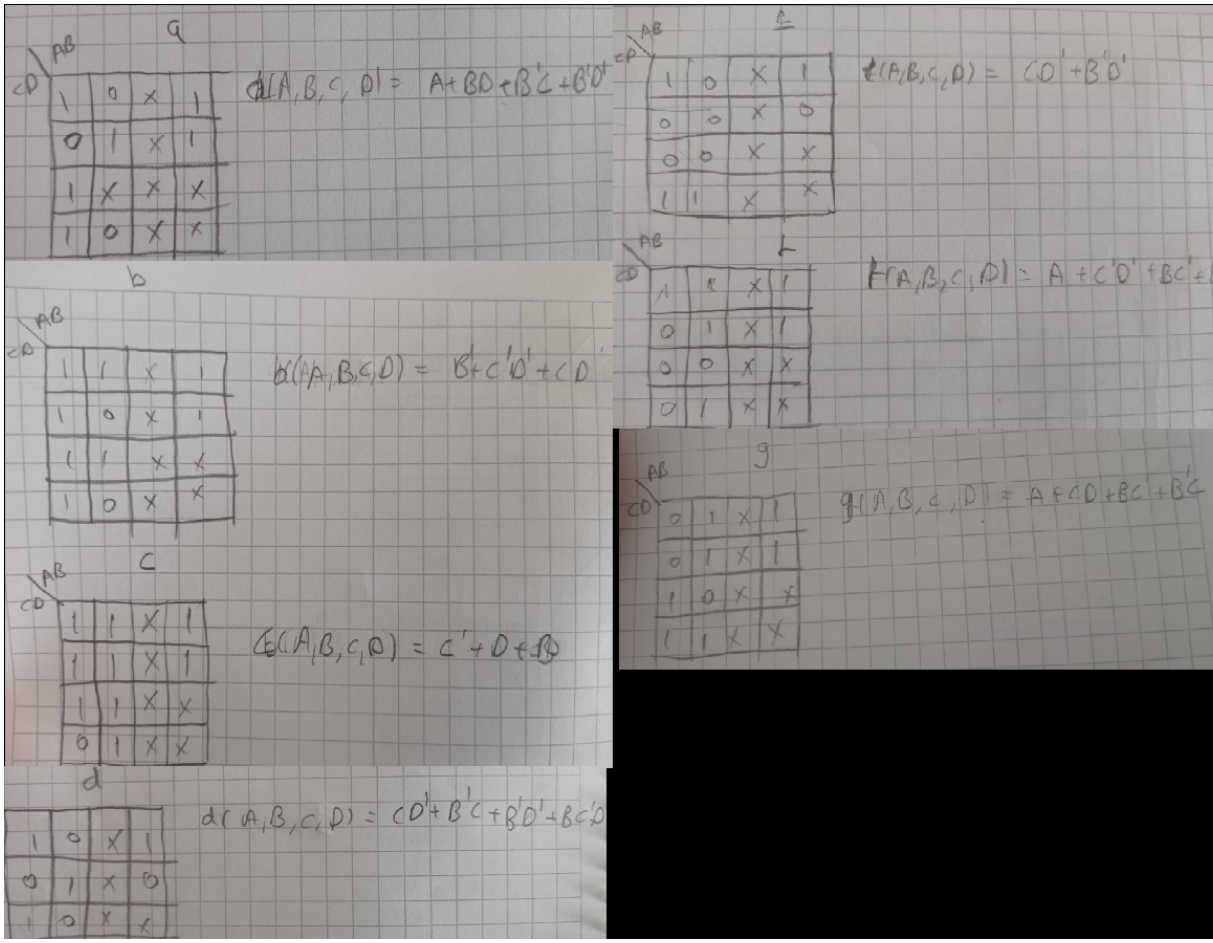
5

Valid output table:

Decimal Digit	Input lines				Output lines							Display pattern
	A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	
1	0	0	0	1	0	1	1	0	0	0	0	
2	0	0	1	0	1	1	0	1	1	0	1	
3	0	0	1	1	1	1	1	1	0	0	1	
4	0	1	0	0	0	1	1	0	0	1	1	
5	0	1	0	1	1	0	0	1	0	1	1	
6	0	1	1	0	0	0	1	1	1	1	1	
7	0	1	1	1	1	1	1	0	0	0	0	
8	1	0	0	0	1	1	1	1	1	1	1	
9	1	0	0	1	1	1	1	0	0	1	1	

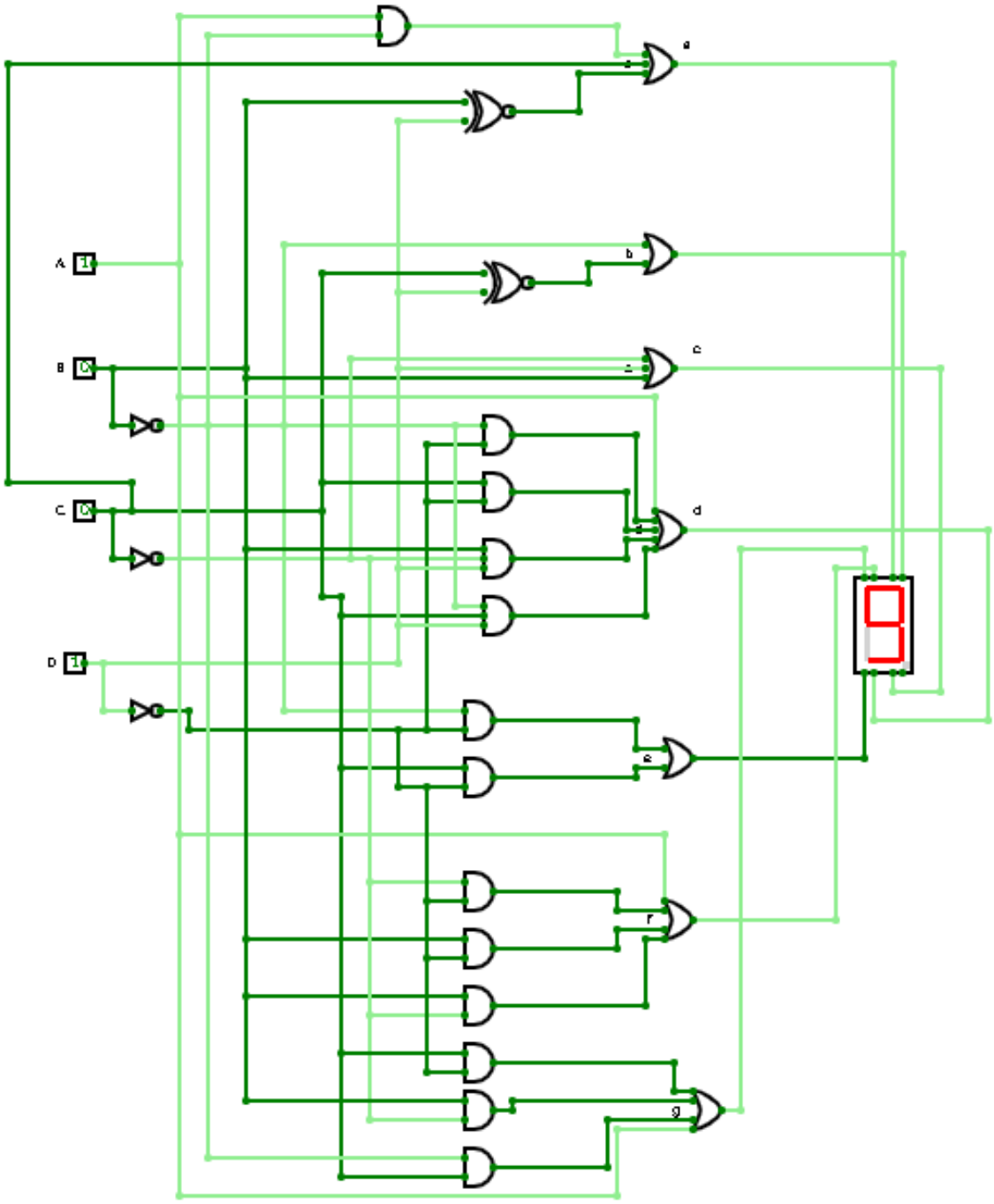
6

Karnaugh map:



7

Final Circuit:


A
1
B
0
C
0
D
1
a
b
c
d
e
f
g
9

8 NAND gate implemantation

$\mathrm{a} = \overline{A} \uparrow (A \uparrow B) \uparrow (\overline{B} \uparrow C) \uparrow (\overline{B} \uparrow \overline{D})$
$b = B \uparrow (C \uparrow D) \uparrow (\overline{C} \uparrow \overline{D})$
$c = \overline{B} \uparrow C \uparrow \overline{D}$
$d = (\overline{B} \uparrow D) \uparrow (C \uparrow \overline{D}) \uparrow (\overline{C} \uparrow D)$
$e = (\overline{B} \uparrow \overline{D}) \uparrow (C \uparrow \overline{D})$
$f = \overline{A} \uparrow (\overline{B} \uparrow D) \uparrow C$
$g = \overline{A} \uparrow (B \uparrow \overline{C}) \uparrow (\overline{B} \uparrow C) \uparrow (C \uparrow \overline{D})$
$9 NOR gate implemantation$

$\mathrm{a} = (\mathrm{A} \downarrow \overline{B} \downarrow \overline{C} \downarrow \overline{D}) \downarrow (A \downarrow B \downarrow C)$
$b = \overline{(\overline{B} \downarrow \overline{C} \downarrow D)} \downarrow (\overline{B} \downarrow C \downarrow \overline{D})$
$c = \overline{(B \downarrow \overline{C} \downarrow D)}$
$d = (A \downarrow \overline{B} \downarrow C) \downarrow (A \downarrow \overline{B} \downarrow \overline{D}) \downarrow (A \downarrow C \downarrow \overline{D})$
$e = (\overline{B} \downarrow C) \downarrow D$
$f = (A \downarrow \overline{B} \downarrow \overline{C}) \downarrow (A \downarrow \overline{C} \downarrow D)$
$g = (A \downarrow \overline{B} \downarrow \overline{C} \downarrow \overline{D}) \downarrow (A \downarrow B \downarrow C)$