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Digital System Design Capsule Project Task 1 Simulation Report

INTRODUCTION

A ring oscillator is a circuit that electronically generates a continuously oscillating signal. It consists of an odd number of inverting stages (e.g. CMOS inverters). Due to the phase shift, the feedback loop with an odd number of inverters produces a continuous oscillation.

The operating principle of the ring oscillator is resistance to the switching delay of the transistors. A transistor, at the instantaneous switching on of a signal at the gate terminal, has a certain freedom to charge and discharge due to their internal capacitance. This delay is caused by the gate-source (Cgs) and gate-drain (Cgd) capacitances. In particular, the gate-drain capacitance (Cgd) is one of the main factors affecting the switching region through the Miller effect and determining the oscillator frequency.

The operating principle of CMOS is as follows: When the input signal is low (0), the PMOS transistor becomes conductive and provides a path to VDD to make the output high (1). Conversely, when the input signal is high (1), the NMOS transistor becomes conductive and provides a path to ground to make the output low (0).

The advantages of using the CMOS configuration with the ring oscillator are that the frequency of the ring oscillator is easier to adjust and the CMOS configuration has less static current, meaning less energy loss in the design. The working principle of the ring oscillator is as follows: In a ring oscillator, there is an odd number of inverters (NOT gates) and there is a feedback at the end of the circuit that provides the oscillation. If there were an even number of inverters, the final output of the system would be the same as the initial input and no oscillation would occur.

DESIGN AND TEST PROCEDURES

For the first part of the project, a ring oscillator was created. For this, BS250 was used as PMOS and 2N7000 as NMOS. Using 7 of each of these transistors, a 7-stage ring oscillator was created. In addition to these transistors, 5.6 kΩ resistors and 10 µF capacitors were used.

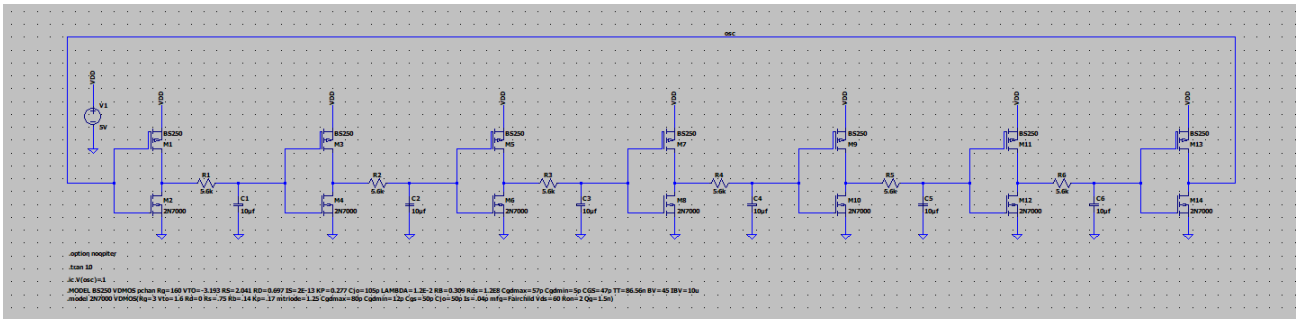

Figure 1 LTSpice diagram of 1 bit generator (A_1)

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$V(t) = V_{DD} \cdot e^{\frac{-t}{RC}} \rightarrow This\ formula\ represents\ the\ discharge\ process\ of\ a\ capacitor\ in\ RC\ circuits.$

$$\frac{V_{DD}}{2} = V_{DD} \cdot e^{\frac{-t_{1/2}}{RC}}$$

$t_{1/2} = R \cdot C \cdot \ln 2 \rightarrow This\ is\ the\ time\ it\ takes\ for\ the\ capacitor\ to\ reach\ half\ range.$

Total delay for each gate:

$t_{gate} = t_{rise} + t_{fall} = 2 \cdot R \cdot C \cdot \ln 2$

For N gate:

$N \cdot t_{gate} = 2 \cdot N \cdot R \cdot C \cdot \ln 2$

$$f = \frac{1}{2 \cdot \ln(2) \cdot N \cdot R \cdot C}$$

$f = frequency\ of\ oscillation$

$N = inverting\ gates$

$C = capasitance\ value$

$R = resistance\ value$

$$f = \frac{1}{2 \cdot \ln(2) \cdot 7 \cdot 5600 \cdot 10 \cdot 10^{-6}} = 1.84\ Hz$$

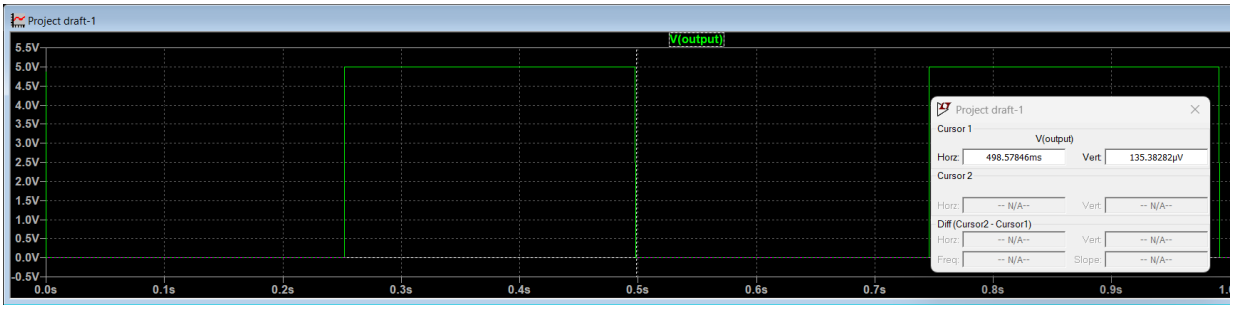

Figure 2 Period of designed circuit diagram in LTSpice

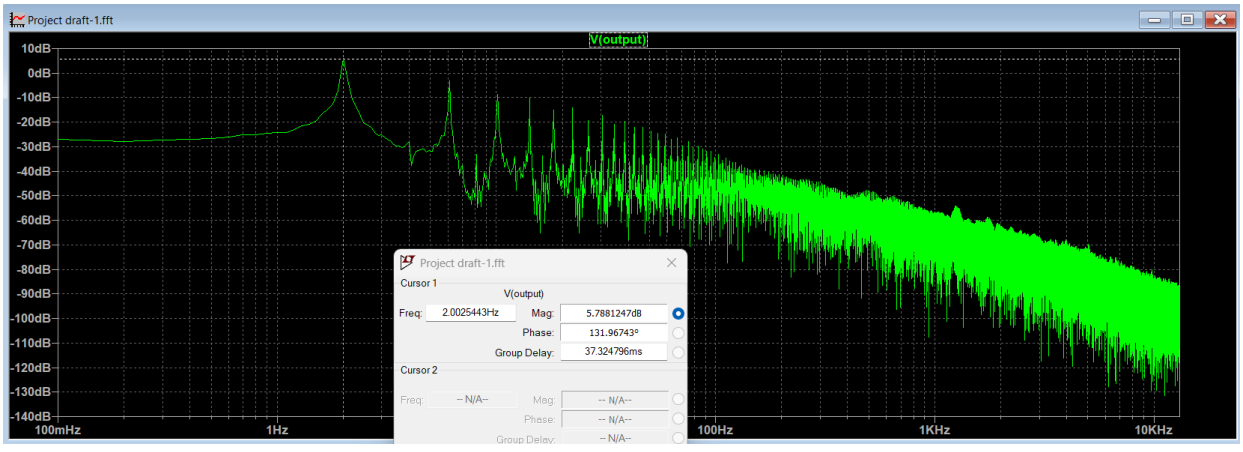

Figure 3 Frequency of designed circuit diagram in LTSpice

RESULT AND DISCUSSION

Table 1 Comparison of frequency values in simulation and calculation

	Hand Calculation	**LTSpice**
Frequency Values	1.84 Hz	2 Hz

Hand calculation and simulation values are close to each other. The reasons for the difference:

- Realistic parameters of MOSFETs cannot be included in the hand calculation part. Hand calculations often use idealized parameters (e.g., simplified RDS (on), gate capacitance).
- MOSFET on/off times and gate capacitances are ignored during hand calculation. These parameters are critical for simulation models.
- Non-ideal behaviours of MOSFETs (turn-on delay time(t_d(on)), turn-off delay time(t_d(off)), rise time(t_r), fall time(t_f)) may result from approximate modelling in the simulation.

CONCLUSION

A ring oscillator was designed as a 1-bit generator. The working principle of the designed ring oscillator was investigated, and its purpose was understood. The effects of the number of gates were analysed. It was observed that increasing the number of gates decreased the oscillation frequency but provided more stable operation by absorbing noise and parasitic signals. The circuit was simulated using LTSpice, and the role of each component was clarified. The following observations were made:

Resistors were used to control the oscillation frequency and limit excess current in MOSFET gates.

Capacitors influenced the oscillation frequency, suppressed high-frequency noise, and reduced signal overshoot/undershoot by smoothing edges.

Additionally, the process of adding a MOSFET library to the simulation software was learned. Frequency and period measurements were performed in the simulation. The minor discrepancy between the simulated frequency and the theoretical calculation was attributed to factors such as parasitic effects, component tolerances and non-ideal MOSFET behaviour.

References:

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4- Standard.mos - LTWiki-Wiki for LTSpice. (2013). https://ltwiki.org/index.php?title=Standard.mos