Switchable Counter & Variable Pulse Generator Task-3

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Introduction

This report presents the design and implementation of a digital system combining frequency-selectable square wave generation with a switchable binary counter. At the core of the system, a ring oscillator was initially designed to operate at frequencies of 1 Hz and 2 Hz. The two outputs from this oscillator were connected to a 2×2 CMOS multiplexer, allowing the user to select the desired frequency. The selected output signal (referred to as B1) was then connected to the clock input of a switchable 4-bit counter. The outputs of this counter were passed to a 7-segment decoder, and the decoder outputs were connected to a single-digit 7-segment LED display to show binary values in decimal form.

System Components

The system is composed of five main components:
• Two 1-bit square wave generators
(A0: 1 Hz, A1: 2 Hz)
• CMOS-based 2-by-2 multiplexer
• Synchronous BCD counter
(switchable: +1 or +2)
• Duty-cycle-variable pulse generator
(adjustable from 0% to 50%)
• Output units: 2-digit 7- segment display and 5 LEDs

Switchable BCD Counter

The counter was constructed using four JK flip-flops per digit to form a synchronous BCD counter. The flip-flop outputs were labelled A3 (MSB) through A0 (LSB), and these outputs were configured to generate a 4-bit binary number. Starting with the least significant bit, A0, representing the fundamental frequency, each higher digit (A1, A2, A3) was triggered at half the frequency of the previous one. With this structure, the combinations A3A2A1A0 were observed to proceed sequentially as 0000, 0001, 0010, ... 1001 (decimal 9). Since the counter only had to count from 0 to 9, the JK flip-flops were controlled using logic gates so that the counter would be reset when the value reached 1010 (decimal 10), allowing a continuous counting cycle. An additional counter was designed for the second display. However, the clock input of this second counter was not given directly by the ring oscillator or multiplexer. Instead, it was triggered by a signal generated through an AND gate when the output of the first counter reached 1010 (decimal 10). In this way, each time the first counter went from 9 to 0, the second counter was incremented by 1, causing the display to show values such as 10, 11, 12, etc. A control switch was also added that allowed the counter to operate in two modes: counting by 1s and 2s, depending on the user's choice. Different ways were tried to accomplish the 2 consecutive counting operation. The least important step was to combine the signal received from the 2nd flip-flops with a half adder or OR gate, but no correct result was found. This was because it was observed that the signal received from the 2nd flip-flops would make a logical maximum of 1, and no different result could be obtained from using a 1st flip-flop. Later, the excess 2 design was made like the excess 3 logic, but no valid result was found. As a result, the least significant step was counted by ones or twos by turning the Sc key on and off.

The operating logic of the JK flip flop used is as follows:

A JK flip-flop is a type of digital flip-flop with two inputs, J and K, a clock input, and two outputs, Q and Q'. The output depends on the values of J and K when the clock is at 1. Below is the truth table for a JK flip-flop:

J = 0, K = 0: No change in output.

J = 0, K = 1: Output Q is reset (Q = 0).

J = 1, K = 0: Output Q is set (Q = 1).

J = 1, K = 1: Output Q toggles (Q switches state).

A D flip-flop, on the other hand, has a single input D and a clock input. The output Q follows the input D when the clock pulse occurs.
When the clock is triggered, the output Q becomes equal to the input D. If D is 0, Q becomes 0, and if D is 1, Q becomes 1.

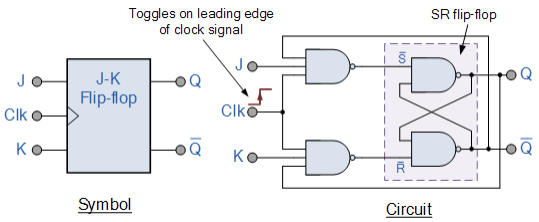

Figure 1 JK flip flop circuit visual and content.

The operating logic of the D flip flop used is as follows:

D flip-flop is a fundamental digital circuit used to store a single bit of binary information. It has one data input (D), a clock input, and two outputs, Q and Q'. The D flip-flop transfers the value at the D input to the Q output on the triggering edge of the clock signal. The output value remains constant until the next clock pulse.
The operation of a D flip-flop can be summarized as follows:
When the clock pulse occurs:

If the input D is 0, the output Q will be 0.

If the input D is 1, the output Q will be 1.

The D flip-flop is useful in memory storage applications, as it holds the input value steady at the Q output until the next clock pulse, making it ideal for data synchronization and timing control in sequential circuits.

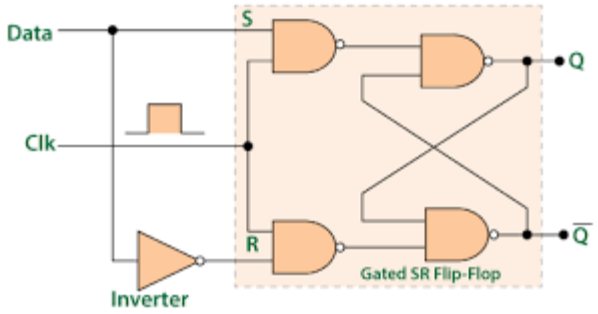

Figure 2 D flip flop circuit visual and content.

D3	D2	D1	D0	B0
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1

Figure 3 Truth table for a BCD counter, showing the states of D3, D2, D1, D0, and the B0 output.

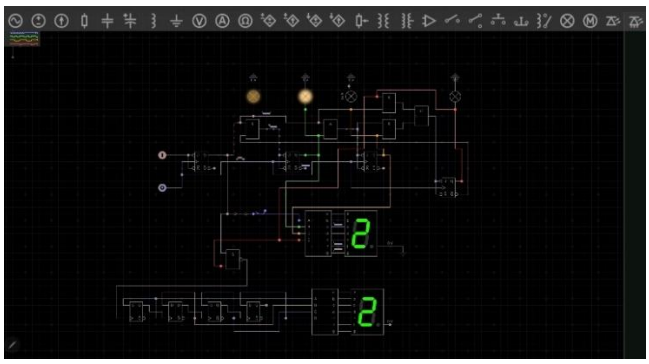

Figure 4 Circuit diagram of switchable BCD counter.

Duty-Cycle-Variable Pulse Generator

Duty cycle is defined as the ratio of the time the signal is high (active) over a given period of time to the total cycle time (i.e. the sum of the high and low times of the signal).

Here:

$$Duty\ Cycle = \frac{TON}{TON + TOFF}$$

$$Duty\ Cycle\ (\%) = \frac{TON}{TON + TOFF}\ X\ 100$$

Time On: The time the signal is high (5V).

Time Off: The time the signal is high (5V).

Total Time: The sum of the time on and time of (period).

The duty cycle in a circuit is not fixed but has an adjustable value. The main component that provides this adjustment is the potentiometer. The potentiometer allows you to control the resistance in the charging path of the capacitor. By adjusting the potentiometer, you affect the time the capacitor charges and discharges, thus changing the high and low times of the output signal. This directly changes the duty cycle.

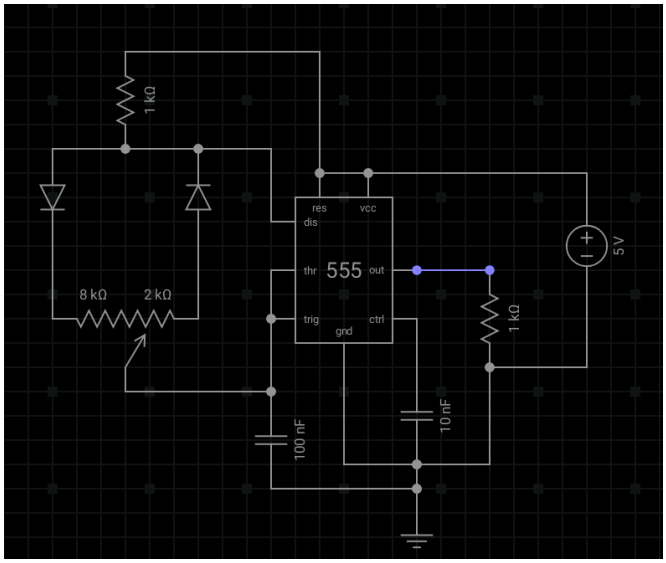

Figure 5 Adjustable duty cycle circuit diagram.

Simulation Results

The circuit was run via LTSpice simulation, but when reset was connected to the circuit with logic gates, the error time step too small and even though the logic gates could be run, reset could not be done. Only the count from 0 to 15 was taken from the LTSpice simulation. In the alternative circuit simulation, the circuit reset was done successfully, and in addition to this, the decoder and 7 segment 1 digit LED display added to the circuit resulted in a simulation that is exactly compatible with real life.

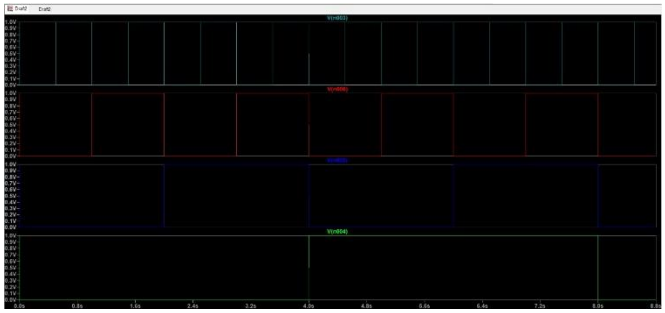

Figure 6 The output signal images of the circuit without the reset included in the LTSpice simulation.

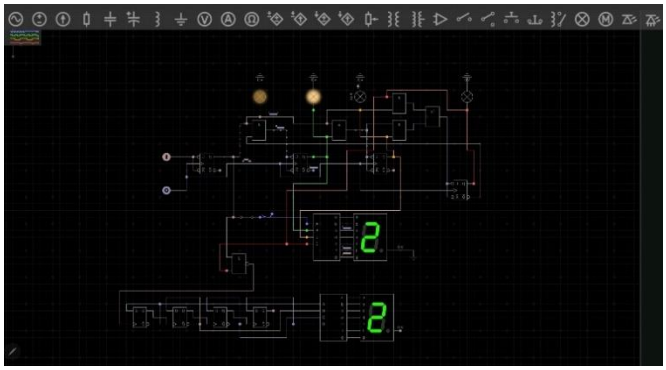

Figure 7 Circuit diagram in alternative circuit simulation.

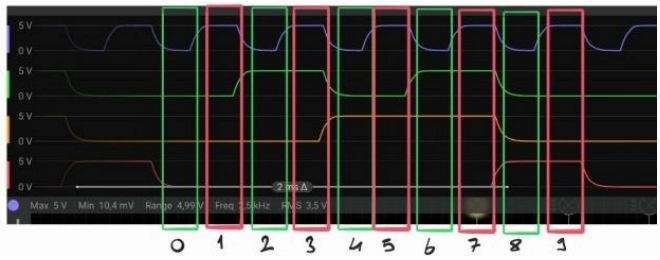

Figure 8 The operation of a switchable counter that counts from 1 to 9, incrementing by 1, and its graphical representation.

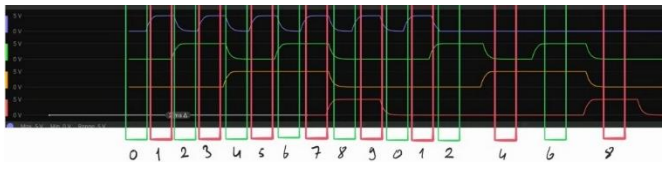

Figure 9 The operation of a switchable counter that counts from 1 to 9, incrementing by 2, and its graphical representation.

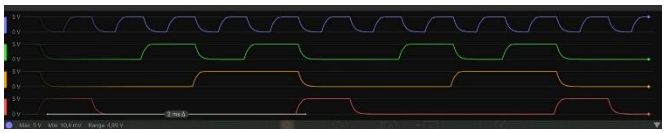

Figure 10 The states of the outputs in the graph.

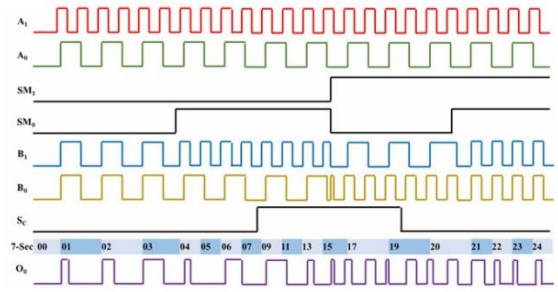

Figure 11 Timing diagram showing 2 Hz ring oscillator output A1 and 1 Hz ring oscillator output A0. Based on these signals, selection signals SM1 and SM2 control a 2x2 multiplexer with outputs B1 and B2. The SC signal represents the active period of a counter that increments by 2. The 7-segment counter operation from 0 to 24 is plotted on the time axis. The O0 signal represents the output duty cycle.

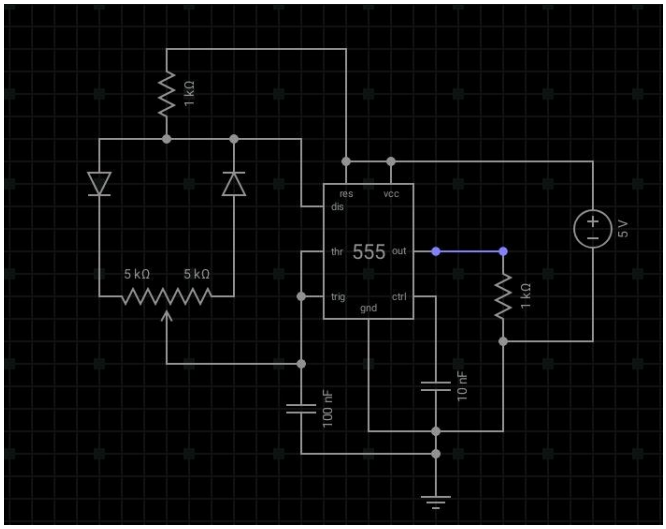

Figure 12 Adjustable duty cycle circuit diagram.

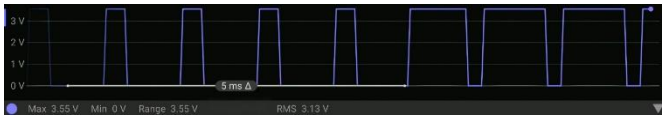

Figure 13 Graphical display and response of adjustable duty cycle circuit.

The figure 11 given above is in the project task given to us. The simulation results were compared with the values in this graph and it was observed that they were the same. As a result, it was concluded that the circuit worked correctly.

The online simulated video of the circuit is in the link below:
https://youtu.be/IeM8DrGkxiU?si=mjXi2CzFAM30sUeK

Discussion

During the development of a switchable counter, several problems were encountered, which are outlined as follows:

The first issue occurred when simulating the circuit derived from the Boolean algebra in LTSpice. Although the circuit worked initially, errors were generated with the AND and OR gates added for the reset function, specifically the "time is too small" error. We identified that the rise and fall times of the D flip-flop and JK flip-flops, already part of the circuit, had not been entered. As a result, there was a time mismatch between the flip-flops and the logic gates. This was corrected by entering the rise and fall time values for the D flip-flops, which had been obtained through further research. This issue emphasized the importance of time synchronization in circuits.

The second problem arose from the reset circuits for the flip-flops, which were faulty due to the absence of a reset input in the alternative simulation used. It was discovered that the solution was to reset the JK flip-flops using different combinations of the J and K inputs, even without a dedicated reset input. This experience provided insight into how JK flip-flops operate and where they can be applied.

Through this experiment, several key lessons were learned:

- Single and double counting can be achieved using flip-flops, and the desired counting behavior can be obtained by first deriving the Boolean algebra using Karnaugh maps (K-map), applying it to the circuit, and achieving the desired result.
- The duty cycle of the signal can be adjusted in the circuit using a timer and potentiometer and understanding when to use them is important.
- The function of the decoder circuit element in the system was clarified, demonstrating that different outputs can be obtained by using different combinations of decoders.
- An error revealed that only double counting occurs when the least significant bit (LSB) port of the decoder input is disconnected.
- It became clear that the counter circuit can either stop at a desired number or operate at the desired interval by using different combinations of the next stage tables and logic gates.
- The importance of the input signal for the second 7-segment display (tens digit) in the circuit was understood.

This experiment highlighted the significance of logic gates in circuits, the various circuits that can be formed using flip-flops and their combinations, and the diverse applications of these components. The experiment has provided valuable insights in a clear and understandable way for second-year engineering students.

Conclusion

This project successfully demonstrates the design and implementation of a gate-level digital system that integrates a switchable BCD counter and a duty-cycle variable pulse generator. The system is built using basic components such as flip-flops, logic gates, and a 2x2 CMOS multiplexer. The switchable BCD counter operates effectively by allowing increments of 1 or 2, and the pulse generator generates pulses with a duty cycle that can be adjusted from 0% to 50%.

The simulation results validated the design by verifying that the system performs as expected, with the BCD counter outputting accurate values and the pulse generator responding to changes in resistance values.

The project achieved its objectives of using basic gates and flip-flops to create a functional and reliable counter and pulse generator.

References:

1- Varghese, G. (2005). Network Implementation Models. In Elsevier eBooks (pp. 16–49). https://doi.org/10.1016/b978-012088477-3/50003-5

2- Brehl, D., & Dow, T. (2007). Review of vibration-assisted machining. Precision Engineering, 32(3), 153–172. https://doi.org/10.1016/j.precisioneng.2007.08.003