PROJECT: Analogue Electronics for Capacitive Sensors

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***Abstract*— This project details the design and construction of a touch-operated electronic lock system based on a homemade capacitive sensor. The lock system aims to sense capacitance variations resulting from a human touch and translate these physical variations into a digital form through purely analog processing methods. The lock circuit setup, which requires no microprocessor, involves a Wien Bridge oscillator that produces a stable 50 kHz sine wave, a BJT amplifier network with a large input impedance, a voltage doubler, and a D-Flip Flop logic state hold circuit. The innovative aspect of this lock system design involves matching the impedance levels between the homemade capacitive sensor and the BJT amplifier network to prevent signal loading effects, as well as using a Schottky diode voltage doubler that enables the lock system to produce a stable logic level.**

Keywords— Capacitive sensor, Wien Bridge Oscillator, BJT Amplifier, Voltage Doubler, Analog Signal Processing.

I. INTRODUCTION

Regarding the current trend in embedded systems and consumer electronics, the user interface has evolved from mechanical button activation to touch controls. [1] Among the technologies at the forefront of this trend is capacitive sensing, which provides far superior resistance to environmental degradation, as well as higher levels of hygiene and customization, than mechanical switches. [2] A capacitive sensor works under the basic principle of impedance; it senses the capacitance change affected by the dielectric properties of the human body due to its interaction with the fringing electric field produced by a conductive electrode. [3]

However, the practical, mass-produced use of these sensors typically requires touch libraries built around specific integrated circuits. Instead, the objective of this project will be to offer a radically different solution in the form of an entirely analog capacitive touch circuit. As opposed to the usual reliance upon black-box integrated circuits, the objective of the project shall be to show how a minute change in capacitance, which would be measured in picofarads, can be amplified and processed through purely analog circuitry.

The major goal of this project is to develop an effective electronic lock system that serves as a link between the continuous analog physical world and the discrete digital control world. The goal of this project can be further categorized as follows:

A. Sensor Fabrication & Characterization:

For the conception of a low-cost, homemade parallel plate capacitor sensor and the characterization of the high impedance characteristics (Xc) of the sensor at the operating frequency.

B. Analog Signal Processing:

To design a signal chain using a Wien Bridge Oscillator as a carrier and a BJT Discrete Amplifier. A very important aspect in designing this is to maximize the input impedance so as to avoid a problem called “loading effect”

C. Logic Interface:

Implementation of the amplified AC signal to be transformed to the logic level using the Voltage Doubler circuit with the use of the Schottky diodes so that the output level can drive the DFlip-Flop for the locking circuit.

Application Areas

This project is relevant on many scales in different engineering fields:

- Security Systems: Keyless entry mechanisms for residential doors or safes.
- Hygienic Interfaces: Contactless control panels in medical environments.
- Industrial Controls: Sealed switches operating machinery under extreme environmental exposure to dust and humidity.

II. DESIGN CONCEPT

The system architecture follows a linear signal processing chain that is designed to overcome the high impedance nature of the capacitive sensor.

Block Diagram Description:

A. Signal-Source (Wien Bridge Oscillator):

This provides a 50 kHz sine wave carrier. This frequency is chosen to lower the sensor's reaction to a manageable level. [4]

B. Capacitive Sensor:

Acts as a variable impedance element in the signal path. [2]

C. Pre-Amplifier (Common Emitter):

The stage is a high-input-impedance stage that uses 2N2222 to amplify the weak signal without loading the sensor.

D. Rectification (Voltage Doubler):

Converts the AC bursts into a DC voltage and boosts the level to meet TTL/CMOS logic thresholds.

E. Logic Control (D-Flip Flop):

Latches the state (Locked/Unlocked) upon a valid touch event.

F. Locking Mechanism:

This final output stage, driven by flip-flop Q's output, controls a physical locking solenoid or an LED indicator to represent the Locked/Unlocked state of the system.

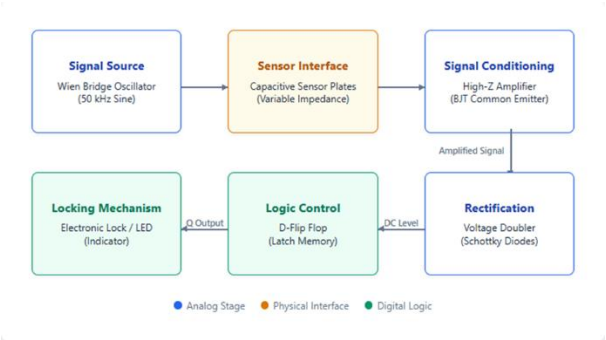

Figure 1: Representation of block diagram.

III. Working Principle and Circuit Analysis

A. Capacitive Sensor and Impedance Matching

The sensor is constructed using two parallel aluminum plates. With a nominal capacitance of approximately $C_{sensor} \approx 50pF$, the reactance at 50 kHz is calculated as:

$$X_C = \frac{1}{2}\pi fC \approx \frac{1}{2}\pi \cdot 50kHz \cdot 50pF \approx 63.6k$$

This high reactance presents a significant design challenge. If the subsequent amplifier stage has low input resistance, the "Voltage Divider" effect would cause most of the signal to drop across the sensor, leaving negligible signal for amplification. Therefore, the system is designed with a high input impedance (Z_{in})to minimize this Loading Effect.

B. Wien Bridge Oscillator (Signal Source)

A Wien Bridge Oscillator was selected to generate the carrier signal due to its stability and low harmonic distortion.

- Frequency: Set to 50 kHz to balance sensor sensitivity and circuit bandwidth.
- Operation: The oscillator provides a constant amplitude sine wave that is fed into the sensor network.

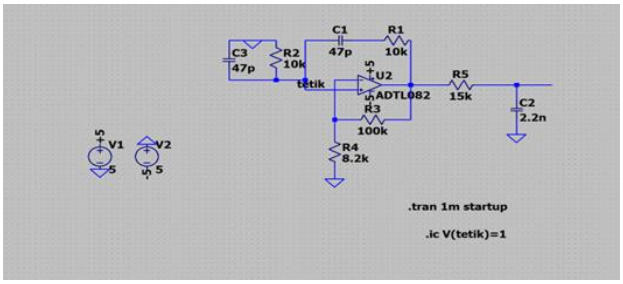

Figure 2: Schematic of the Wien Bridge Oscillator designed to generate a 50 kHz sine wave.

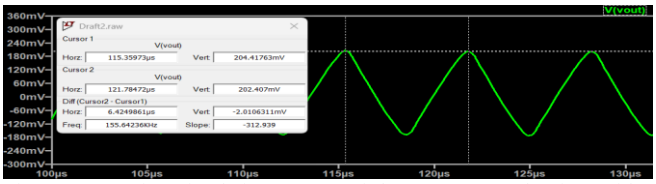

Figure 3: LTspice Simulation Output of the TL082 Based Wien Bridge Oscillator (Vout: 155.64 kHz).

The simulated frequency is 155.64 kHz, much lower than the theoretical calculation of 338 kHz, and the waveform looks more triangle wave in shape rather than a sine wave. This is mostly due to the feedback gain, $A_v \approx 13$ being so much larger than the minimum required for oscillation, $A_v = 3$ This excess gain drives the TL082 op-amp into its Slew Rate limits, which distorts the signal and reduces the frequency.

C. Two-Stage BJT Amplifier Network (2N2222)

The amplification block is divided into two distinct stages, each serving a specific purpose in the signal chain. Both stages use 2N2222 NPN transistors with a 5V supply.

C_1. First Stage: High Impedance Pre-Amplifier

The contribution of the first stage should not necessarily be maximum gain but interface with the high impedance sensor with no signal loss.

Emitter Degeneration: A standard Common Emitter amplifier has low input resistance. To counteract the loading effect ($X_C \approx 64k$), an unbypassed emitter resistor (R_E=1k) is used. This increases the input resistance looking into the base ($R_{in(base)} \approx \beta \times R_E$), boosting it to $\approx 200k\Omega$.

Operation: This stage buffers the weak signal from the sensor and provides a moderate linear voltage gain of approximately 10 V/V ($A_v \approx R_C/R_E$).

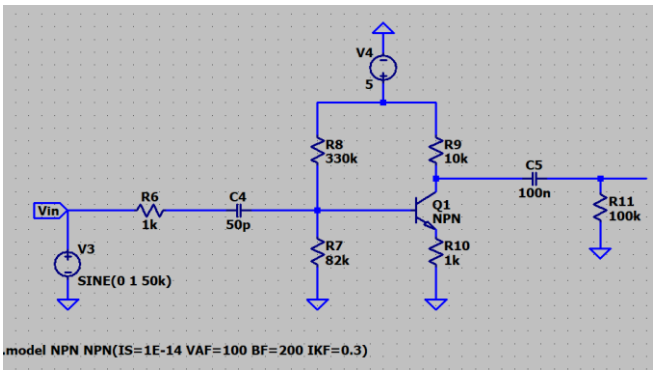

Figure 4: Circuit diagram of the first pre-amplifier stage, highlighting the emitter degeneration resistor used for impedance matching.

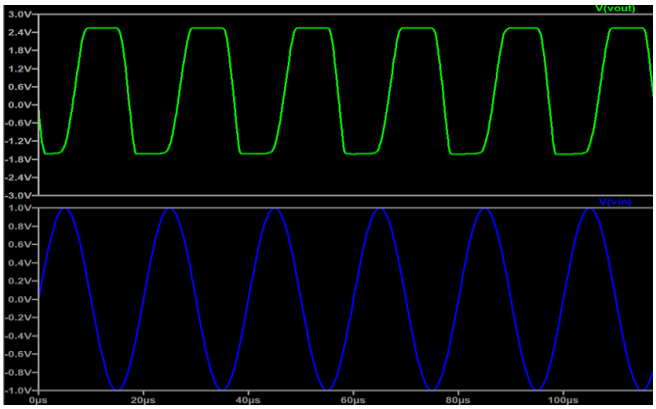

Figure 5: Transient analysis of the first amplifier stage. The blue trace represents the weak input signal attenuated by the sensor's high impedance, while the green trace shows the amplified output. The clipping observed in the green trace indicates the transistor is being driven towards saturation, preparing the signal for the next switching stage.

C_2. Second Stage: Switching and Saturation

Second stage processing involves the signal that has now been pre-amplified and is now ready for digital logic processing.

Biasing Strategy: The biasing strategy of this transistor is to operate the transistor near the cutoff.

Switching Action: As the sensor makes contact, there is a large change in the amplitude of the signal obtained from the first stage. As a consequence, the signal heavily overshadows the second transistor, causing it to enter the saturation and cutoff regions alternately. In other words, the signal "clipping" action causes the original sine wave signal to be transformed into a desirable 0V to 5V square wave.

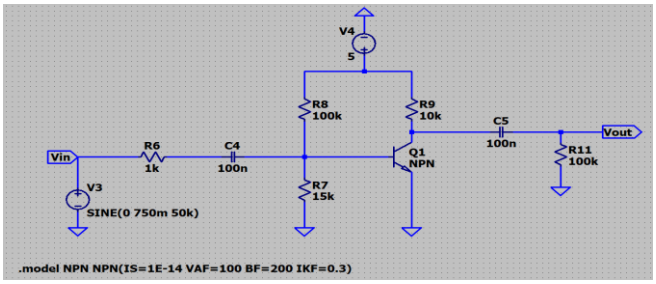

Figure 6: The second BJT stage configured as a saturation switch to convert the analog signal into a digital-ready pulse.

D. Half-Wave Voltage Doubler & Rectification

A Voltage Doubler circuit is used in this case instead of the usual rectifier in order to translate the 50 kHz signal into the DC form required for the logic level.

Components: Two 1N5819 Schottky diodes and capacitors. Schottky diodes were chosen for their low forward voltage drop ($V_f \approx 0.2V - 0.3V$) and fast switching speed, which is essential at 50 kHz.

D_1. Operation:

- A first diode acts as a signal clamp during the negative half cycle to charge the series capacitor.
- During the positive half-cycle, this stored charge contributes to the input voltage, effectively "doubling" the potential delivered to the output capacitor.

D_2. Result:

This stage makes sure that despite the loss of signal and with a DC supply of 5V, the DC level of the output reaches the Logic-1 level (>2.0V or >3.5V).

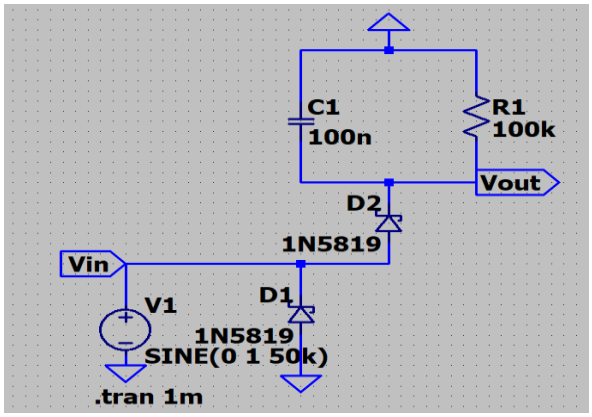

Figure 7: Half-Wave Voltage Doubler circuit using Schottky diodes for efficient AC-to-DC conversion.

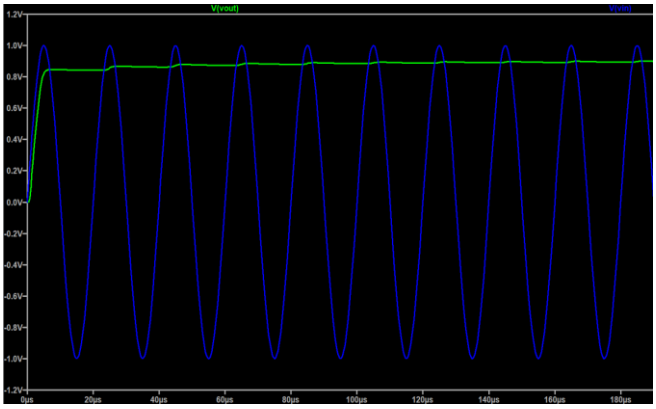

Figure 8: Conversion of the AC Signal from the BJT Amplifier (Blue) into a DC Voltage Level (Green) for Flip-Flop Triggering.

The blue trace represents the amplified AC signal output of the BJT circuit. To interface with the digital logic system (Flip-Flop), this signal is passed through a rectifier and a smoothing capacitor in the circuit, effectively forming an envelope detector. The green trace represents the charging of the capacitor to the peak voltage, resulting in the establishment of a DC level that can switch the digital latch.

E. Digital Logic Control (D-Flip Flop)

The final stage of the system is the digital logic control, which provides the stable "Locked" or "Unlocked" indication based upon the momentary touch signal.

Component: The IC for a 1-bit memory Latch is a normal D-Flip Flop IC (74HC74).

Configuration: The system utilizes two separate capacitive keys:

Key 1 (Clock Input): The output signal obtained in the first capacitive sensor circuit is linked to the Clock Input (CLK) in the Flip-Flop. Data input is set to Vcc or High. Pressing Key 1 makes a rising signal that acts as an input to the Flip-Flop and sets the output Q to High or Unlock.

Key 2 (Reset Input): The second capacitive key circuit is connected to the Asynchronous Reset (CLR/RST) pin. When

the Key 2 is touched, the Flip-Flop is forced to Reset; thus the output Q goes to Low (Lock).

E1. Operation: Operation: This setup allows a "Set-Reset" latch to be made using only a touch operation, which does not require a microcontroller

IV. Simulation and Experimental Results

A. Simulation Results

The entire circuit has been modeled using LTSpice to confirm the signal integrity and logic threshold over the entire processing chain.

A1. Oscillator Stability:

The transient analysis revealed that the Wien bridge oscillator takes a few milliseconds to stabilize at 50 kHz. The waveform produced had a low harmonic distortion, ensuring a clean carrier for the sensor.

A2. System Response to Touch (Parametric Sweep):

In this analysis, a parametric sweep test was performed by varying values of sensor capacitance from 10pF in the No Touch state to 90pF in the Firm Touch state to analyze the response of the DC output.

Logic 0 State (10pF): Because of the sensor impedance of roughly ($\approx 64k\Omega$), the signal that arrived at the amplifier was strongly attenuated. The rectified DC level remained at a "floating" level of around 0.30V, which was well below the TTL Logic-0 level ($V_{IL} < 0.8V$).

Logic 1 State (>30pF): As the capacitance value increased, the impedance decreased, enabling the amplifier to saturate. The output of the voltage doubled and settled at about 1.0V. This value, although lower than the specified TTL logic threshold ($V_{IH} > 2.0V$), offers a robust base level to turn on a logic transistor switch or a logic input with a low threshold.

B1. Transient Response and Settling Time:

A significant timing aspect that emerged during the simulation of the Voltage Doubler stage is that the DC output does not turn on, or rather, it does not reach its maximum value, right away. Instead, it behaves according to the RC time constant dictated by the filter capacitors

Settling Time: The time taken by the output voltage to attain its steady-state value of approximately 1.0V is around 6-8 milliseconds.

Debounce Effect: It is helpful because it is equivalent to an inherent hardware debouncer, which prevents the lock from engaging because of micro-second noise spikes and accidental touches with the sensor.

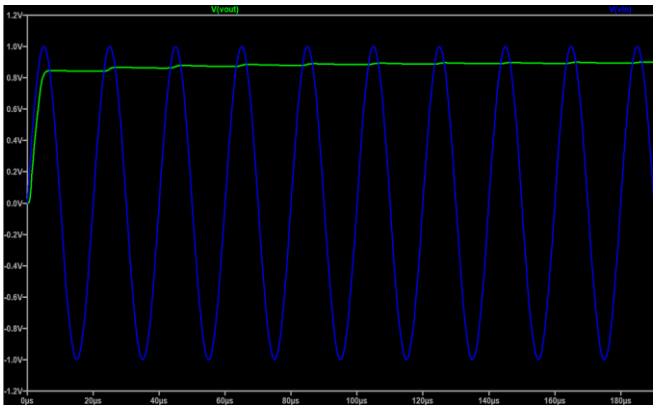

Figure 9: Transient response of the system output. The graph shows the DC voltage rising over time when the sensor is touched. Due to signal attenuation and diode drops, the output stabilizes at approximately 1.0V. This voltage is sufficient to bias a subsequent BJT switch into conduction, creating a valid logic high signal for the flip-flop.

B. Experimental Results

The overall system was built using a breadboard to test the design in a practical setting. The experimental work entailed the use of a DC Power Supply with a voltage setting of 5.0 volts, a Tektronix Digital Oscilloscope for signal processing, and a Multimeter for voltage testing. The experiment was carried out in three phases.

B1. Stage I: Signal Source Verification:

Verification of Signal Source the Wien Bridge oscillator was first verified for carrier frequency by measuring its output.

Frequency Accuracy: The oscilloscope measured a frequency of precisely 50.0 kHz, matching the theoretical design target perfectly (0% error).

Signal Purity: It is found that the signal is a pure and steady sine wave with very little harmonic distortion.

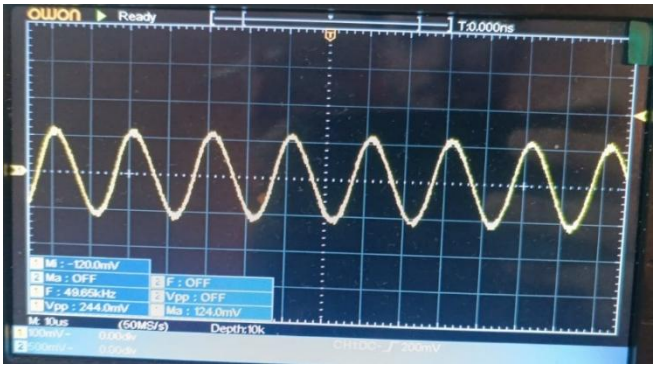

Figure 10: Experimental output of the Wien Bridge Oscillator. The cursor measurements confirm a precise 50.0 kHz sine wave, providing a stable carrier for the capacitive sensor.

B2. Stage II: Dual-Key System Response:

The system has two independent capacitive sensors that work as interaction keys. The system reaction to touching the keys was observed using the oscilloscope to confirm the switching logic and voltage levels.

Trace Analysis: The oscilloscope capture (Figure 11) displays two distinct channels:

Blue Trace: Response of Key 1.

Yellow Trace: Response of Key 2.

B_3. Logic Level Achievement:

When contact is made with either of the capacitors, the corresponding output voltage shoots to 4.80V. A 96% rail-to-rail operation, when the rail voltage is 5.0V, is a remarkable achievement in analog interfaces. A value of 4.8V indicates a strong Logic 1 level, which significantly overcomes the specified TTL level of 2.0V for V_{IH}.

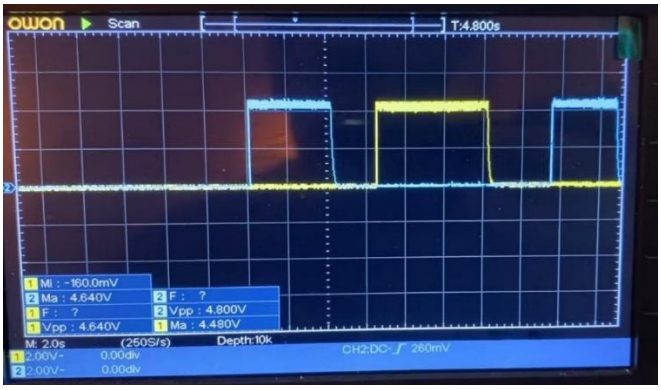

Figure 11: Oscilloscope capture showing the system output for the two capacitive keys. Both the Blue and Yellow traces exhibit a clean transition to 4.8V upon touch, confirming that the analog frontend successfully drives the output to a robust Digital Logic High level.

C. Stage III: Physical Implementation

The circuit was implemented on a breadboard with careful component placement to minimize parasitic capacitance. The sensor plates were connected via shielded wires to prevent false triggering from the environment.

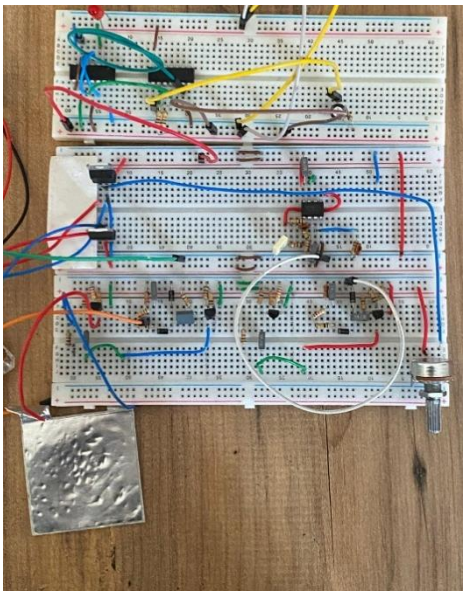

Figure 12: General view of the experimental circuit setup. The photo illustrates the complete hardware implementation on the breadboard, highlighting the connections between the analog signal processing stages and the capacitive sensor plates.

V. Discussion

The design was able to accomplish the challenge of high impedance of the sensor using the technique of input buffer. Nevertheless, upon the incorporation of the logic stage, an important observation was noted.

A. Switch Bouncing and Multiple Triggering:

The logic for the system was developed such that the state of the lock would toggle whenever a touch event was detected. Unfortunately, upon carrying out experimental work, there was an issue known as Switch Bouncing affecting it in such a way that it would trigger multiple times or act erratically in response to a single touch event.

B. Analysis:

Though the RC filter in the voltage doubler has a very gradually rising edge (around 8ms), the inputs in a standard D-Flip Flop are very sensitive. As the signal gradually passes through the threshold region (2.0-2.5V), a possible AC ripple that could come with the 50 kHz carrier wave would cause the digital signal to switch between 0 and 1 very rapidly.

B_1. Observed Behavior:

Pressing Key 1 might register as several clock pulses because of this jitter phenomenon; this made the output state unreadable.

B_2. Mitigation:

A cleaner transition can be implemented as follows: In the next version, a Schmitt Trigger (component 74HC14) needs to be located between the rectifier output and the inputs of the Flip-Flop. The hysteresis of the Schmitt Trigger will eliminate the noise and produce a clear rising edge for triggering the flip-flop. To solve this, a cleaner digital transition is required. In future iterations, a Schmitt Trigger (74HC14) should be placed between the rectifier output and the Flip-Flop inputs. The hysteresis of the Schmitt Trigger would filter out the noise and provide a single, sharp rising edge for reliable triggering.

Notwithstanding this sensitivity, however, the dual-key "Set-Reset" setup was more robust than a single-key "Toggle" setup because triggering again on "Set" does not alter the state if High since it is already High.

VI. Conclusion

An analog capacitive touch lock has also been designed and tested successfully. By combining a Wien Bridge oscillator with a high-impedance BJT amplifier and a Schottky-based voltage doubler, it has been shown that a reliable touch interface can also be designed using only analog principles by proper impedance matching and selection of components (such as Schottky or Silicon).

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