Switchable Counter & Variable Pulse Generator Task-2

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The purpose of this report is to make a simple 2 by 2 multiplexer using CMOS configuration and depending on the input signals from the circuits.

A Multiplexer (MUX) is a combinational logic circuit that selects one of multiple input signals and directs it to the output. MUX circuits are typically used for data selection and routing operations. The selection process is controlled by selection inputs. There are various types of MUX circuits, ranging from small ones like 2x2 MUX to larger ones such as 8x1 and 16x1. Multiplexer circuits are widely used in many electronic systems for data selection and routing purposes.

For example, for a 2x2 MUX:

- 2-bit selection inputs (S_{M0} and S_{M1}) are used.
- There are 2-bit inputs (A_0 (2 Hz) and A_1 (A Hz)).
- 2-bit outputs (B_0 and B_1) are obtained.
- The output takes the input value determined by the selection inputs.

A1 and A0 signals produce a square wave because of the 7-gate ring oscillator design.

$$V(t) = V_{DD} \cdot e^{\frac{-t}{RC}} \rightarrow \textit{This formula represents the discharge process of a capacitor in RC circuits.}$$

$$\frac{V_{DD}}{2} = V_{DD} \cdot e^{\frac{-t_{1/2}}{RC}}$$

$$t_{1/2} = R \cdot C \cdot \ln 2 \rightarrow \textit{This is the time it takes for the capacitor to reach half range.}$$

Total delay for each gate:

$$t_{gate} = t_{rise} + t_{fall} = 2 \cdot R \cdot C \cdot \ln 2$$

For N gate:

$$N \cdot t_{gate} = 2 \cdot N \cdot R \cdot C \cdot \ln 2$$

$$f = \frac{1}{2 \cdot \ln(2) \cdot N \cdot R \cdot C}$$

f = *frequency of oscillation*
N = *inverting gates*
C = *capasitance value*
R = *resistance value*

The ring oscillator frequency calculation is made according to the given formula.
For the A_1 signal to be 2 Hz, the resistance value was selected as 5.6 kΩ and the capacitor value was selected as 10 µF.
For the A_0 signal to be 1 Hz, the resistance value was selected as 11k kΩ and the capacitor value was selected as 10 µF.
The selected resistor and capacitor values were decided because they were easily obtainable.

Selection inputs		Outputs	
S_{M1}	S_{M0}	B_1	B_0
0	0	A_0	A_0
0	1	A_1	A_0
1	0	A_0	A_1
1	1	A_1	A_1

Figure 1 Inputs (A_1 and A_0) are distributed to the outputs (B_1 and B_0) according to selection inputs.

In this table, the selection inputs S_{M0} and S_{M1} determine which input value is transferred to the output.

$S_{M0} = 0$ and $S_{M1} = 0 \rightarrow B_0 = A_0$ and $B_1 = A_0$
Both output bits take the value of A_0.

$S_{M0} = 1$ and $S_{M1} = 0 \rightarrow B_0 = A_0$ and $B_1 = A_1$
B_1 takes A_1 while B_0 takes A_0.

$S_{M0} = 0$ and $S_{M1} = 1 \rightarrow B_0 = A_1$ and $B_1 = A_0$
B_1 takes A_0 while B_0 takes $A_0$1.

$S_{M0} = 1$ and $S_{M1} = 1 \rightarrow B_0 = A_1$ and $B_1 = A_1$
Both output bits take the value of A_1.

Boolean Equation for B_1:

Selection Input		Outputs	
SM1	SM0	A0	A1
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Figure 2 Truth table for output B_1.

$S_{M0} = 0$ and $S_{M1} = 0 \rightarrow B_1$ takes the value of A_0.

$S_{M0} = 1$ and $S_{M1} = 0 \rightarrow B_1$ takes the value of A_1.

$S_{M0} = 0$ and $S_{M1} = 1 \rightarrow B_1$ takes the value of A_0.

$S_{M0} = 1$ and $S_{M1} = 1 \rightarrow B_1$ takes the value of A_1.

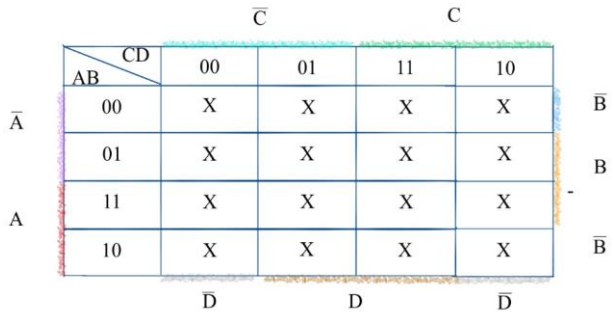

Figure 3 Karnaugh Map is grouped as shown to obtain Boolean equations.

S1S0 / A0A1	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	1	1	1
10	1	0	0	1

$B1=A1S0+\overline{S0}A0$

Figure 4 Karnaugh Map created for output B_1 and expression of output B_1 with Boolean equation.

Boolean Equation for B_0:

Selection Input		Outputs	
SM1	SM0	A0	A1
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

Figure 5 Truth table for output B_0.

$S_{M0} = 0$ and $S_{M1} = 0 \rightarrow B_0$ takes the value of A_0.

$S_{M0} = 1$ and $S_{M1} = 0 \rightarrow B_0$ takes the value of A_0.

$S_{M0} = 0$ and $S_{M1} = 1 \rightarrow B_0$ takes the value of A_1.

$S_{M0} = 1$ and $S_{M1} = 1 \rightarrow B_0$ takes the value of A_1.

S1S0 / A0A1	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	1	1	1	1
10	1	1	0	0

$B0=A0\overline{S1}+A1S1$

Figure 6 Karnaugh Map created for output B_0 and expression of output B_0 with Boolean equation.

Boolean equations provide the mathematical expression of digital circuits. However, when designing physical circuits, it is necessary to implement these equations using logic gates.

When performing this transformation, the basic operations used in Boolean expressions are mapped to certain logic gates:

The multiplication (AND - ·) operation is performed with the AND gate.

The addition (OR - +) operation is represented by the OR gate.

The not (Negation - ¬, overline) operation is represented by the NOT gate.

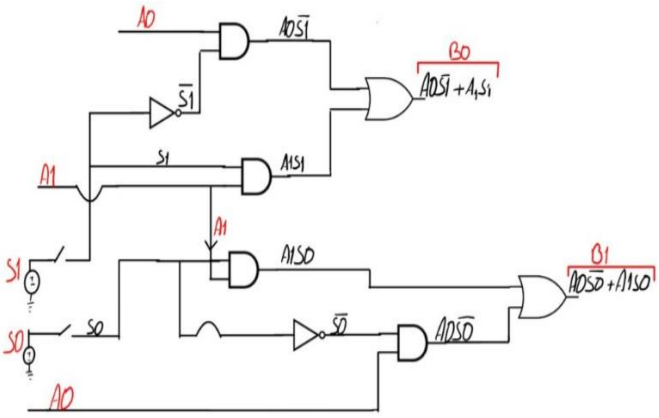

Figure 7 Expression of B_1 and B_0 outputs with logic gates.

In digital circuit design, Boolean equations can be implemented using logic gates designed and manufactured with CMOS (Complementary Metal-Oxide-Semiconductor) technology. CMOS circuits are built using both P-channel MOSFET (PMOS) and N-channel MOSFET (NMOS) transistors, which provide efficient and reliable operation.

- NMOS transistors provide (1) conduction when the input signal is high and form the pull-down network.
- PMOS transistors provide (0) conduction when the input signal is low and form the pull-up network.

This complementary structure allows switching between the high output voltage (VDD) and the low output voltage (GND), resulting in lower static power consumption compared to circuits designed with only NMOS or PMOS transistors. In addition, CMOS logic gates offer higher noise margins, increasing their reliability and performance. The combination of low power dissipation and fast switching speed makes CMOS technology the preferred choice for modern digital circuits.

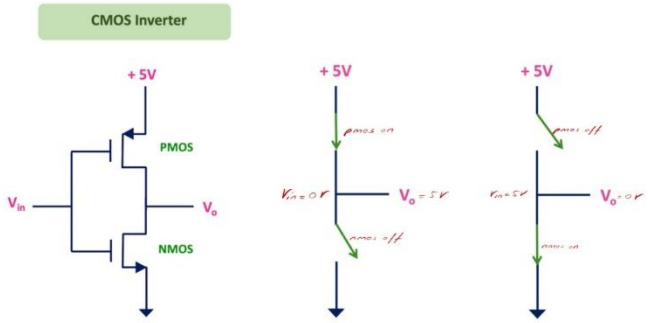

Figure 8 CMOS implementation of an inverter (NOT gate) using PMOS and NMOS transistors. When Vin = 0V, the PMOS conducts, pulling Vo to 5V. When Vin = 5V, the NMOS conducts, pulling Vo to 0V, achieving logical inversion.

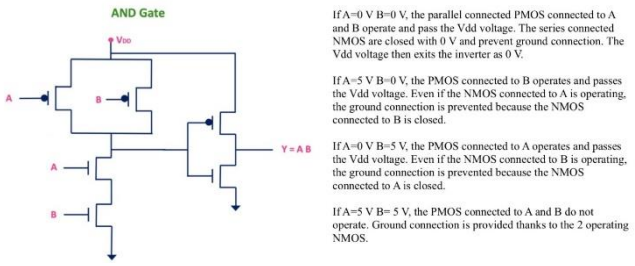

Figure 9 CMOS implementation of a 2-input AND gate using PMOS pull-up and NMOS pull-down networks. The circuit outputs Y = A·B, with NMOS conducting for Y = 1 when both inputs are high, and PMOS ensuring Y = 0 otherwise.

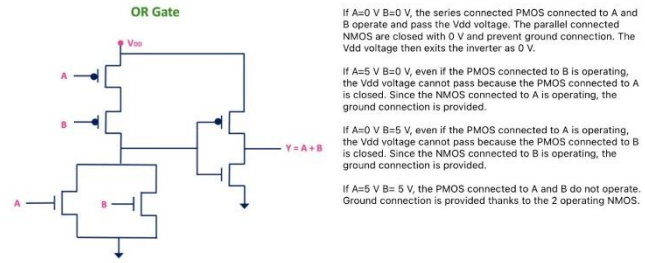

Figure 10 CMOS implementation of a 2-input OR gate using PMOS pull-up and NMOS pull-down networks. The circuit outputs Y = A + B, with PMOS conducting for Y = 1 when at least one input is high, and NMOS ensuring Y = 0 when both inputs are low.

The circuit designed with logic gates derived from the Boolean Equation is constructed with CMOS configuration and BS250 is used as PMOS and 2N7000 is used as NMOS. These transistors are selected based on their low power consumption, fast switching properties and logic level applications.

NMOS transistors (2N7000) are used for output logic low (0V) scanning when selected.

PMOS transistors (BS250) are used for output logic high (VDD) scanning when selected.

The gate terminals of these transistors are controlled according to the MUX selection inputs.

Simulation was designed with the selected transistor models and the circuit was observed.

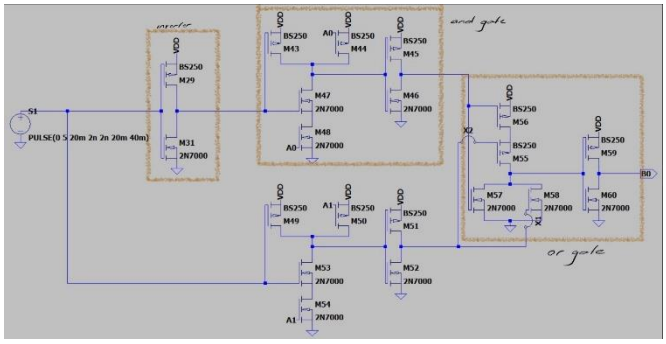

Figure 11 Expressing the B_0 output with CMOS configuration.

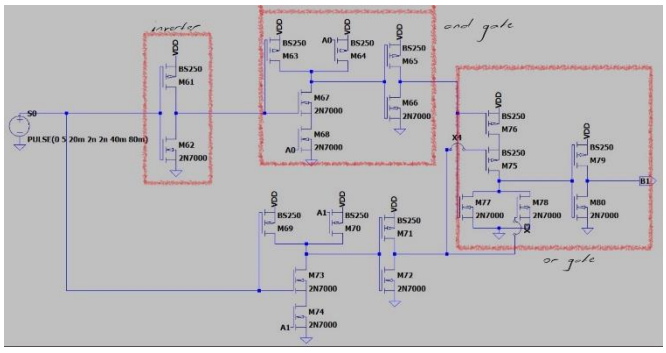

Figure 12 Expressing the B_1 output with CMOS configuration.

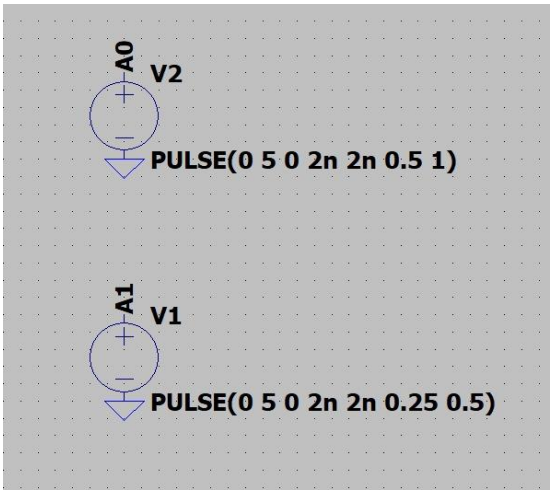

Figure 13 Representing A_1 and A_0 signals with a square wave.

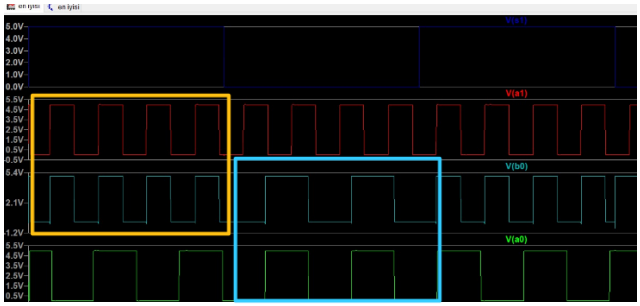

Figure 14 In the graph, when $S_{M1} = 1$, A_1 matches B_0, and when $S_{M1} = 0$, A_0 matches B_0, confirming that the circuit operates as expected.

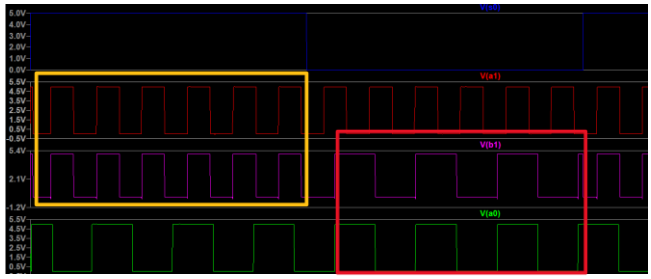

Figure 15 In the graph, when $S_{M0} = 1$, A_1 matches B_1, and when $S_{M0} = 0$, A_0 matches B_1, confirming that the circuit operates as expected.

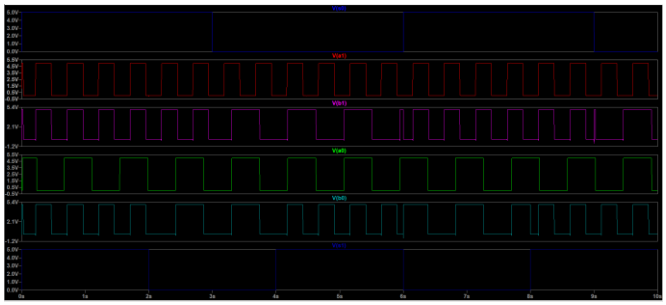

Figure 16 Graphs and values of all input and output signals in the circuit, between 0-5 volts.

As a result, the steps required for 2 by 2 mux design were listed. It was observed how the outputs worked based on the truth table. Karnaugh Maps were extracted based on the truth table of the B_1 and B_0 outputs and Boolean equations were derived. The adaptation of Boolean equations to circuit design with logic gates was investigated. In the simulation design process, the operation of logic gates was observed in order to express logic gates with CMOS configuration. According to the results, it was seen that the logic gates worked in accordance with the truth table. In the simulation process, 2 types of transistors that were sure to be suitable for CMOS configuration were used. In the simulation process, in order for the circuit established to be adaptable in real life, it was ensured that it was the best in terms of space, price, performance and sustainability. Finally, a simulation circuit that completely met the truth table was established and its accuracy was proven with the results obtained.

References:

1- Grout, I. (2008). Introduction to Digital Logic Design with VHDL. Digital Systems Design with FPGAs and CPLDs, 333–474. doi:10.1016/b978-0-7506-8397-5.00006-4

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