2023 Digital IC Design Homework 1

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Functional Simulation Result

Stage 1	Pass	Stage 2	Pass	Stage 3	Pass	Stage 4	Pass

Stage 1

```
------------Stage 1 : Maximum selection with 4-input MMS------------

    ------------Stage 1 :           Pass!             ------------
```

Stage 2

```
------------Stage 2 : Minimum selection with 4-input MMS------------

    ------------Stage 2 :           Pass!             ------------
```

Stage 3

```
------------Stage 3 : Maximum selection with 8-input MMS------------

    ------------Stage 3 :           Pass!             ------------
```

Stage 4

```
------------Stage 4 : Minimum selection with 8-input MMS------------

    ------------Stage 4 :           Pass!             ------------
```

Description of your design

Table 2 in the spec, the selection case of the mutiplexer, indicates that when select and cmp are different, the output will be the second number; otherwise, it will be the first one. This result is similar to that of an XOR gate. Therefore, we can use (select ^ cmp) to simplify the circuit and construct 2-number MMS, eliminating the need for another multiplexer that would require 4 gates. Once we have a 2-number MMS, we can hierarchically construct a 4-number MMS and further an 8-number MMS by utilizing the 2-nunber MMS.