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EE-413 Project Phase 1

Introduction

In this report subblocks of the 'Custom Signal Manipulator' will be examined. Main function of overall system is to take triangular analog inputs and determine the operation on those signals depending on another input coming from the digital block. To accomplish this purpose serial to parallel converter, decoder, successive approximation register(SAR), analog to digital converter(ADC), digital to analog converter (DAC) and arithmetic logic unit (ALU) will be used.

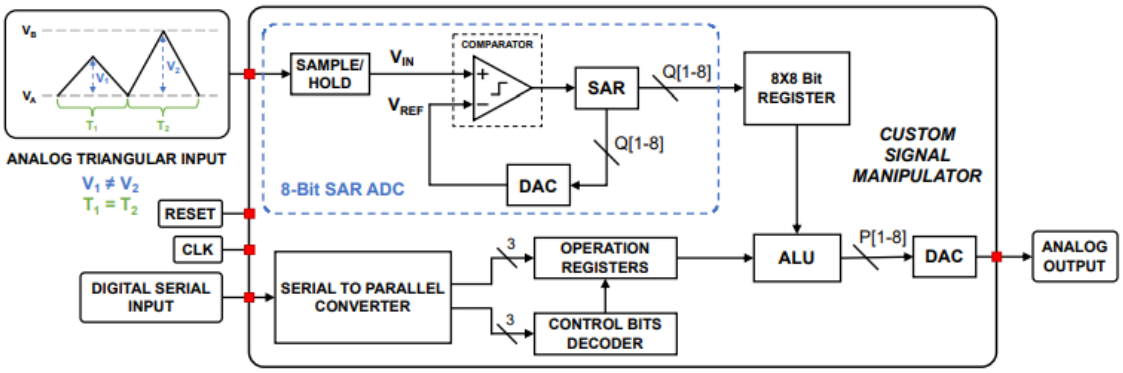

Figure 1 : Overall System Structure

Subblocks of the system

Serial to Parallel Converter

This block will be utilized to convert the serial input to parallel data. To be able to do that I will use 6 bit shift register. 3 of them used in control bits decoder and 3 of them will be used in operation register. Decoder will look for start (101) code to start the operation.

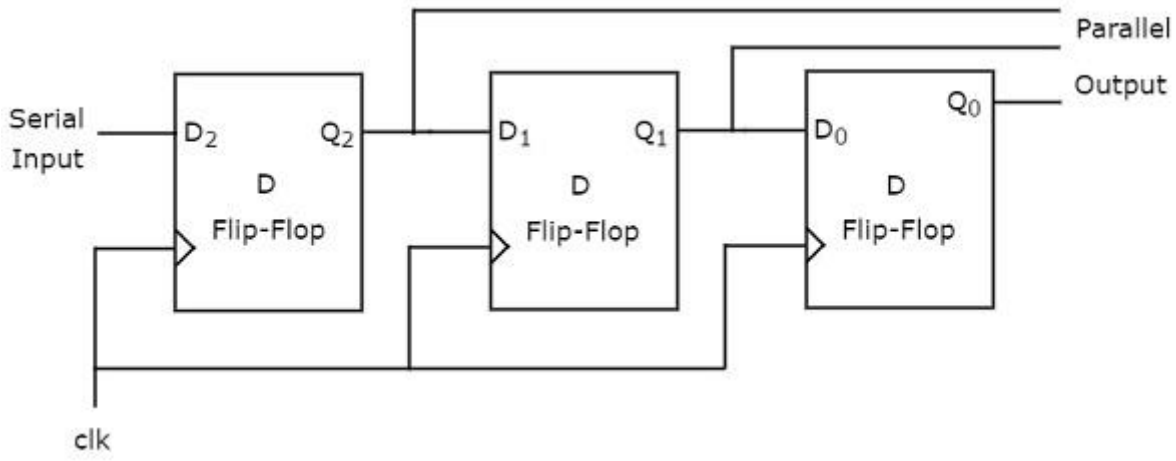

Figure 2 : 6 bit shift register design

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Control Decoder

As it is mentioned in the previous block, this subblock will determine whether the correct data is coming or not. This will provide that system is not mistakenly initiated etc.

Operation Register

This block will hold the operation code to be executed. It will work as a temporary memory or a buffer such that ALU executes the correct operation. Hence delay times should be arranged very well for this block.

8x8 Register

It holds 8 8-bit data to be executed in the ALU. It should work with operation register with a certain harmony so that a phase shift or any kind of that error occurs.

Arithmetic Logic Unit

Certain operations was described in the project manual for 3 bit operation codes. Those operations are namely dividing, multiplying, pulling up-down, offset addition-removal and flipping. Output of this block will be transformed into analog signal with DAC at the end.

SAR ADC

This block will be used for converting analog data to digital data. SAR ADC is used since it has a good characteristic in speed required applications.

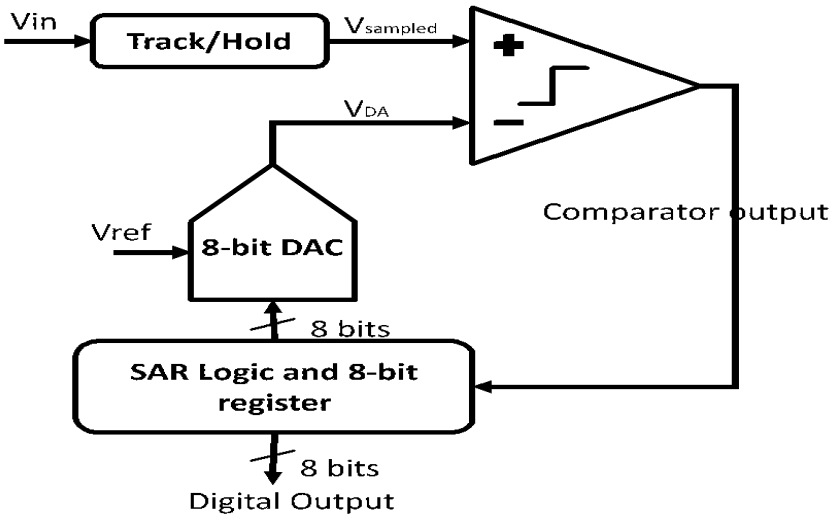

Figure 3 : 8 bit SAR structure

Sample/Hold Circuit

This sub block of the SAR enables the sampling by holding the analog data till it is converted to digital. In the below figure overall structure is shown. First amplifier has a gain of unity which does not change the V_{in}. Also A1 has high R_{in} to prevent load at the input. While it has low R_{out} to reduce the charging time of C_H. MFET is used to control the data routine, so C_H is loaded and given to the system while rest analog signal waits. A2 has a gain of unity as well so that V_{in} doesn't disturbed.

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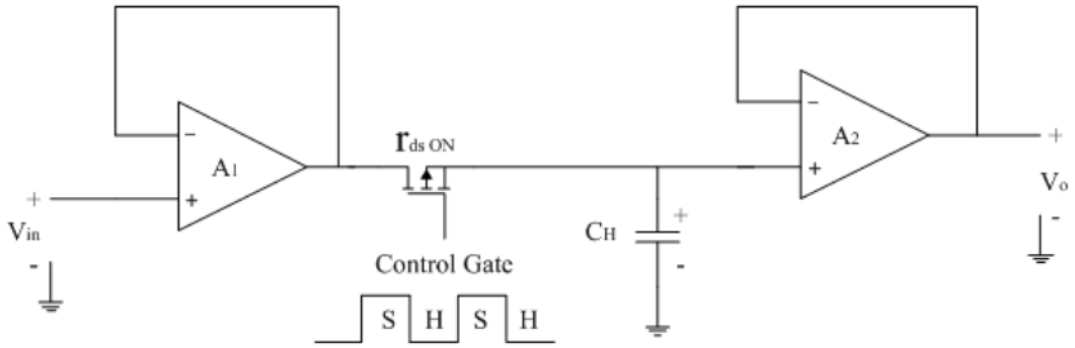

Figure 4 : Sample/Hold Circuit Schematic

Comparator

This block will be used to compare between V_{ref} and the input signal. As it is stated in the project manual a basic comparator will be used. W/L ratios will be determined later in the design stage.

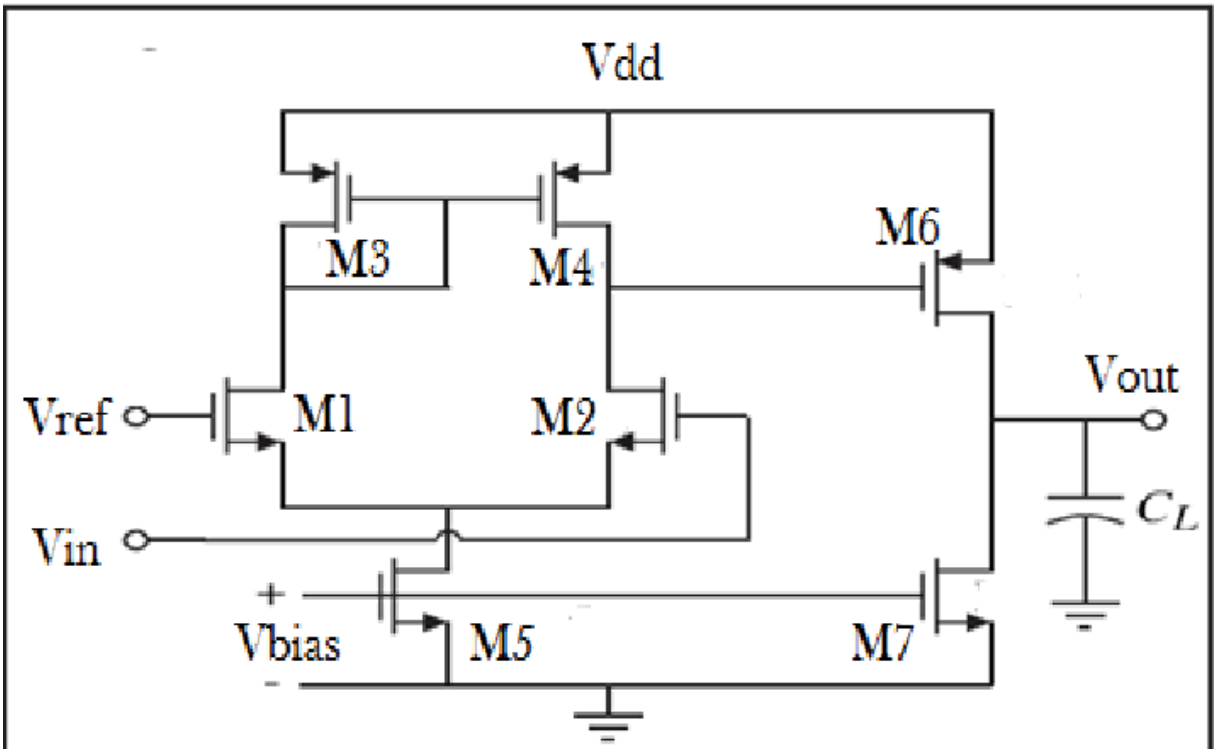

Figure 5 : Comparator Circuit Design

SAR Control Unit

This block is responsible for the determining the right conversion of the analog signal to the digital signal. This is done by looking at the result of the comparison in the previous stage. At the first cycle MSB is set to 1 so the overall register is '10000000' and compared with the sampler output. If the result of the comparison is less than 0 then MSB set to 0 and vice versa. Hence this goes on and on for 8 bit of 10 cycles to generate an output to be written on 8x8 bit register. Since this process goes on for 10 cycles sampling process should be 10 times slower than this.

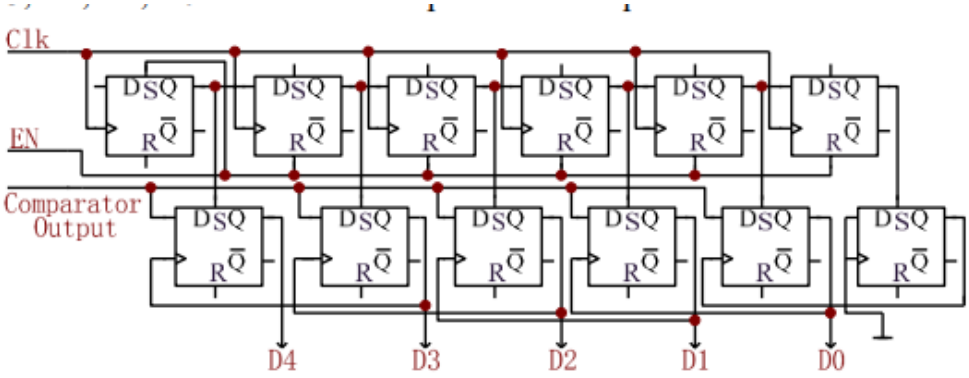

Figure 6 : SAR Control Logic Unit

Digital to Analog Converter (DAC)

This block converts the digital data in the SAR control unit to the analog data so that it can be compared with the input. To succeed this purpose 8 bit switched capacitor DAC will be used. This decision based on the urge of decreasing the power consumption while complexity of the design doesn't change much. However it should be noted that in a case of this doesn't work as desired one can change it design with R-2R logic easily.

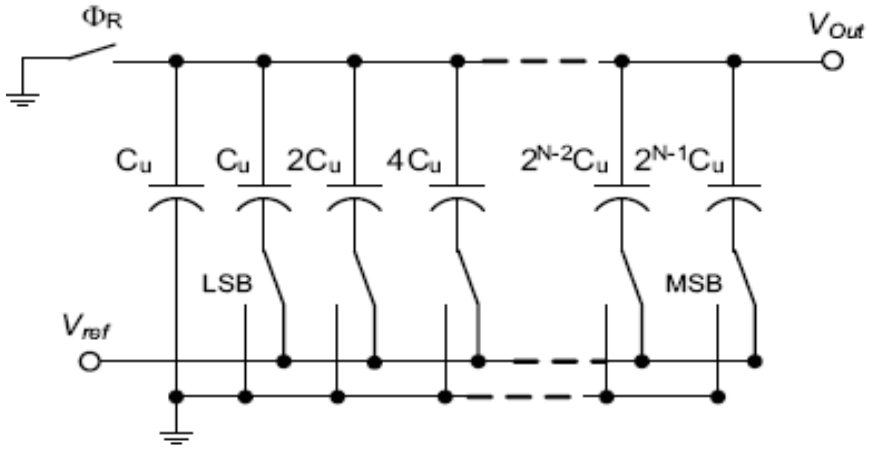

Figure 7 : Switch Capacitor Structure DAC

Conclusion

To sum up, in this report general structure of the custom signal manipulator is determined. While the basic concepts that will be used is determined, the specific design values will be determined in the design process. Hence a general opinion and view of the project is built on.