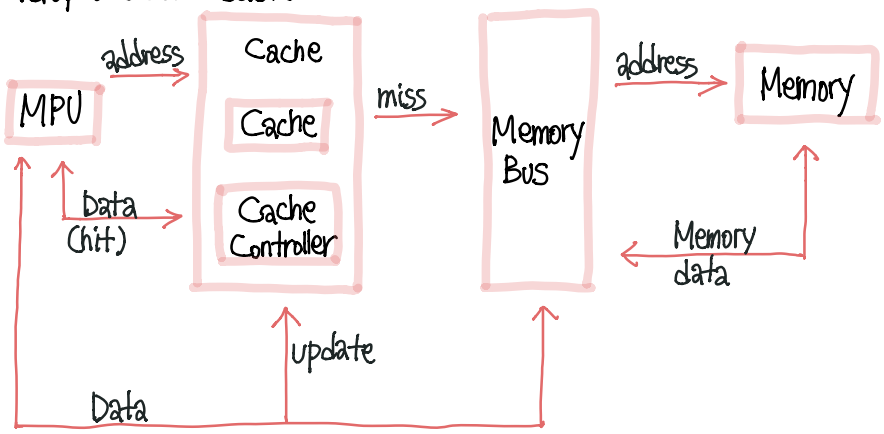
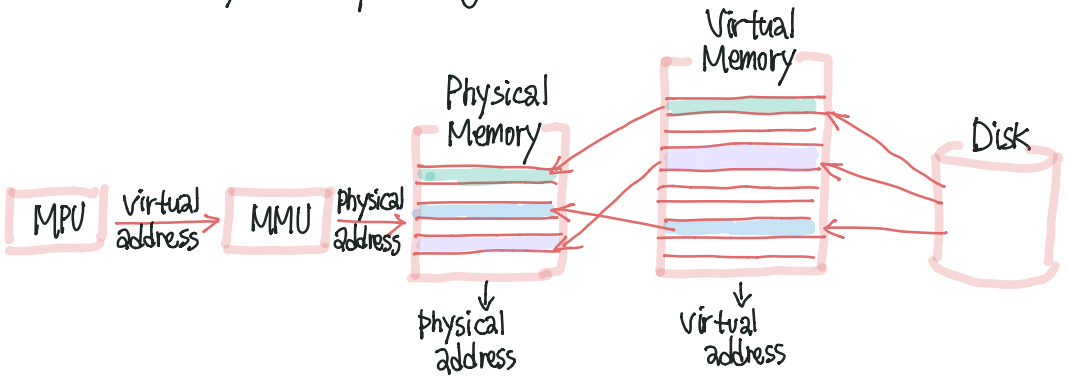
컴퓨터구조

- Microprocessor cache

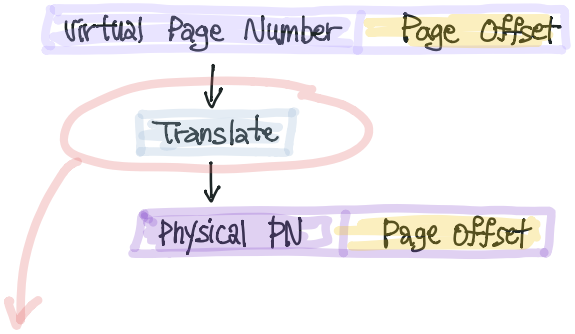


- Virtual Memory (Memory Management)

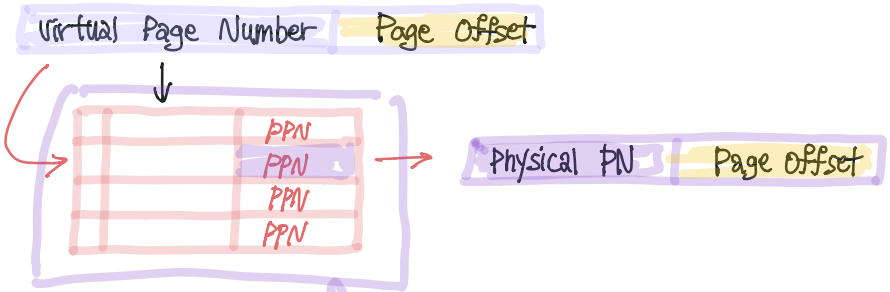


→ 동적 메모리 할당.
가상메모리 주소와, 물리메모리 주소를, 관리 (translate)

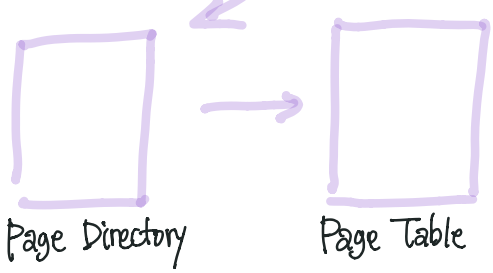
- 어떻게 Virtual Address → Physical Address !



1. 기본적인 Translate



2. Two-level Paging

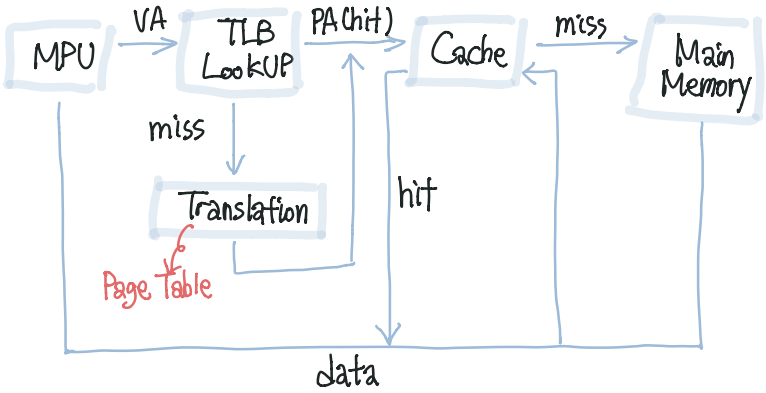


3. TLB (Translate Look-Aside Buffer)

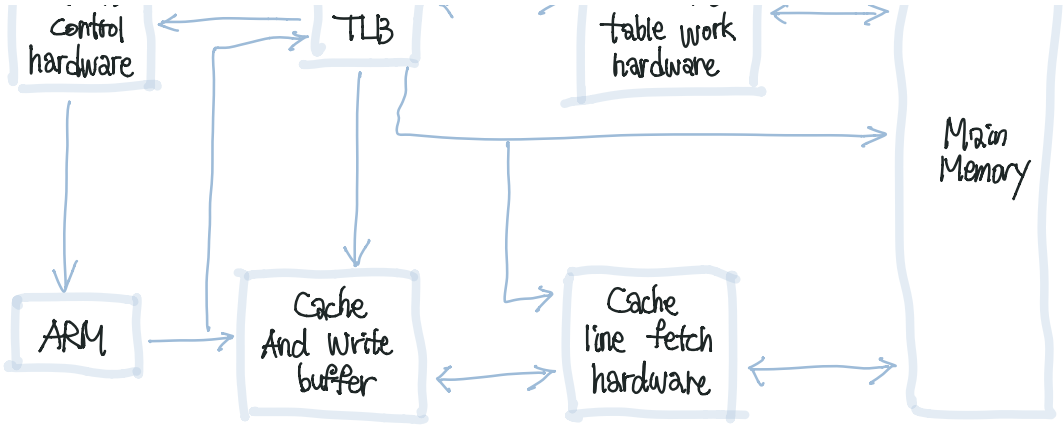
- translate의 속도 향상.
- permits fully associate lookup

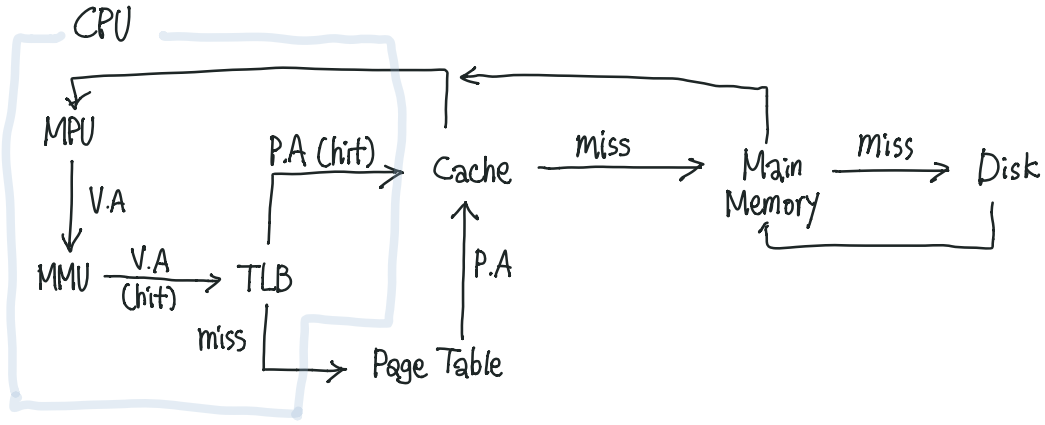
virtual address	physical address	Dirty	Ref.	Valid	Access

- 흐름.



- Cached MMU Memory Overview


control hardware
TLB
table work hardware
Main Memory
ARM
Cache And Write buffer
Cache line fetch hardware


CPU
MPU
V.A
MMU
V.A (hit)
TLB
P.A (hit)
Cache
miss
Main Memory
miss
Disk
P.A
miss
Page Table