SRM UNIVERSITY AP
Amaravati

Department of CSE

Computer Organization and Architecture (CSE204)

Assignment I

Note: Choose the most appropriate option for following questions and give reason to justify your choice.

1. The decoded instruction is stored in:
   a) PC b) MDR c) Registers d) IR

2. The interrupt vector address for TRAP is

   a) 000h b)0024h c)0018h d) 002Ch

3. Consider the following register transfer language R3←R3+M[R1+R2] Where R1, R2 are the CPU registers and M is a memory location in primary memory. Which addressing mode is suitable for above register- transfer language?
   a)Immediate b) Indexed c) direct d) Displacement

4. In a 16-bit instruction code format 3 bit operation code, 12 bit address and 1 bit is assigned for address mode designation. For indirect addressing, the mode bit is
   a) 0 b) 1 c) pointer d) Offset

5. A 32-bit address bus allows access to a memory of capacity
   a) 64 MB b) 16 MB c) 1GB d) 4GB

6. Cache memory enhances
   a) Memory capacity b)Memory access time

   c) Effective memory access time d) secondary memory access time.

7. The Read/ Write line
   a) Belongs to the data bus b) Belongs to the control bus
   c) Belongs to the Address bus d) CPU Bus

8. Which of following registers are used by the processor for fetch and execute operations?
   1) Program counter 2. Instruction Register 3. Address register
   a) 1 and 3 b) 1 and 2 c) 2 and 3 d) 1, 2 and 3.

9. If the memory chip size is 256*1 bits, then how many chips are required to make up 1KB of memory?
   a) 8 b) 16 c) 24 d) 32

10. Which of the following is not involved in a memory write operation?
a) MAR b) PC c) MDR d) data bus

11. Which of the following holds data and processing instructions temporarily until the CPU needs it?
a) ROM b) Control unit c) main memory d) coprocessor chips

12. Which of the following affects processing power?
a) data bus capacity b) addressing scheme c)clock speed d) all of these

13. The size of the exponent in IEEE 754 32-bit format is
a) 10 bits b) 9 bits c) 8 bits d) 11 bits

14. The load instruction is mostly used to designate a transfer from memory to a processor register known as:
a) Instruction Register b) Accumulator c) Program counter d) Memory address Register

15. Which is not a function of EU (Execution Unit) in 8086 architecture?
a) Instruction Fetching from memory b) Instruction Execution
c) Instruction Decoding d) Requesting BIU (Bus Interface Unit) for data read

16. Which method/s of representation of numbers occupies a large amount of memory than others?
a) Sign-magnitude b) 1's complement c) 2's complement d) 1's & 2's compliment

17. How many conditional flag and control flag 8086 contains?
a) 3,6 b) 6,3 c) 6,6 d) None of these

18. The word length of CPU is defined as
a) The maximum addressable memory size b) The width of the address bus
c) The width of the CPU register d) the number of general purpose CPU register

19. Match List-I with List-II and select the correct answer using the codes given below the list:

List-I	List-II
A. MOV X, R1	1. Three address instruction
B. STORE X	2. Zero address instruction
C. POPX	3. One Address instruction
	4. Two Address instruction

Codes:	A	B	C
a)	4	3	2
b)	3	2	1
c)	2	3	4

d) None of these

20. The following are the some of the sequences of operations in instruction cycle, which one is the correct sequence?

a) Data from memory → Data Register
PC → Address register
Data Register → IR
PC+1 → PC

b) Address register → PC
Data register → Data from memory
Data register → IR
PC + 1 → PC

c) PC → Address register
Data from memory → Data register
Data register → IR
PC + 1 → PC

d) None

21. Secondary memory is also called____

a) Auxiliary b) Backup store c) Both a and b d) None of these

22. INTR: it implies the_____ signal:

a) INTRRUPT REQUEST b) INTRRUPT RIGHT
c) INTRRUPT RONGH d) INTRRUPT RESET

23. The memory which is programmed at the time it is manufactured

a) EPROM b) RAM c) ROM d) PROM

24. The idea of cache memory is based

a) on the property of locality of reference b) on the heuristic 90-10 rule
c) on the fact that references generally tend to cluster d) all of the above

25. An n-bit microprocessor has

a) n-bit program counter b) n-bit address register
c)n-bit ALU d) n-bit instruction register

26. How many clock cycles are required for implementing the Fetch micro program?

a) <3 b) 4 c) 3 d) >4

27. If system is supporting F flags/conditions, then how many bits are required for representing flag/condition in one address control instruction?

a) $\log_3 F$ b) F c) $\log_F 2$ d) $\log_2 F^2$

28. In which of the following control unit design technique one control word always generate only one control signal?

a) Horizontal microprogramming b) Nano programmed control unit design
c) Vertical microprogramming d) None of the above

29. A system supports vertical microprogramming to generate N control signals. How many bits are needed to encode N control signals in control memory?

a) N Bits b) N2 bits c) $\log_2 N$ bits d) None of the above

30. Assume a system with limited memory. Which one of the following control unit design technique is suitable for generating the N control signals:

a) Vertical microprogramming b) Nano programmed control unit design
c) Horizontal microprogramming d) Both b and c

31. Control word sequencing is used for:
a) Fetching the instruction from memory
b) Generating the 20 Bit physical address
c) Generating the control signals in proper
d) Storing the control signals in control memory

32. Which of the following is false about RISC Architecture?
a) Uses Load/Store Architecture
b) Instruction takes single clock cycle to get executed
c) Each instruction occupies exactly one word in memory
d) None of the above

33.Time required to generate the control signal in Vertical microprogramming is
a) $T_{CS} = T_{CM} + T_{HW}$ b) $T_{CS} = T_{CM} + T_{HW} - T_{Decoder}$
c) $T_{CS} = T_{CM} + T_{Decoder} + T_{HW}$ d) None of the above-ed

34. Which of the following is true about the RISC architecture:
a) has fewer instructions b) has fewer addressing modes
c) is easier to implement using hard-wired control logic d) All of the above

35. RTN stand for
a) Register Transmission Notation b) Regular Transmission Notation
c) Register Transfer Notation d) Regular Transfer Notation

36. The Instruction Fetch phase ends with
a) Placing the data from the address in MAR into MDR
b) Placing the address of the data into MAR
c) Completing the execution of the data and placing its storage address into MAR
d) Decoding the data in MDR and placing it in IR

37. When the instruction is read from the memory, it is called
a) Memory Read Cycle b) Fetch Cycle
c) Instruction Cycle d) Memory Write Cycle

38. N bits in operation code imply that there are ____possible distinct operators.
a) 2n b) 2^n c) n/2 d) n^2

39. Which is the order decided by a processor to execute an instruction
a) Decode, Fetch, Execute b) Execute, Fetch, Decode
c) Fetch, Execute, Decode d) Fetch, Decode, Execute

40. In which of the following control unit design the control signal is represented as sum

of products (SOP) expression?
a) Horizontal microprogramming b) Nano programmed control unit design
c) Hardwired control unit design d) Vertical microprogramming

41. The control unit controls other units by generating_____
a)Control Signals b) Timing Signals c) Transfer Signals d) Command Signals

42. In which of the following control unit design, the maximum degree of parallelism is 1?
a) Nano programmed control unit design b) Horizontal microprogramming
c) Vertical microprogramming d) Both a) and c)

43. Which of the following is true about Horizontal microprogramming?
a) Uses 1 bit per control signal b) Lengthy control word
c) Control signal is stored in encoded form d) Both a) and b)

44. Which of the following control unit design uses decoder for control signal generation?
a) Nanoprogrammed control unit design b) Horizontal microprogramming
c) Vertical microprogramming d) Both b) and c)

45. Which of the following control unit design is not suitable in design and testing kind of environment?
a) Nano programmed control unit design b) Horizontal microprogramming.
c) Vertical microprogramming d) Hardwired control unit design

46. Which of the following control unit design is most flexible among all?
a) Nano programmed control unit design b) Horizontal microprogramming
c) Vertical microprogramming d) Hardwired control unit design

47. Consider a nano programmed control unit with 1024 words in μprogrammed control memory and 64 words in ηprogrammed control memory. The system is using 48 control signals.What is the total control memory size in bytes?
a) 2332 Byte b) 2532 Byte c) 2432 Byte d) 2222 Byte

48 Which of the following control unit design utilize two levels of control memory?
a) Hardwired control unit design b) Horizontal microprogramming
c) Vertical microprogramming d) Nano programmed control unit design

49. If the criteria for choosing the control unit design is memory and time. Then which one of the following pair is ideal?
a) Horizontal microprogramming, Vertical microprogramming
b) Vertical microprogramming, Nanoprogrammed control unit design

c) Nanoprogrammed control unit design, Vertical microprogramming,
d) Nanoprogrammed control unit design, Horizontal microprogramming

50. What are the possible input to the control unit?
a) Clock b) Flags c) Opcode d) All of the above

51 A _____ Hazard may occur if sufficient resources are not available for different stages during the same clock cycle
a) Data hazard b) Control hazard c) Structural hazard d) None of the above

52 Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 Taken on a non- pipelined but identical CPU, then we can say that _____ taken for one instruction fetch cycle.
a) $T1 \leq T2$ b) $T1 \geq T2$ c) $T1 < T2$ d) T1 is T2 plus time

53. A 4-stage pipeline has stage delays as 150, 120, 160 and 140 ns respectively. Registers that are used between the stages have a delay of 5 ns each Assuming constant clock cycle rate, the total time taken to process 1000 data items on this pipeline will be_____ microseconds,
a) 120 b) 160.5 c)165.5 d)590.0

54 Consider a pipelined processor with the following 4 stages:
IF : Instruction Fetch ID : Instruction Decode and Operand Fetch
EX : Execute WB : Write Back
The IF, ID, and WB stages takes one clock cycle each to complete the operation.
EX of ADD instruction requires 1 cycle,
EX of SUB instruction requires 1 cycle,
EX of MUL instruction requires 3 cycles
IF operand forwarding is used then the no. of cycles required to execute following set of instructions are

```
ADD R2, R1, R0      // R2←R1 +R0
MUL R4, R3, R2      // R4←R3*R2
SUB R6, R5, R4      // R6←R5-R4
```

a)7 b) 8 c) 10 d) 14

55. For a pipelined CPU with single ALU, consider the following
1. The J+1 instruction uses the result of the J^{th} instruction as an operand
2. The execution of a conditional Jump instruction
3. The J^{th} and $(J+1)^{th}$ instruction requires ALU at the same time
Which of the above can cause a hazard?
a) Only b) 2 and 3 Only c) 3 Only d)All of the above

56. Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining, When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instruction incurs 2 pipeline stall cycles is _____

a) 2 b) 5 c) 4 d) 3

57. Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.
    P1: Four stage pipeline with stage latencies 1ns, 2ns, 2ns, 1ns.
    P2: Four stage pipeline with stage latencies 1ns, 1.5ns, 1.5ns, 1.5ns.
    P3: Five stage pipeline with stage latencies 0.5ns, 0.5ns, 1ns, 1ns, 1ns.
    P4: Five stage pipeline with stage latencies 0.5ns, 0.5ns, 1ns, 1ns, 1.1ns.
    Which of the processor has the highest peak clock frequency?
    a) P1 b)P2 c) P3 d)P4
58. Consider the following code, it has to be executed using a pipelined processor with one delay slot.
    I1: ADD R2 ← R7 + R8
    I2: SUB R4 ← R5 – R6
    I3 : ADD R1 ← R2 +R3
    I4 : Store Memory [R4] ← R1
    Branch to Label if R1 == 0
    Which of the instructions I1, I2, I3, I4 can legitimately occupy the delay slot without any other program modification?
    a) I1 b) I2 c) I3 d) I4

59. Which of the following techniques can help achieve throughput of less than 1 clock cycles?
    a) Very long Instruction word b) Superscalar Processors
    c) Both (a) and (b) d)None of the Above

60. Consider the following code Sequence having five instructions I1 to I5. Each of these instructions has the following format. OP R_i, R_j, R_kWhere operation OP is performed on contents of registers Rj, and Rk, and the result is stored in register Ri.
    I1 : ADD R1, R2, R3
    I2 : MUL R7, R1, R3
    I3 : SUB R4, R1, R5
    I4 : ADD R3, R2, R4
    I5 : MUL R7, R8, R9
    Consider the following three statements
    S1: There is an anti-dependence between I2 and I5.
    S2: There is an anti-dependence between I2 and I4
    S3: Within an instruction pipeline an anti-dependence always creates one or more stalls.
    Which one of the above statements is/are correct?
    a) Only S1 is true. b) Only S2 is true
    c) Only S1 and S3 are true d)Only S2 and S3 are true

61. As a computer architect you have been tasked with designing a CPU with static branch prediction then which of the following is true
    a) Branch penalty of (a) is minimum b) Branch penalty of (b) is minimum
    c) Branch penalty of (c) is minimum d)None of the above.

62. Suppose the function F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G, respectively. Given two instances of U_F and U_G, find the minimum time required to compute F(G(Xi)), for $1 \le i \le 10$.

a) 50 b) 30 c) 18 d) 28

63. A 5-stage pipeline processor has 5 stages as Instruction Fetch (IF), Instruction Decode(ID), Operand Fetch (OF), Execute (EX), and Write Back (WB). These stages take 5, 4, 20, 10, and 3 nanoseconds respectively. Additionally, inter-stage buffer delay is 2 ns. As a computer architect you have 2 choices.

1.A basic pipeline design with 5-stages. Or,

2. An advanced design where operand fetch stage is divided into two stages OF1 and OF2 with delays 12 and 8 ns respectively.Then the speed-up achieved by advanced design over basic design is _____

a) 1 b) 1.5 c) 2.5 d) 3

64. A pipeline system has 40% branch instructions each of which introduces 3 stall cycles. The throughput of the pipeline assuming a clock duration of 15 ns is

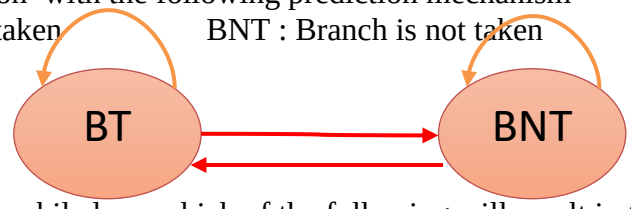
a) 10 MIPS b) 15 MIPS c) 23 MIPS d) 33 MIPS

65. A pipeline has a speedup factor of 10, and operating with an efficiency of 80%, then the no. of stages in the pipeline is

a) 10 b) 11 C) 12 D)13

66. As a computer architect you have been tasked with designing a CPU with dynamic branch prediction with the following prediction mechanism

BT : branch is taken BNT : Branch is not taken



To implement a do while loop which of the following will result in the minimum branch penalty if the initial assumption is branch is taken (BT).

(a) Do { A=A+4;
i++;
} while (i<50)
B= B+4;

(b) Do { A=A+4;
A=A+4;
i++;
} while (i<25)
B= B+4;

(c) Do { A=A+4;
A=A+4;

```
A=A+4;
A=A+4;
A=A+4;
i++;
} while (i<10)
B= B+4;
```

a) Branch penalty of (a) is minimum b) Branch penalty of (b) is minimum
c)Branch penalty of (c) is minimum d) None of the above.

67. Consider a machine with 10 ns clock and it takes 4 clock cycles per ALU instruction, 5 clock cycles per branch instruction, 6 clock cycles per memory instruction. If there exists 40% ALU instructions,20% branch instructions and 40% memory instructions what is the speedup factor?
a) 10 b) 5 c) 7 d) 8

68. Consider a 5-stage pipeline system having clock duration of 10 ns. The pipeline system has 30% branch instructions with 60% conditional instructions, 40% of those satisfy the condition. If there is no penalty if branch is taken, and penalty of 4 cycles otherwise then what is the average execution time?
a) Approx. 10 b) Approx. 15 c) Approx. 17 d) Approx. 18

69. A 4-stage pipeline has stage delay of 800, 500, 400 and 300 picoseconds. The stage with 800 ps is replaced with two stage of 600 and 350 ps. The throughput increase due to modification is
a) 25% b)30% c)33.33% d) 40%

70. Write after read hazard is
a) Output dependency b) Anti dependency c) True Dependency d) All of these

71. The following instructions have
I1: SUB R3, R1, R4
I2: OR R2, R4, R5
a) True dependency b) Anti dependency c) Output dependency d)None of the above

72. Branching is an example of
a) Data Hazard b) Control Hazard c) Structural Hazard d) None of the above

73. Register renaming is done in the pipelined processors
a) As an alternative to register allocation at the compile time.
b) For efficient access to function parameters and local variables.
c) To handle certain kinds of hazards.
d) As part of address translation.

74. The pipelining process is also called as _____
a) Superscalar operation b) Assembly line operation
c) Von Neumann cycle d) None of the above

75. Each stage in pipelining should be completed within _____ cycle.
a) 1 b) 2 c) 3 d) 4

76. The standard SRAM chips are costly as _____
a) They use highly advanced micro-electronic devices
b) They house 6 transistor per chip
c) They require specially designed PCB's
d) None of the mentioned

77. The drawback of building a large memory with DRAM is _____
a) The large cost factor b) The inefficient memory organization
c) The Slow speed of operation d) All of the mentioned

78. The fastest data access is provided using _____
a) Caches b) DRAM's c) SRAM's d) Registers

79. 5. The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____
a) Level 1 cache b) Level 2 cache c) Registers d) TLB

80. The larger memory placed between the primary cache and the memory is called _____
a) Level 1 cache b) Level 2 cache c) EEPROM d) TLB

81. The next level of memory hierarchy after the L2 cache is _____
a) Secondary storage b) TLB c) Main memory d) Register

82. The last on the hierarchy scale of memory devices is _____
a) Main memory b) Secondary memory c) TLB d) Flash drives

83. In the memory hierarchy, as the speed of operation increases the memory size also increases.
a) True b) False

84. If we use the flash drives instead of the hard disks, then the secondary storage can go above primary memory in the hierarchy.
a) True b) False

85. In the memory control the fastest memory is

a) SRAM b) Cache c) Registers d)DRAM

86. Cache memory is implemented using
a) Dynamic RAM b) Static RAM c) PROM d)EPROM

87. The Minimum delay between two successive read operations is_____
a) Cycle time b) Latency c) Delay d) None of the above

88. Because of virtual memory, the memory can be shared among _____
a) processes b) threads c) instructions d) none of the above

89. _____ is the concept in which a process is copied into the main memory from the secondary memory according to the requirement.
a) Paging b) Demand paging c) Segmentation d) Swapping

90. The type of device which is 3 ½ inch floppy drive is nothing but
a) Storage b). Input c) Output d) Software

91. The storage device that uses rigid, permanently installed magnetic disks to store data is
a) Floppy b) Permanent disk c) Optical disk d) Hard disk

92. How will know surely that the hard drive has failed?
a) Scrapping b) Clicking c) Buzzing sound d) All of the above

93. What is the main directory of a disk called?
a) Folder b) Root c) Sub d) Network

94. In FIFO page replacement algorithm, when a page must be replaced _____
a) oldest page is chosen b) newest page is chosen
c) random page is chosen d) none of the mentioned

95. Effective access time is directly proportional to _____
a) page-fault rate b) hit ratio c) memory access time d) none of the mentioned

96. Working set model for page replacement is based on the assumption of _____
a) modularity b) locality c) globalization d) random access

97. When a program tries to access a page that is mapped in address space but not loaded in physical memory, then _____
a) segmentation fault occurs b) fatal error occurs
c) page fault occurs d) no error occurs

98. Swap space exists in _____
a) primary memoryb) secondary memory c) cpu d) none of the mentioned

99. _____has smallest storage capacity

a) Floppy disk b) Zip disk c) Hard disk d) CD

100. What is a zip drive?

a) An output device b) An input device

c) A medium capacity removable disk storage system d) Software