NCTU-EE IC LAB – Fall 2017

Lab04 Exercise

Design: ALU

Data Preparation

1. Extract test data from TA's directory:

% tar xvf ~iclabta01/Lab04.tar

2. Ask the TA if you have any question.

Design Description

A calculator with two stages will be implemented. In the first stage, the calculator will receive five 5-bit signed numbers which are out of order. Then, it reorders data into numerically descending manner first. In the second stage, four arithmetical operations will be applied with following modes:

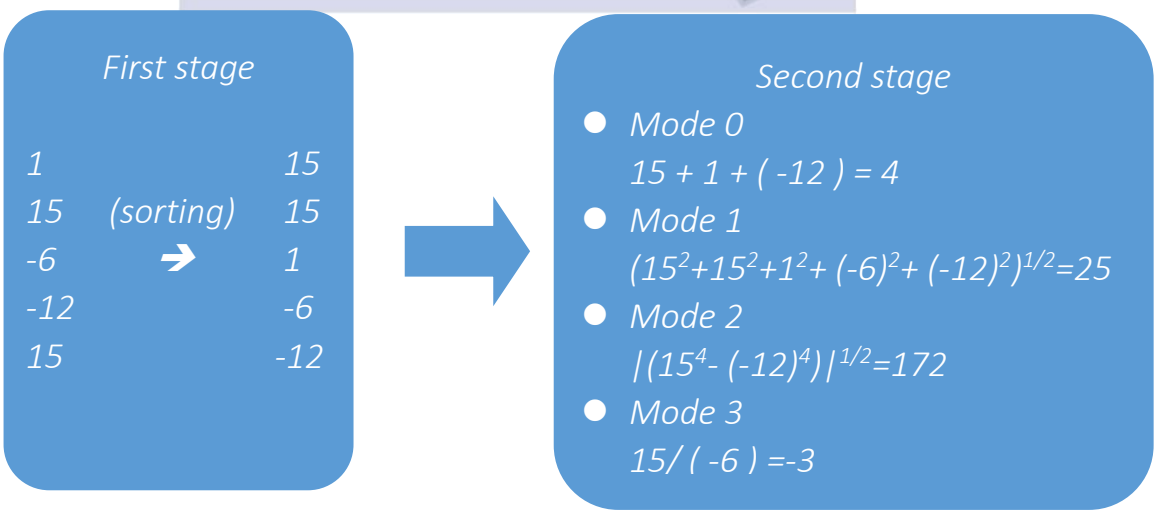
- Mode 0:

  Sum up the first, the third and the fifth number.
- Mode 1:

  Square all the input numbers. Then, sum up them and take a square root.
- Mode 2:

  Take a square root of the absolute value of the first number to the fourth power minus the fifth number to the fourth power.
- Mode 3:

  The second number is divided by the fourth number. (the fourth wouldn't be 0)



Input and Output

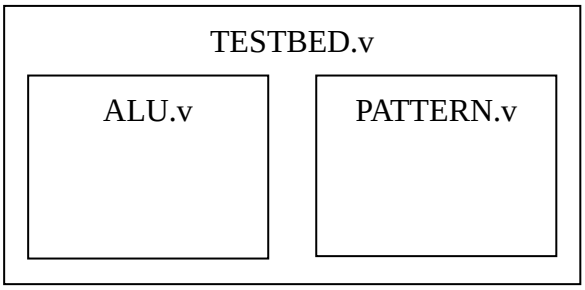
Input signal	Bit width	Definition
clk	1	Clock
rst_n	1	Asynchronous active-low reset
in_valid	1	Enable input signal
mode	2	Output mode
in_number1	5	Input number1 (number doesn't mean it's order)
in_number2	5	Input number2 (number doesn't mean it's order)
in_number3	5	Input number3 (number doesn't mean it's order)
in_number4	5	Input number4 (number doesn't mean it's order)
in_number5	5	Input number5 (number doesn't mean it's order)

Output signal	Bit width	Definition
out_valid	1	Enable output check
out_number	10	Output number

Specification

1. Top module name: **ALU**(design file name: **ALU**.v)
2. It is **asynchronous** reset and **active-low** architecture.
3. The reset signal would be given only once at the beginning of simulation. All output signals should be reset after the reset signal is asserted.
4. The clock period of the design must be shorter than **5ns**.
5. After **2 cycles** of rst_n, in_valid will pull up.
6. Input data will be given continuously when in_valid pull up.
7. out_number should output **continuously** when out_valid pull up.
8. The synthesis result of data type **cannot** include any latches.
9. After synthesis, you can check ALU.area and ALU.timing. The area report is valid when the slack in the end of timing report should be **non-negative**.
10. You must output your answer within **50 cycles**.
11. In mode 3, the **quotient** will be **rounding to the nearest integer**. For -2.49 and 2.51, they will be -2 and 3 separately.
12. The **square root** will be **rounding down**. For 2.51, it will be 2.

Block Diagram



Note

1. **Grading policy:**

   RTL and Gate-level simulation correctness: 70%

   Performance: 30%

   - Latency 20%
   - Area 10%

2. **Please upload the following file on e3 platform before 12:00 p.m. on Oct. 23:**

   - ALU_iclabxx.v (xx is your account number)
   - oo.txt (oo is clock period of your design)

3. **Template folders and reference commands:**

   01_RTL/ (RTL simulation) **./01_run**

   02_SYN/ (Synthesis) **./01_run_dc**

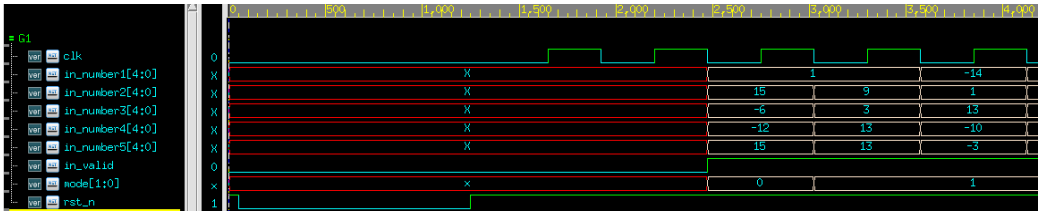
   (Check the design if there's latch or not in ***syn.log***)

   (Check the design's timing in /Report/ **ALU.*timing***)

   03_GATE / (Gate-level simulation) **./01_run**

Example Waveform

Input signal



Output signal