Computer Organization Lab 3

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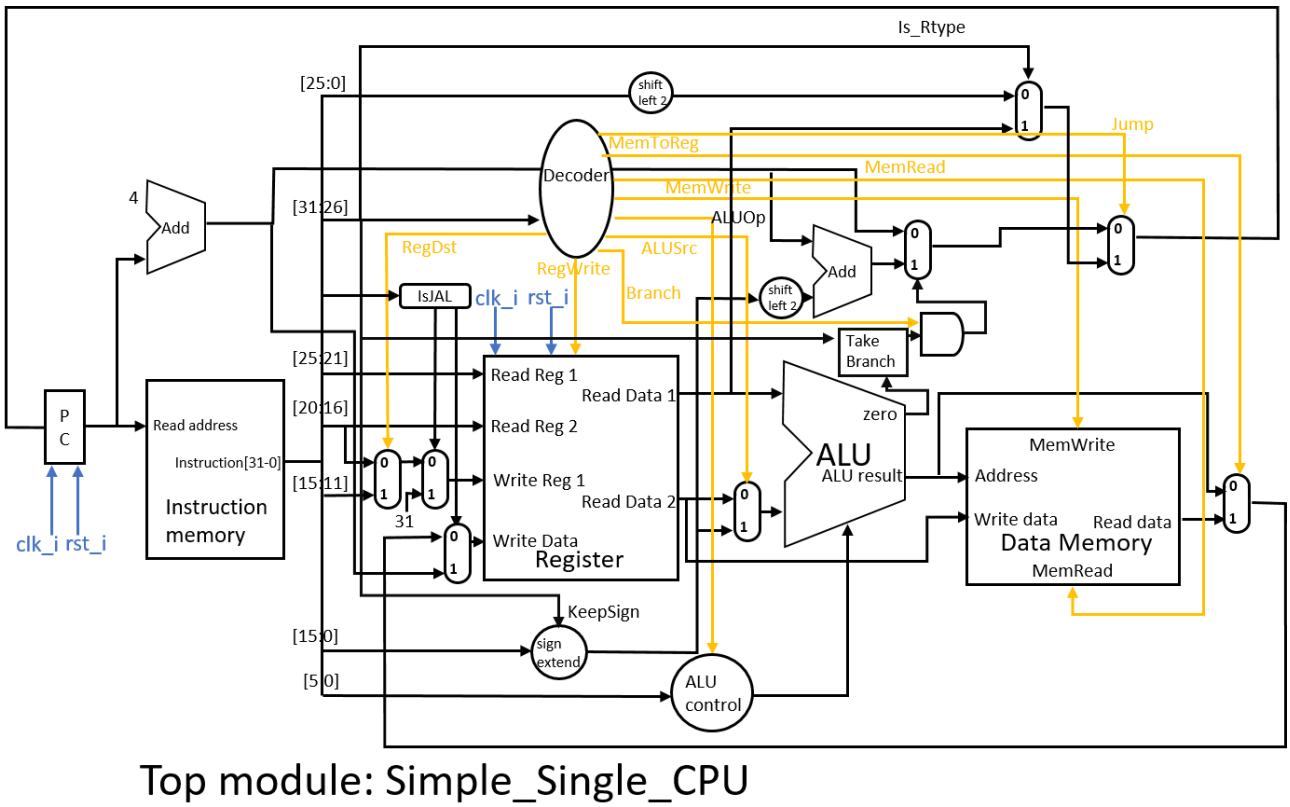
Architecture Diagram



Top module: Simple_Single_CPU

Detailed Description of the Implementation

Here are the major changes since Lab2:

1. A *Data_Memory* module was added, along with new signals *MemRead*, *MemWrite* and *MemToReg*.
   MemRead = 1, if instruction is LW.
   MemWrite = 1, if instruction is SW.
   MemToReg = 1, if instruction is LW.

2. Support for JAL and JR.
   JumpAddress = instruction[25:0] << 2, if instruction is R-type (JR).
   = Read Data 1, otherwise.
   Write the next instruction address to the 31st register if instruction is JAL.

3. Support for more Branch instructions.
   TakeBranch = inst[31:26] == 1 ? Less :
   (inst[31:26] == 4 ? Zero : // BEQ
   (inst[31:26] == 5 ? !Zero : // BNE
   (inst[31:26] == 6 ? (Less || Zero) : // BLE
   0)));

4. Added new ALU signal for MUL.

Problems Encountered and Solutions

1. I didn't fully understand how JAL and JR work until reviewing Chapter 2. The architecture illustrated in the handout of Chapter 4 is incomplete.
   Going over the second test case also helped me fully understand the instructions.

2. It took me quite some time to implement the Bubble Sort machine code. It was also difficult to debug since I wasn't sure whose fault was it (machine code or CPU).

Lesson Learned (If Any)

1. Lab4 looks scary …