Computer Organization Lab 1

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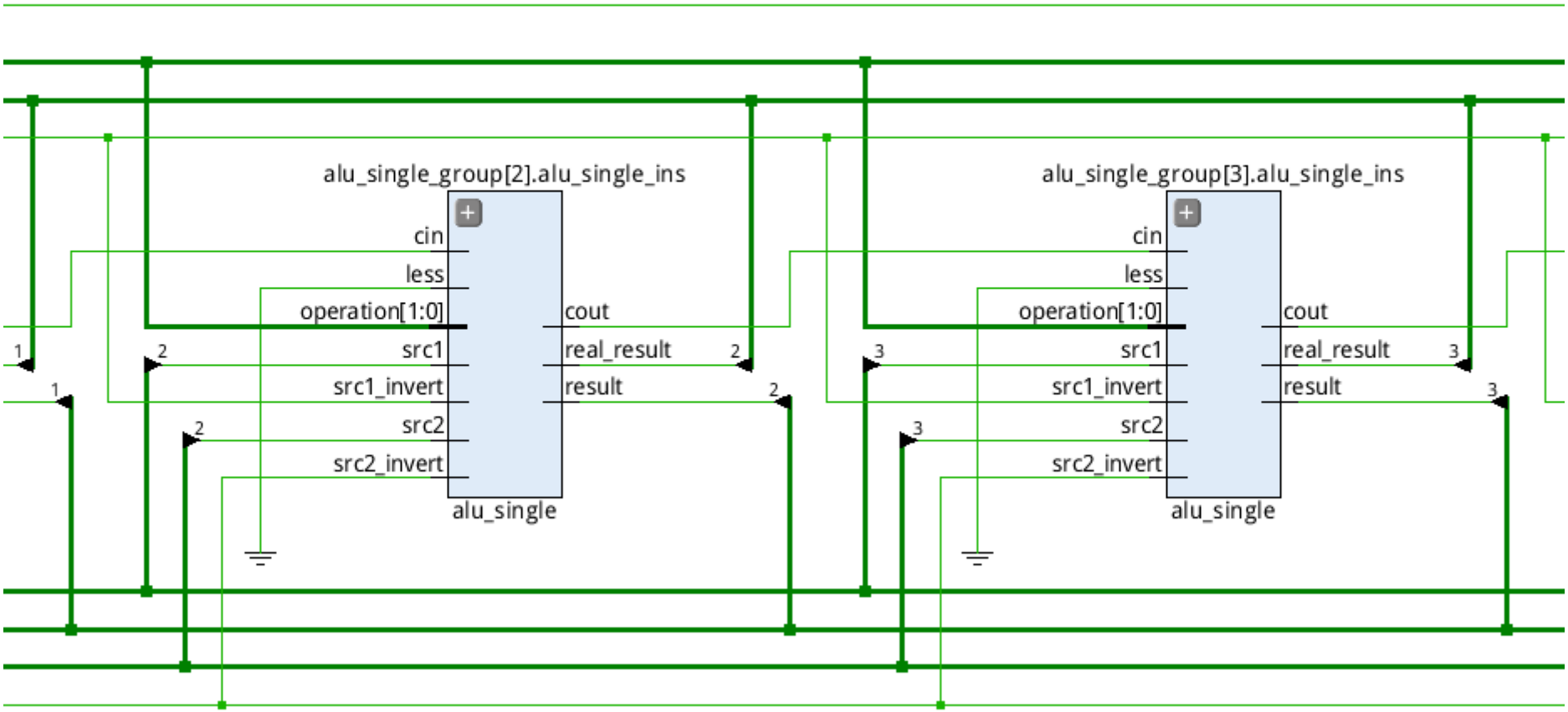
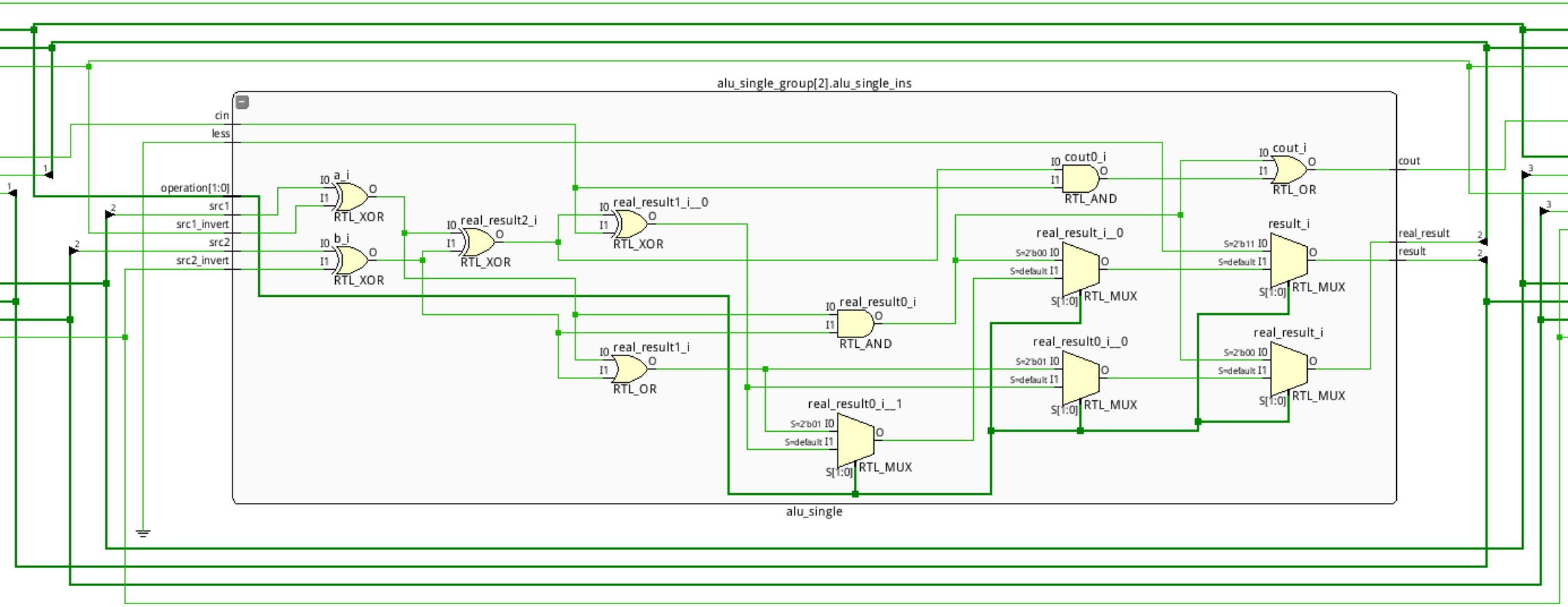
Architecture Diagram

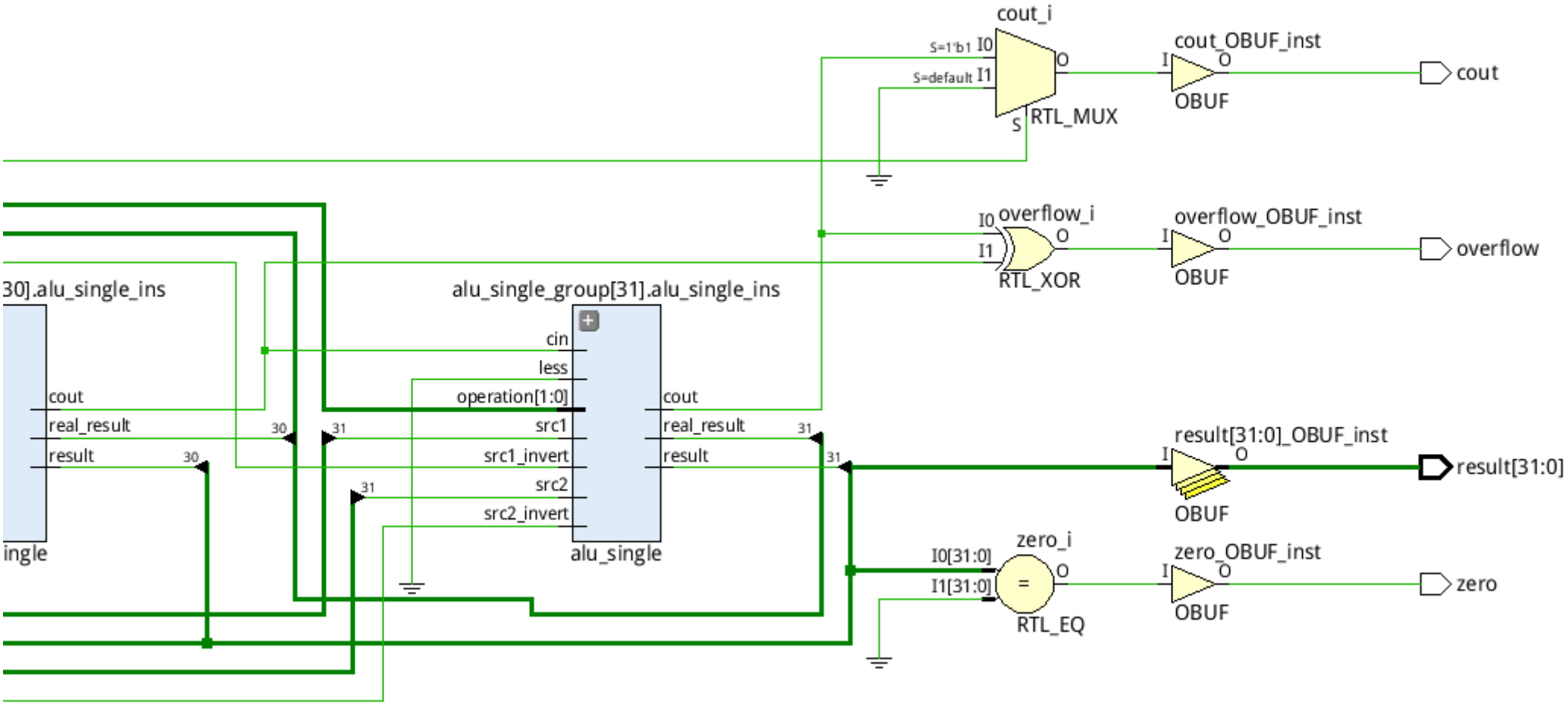
Schematic 1



Schematic 2


alu_single_group[2].alu_single_ins
cin
less
operation[1:0]
src1
src1_invert
src2
src2_invert
a_i
b_i
real_result2_i
real_result1_i__0
real_result1_i
real_result0_i
real_result0_i__1
cout0_i
real_result_i__0
real_result0_i__0
cout_i
result_i
real_result_i
RTL_XOR
RTL_AND
RTL_OR
RTL_MUX
cout
real_result
result
alu_single

Schematic 3


cout_i
S=1'b1 I0
S=default I1
O
S
RTL_MUX
cout_OBUF_inst
I
O
OBUF
cout
overflow_i
I0
I1
O
RTL_XOR
overflow_OBUF_inst
I
O
OBUF
overflow
30].alu_single_ins
cout
real_result
result
30
ingle
alu_single_group[31].alu_single_ins
cin
less
operation[1:0]
src1
src1_invert
src2
src2_invert
alu_single
cout
real_result
result
31
31
31
31
result[31:0]_OBUF_inst
I
O
OBUF
result[31:0]
zero_i
I0[31:0]
I1[31:0]
=
O
RTL_EQ
zero_OBUF_inst
I
O
OBUF
zero

Detailed Description of the Implementation

Nunc id quam a ex accumsan rhoncus. Vestibulum ut est non metus porttitor ullamcorper hendrerit sed nibh. Proin suscipit malesuada magna, a faucibus ipsum accumsan quis. Nulla facilisi. Phasellus massa risus, elementum non diam at, dapibus cursus eros. Nullam efficitur tortor id ipsum molestie, et condimentum felis congue. Donec aliquet efficitur elit at rutrum. Praesent aliquam dui eu tincidunt tempor. Curabitur vitae mi posuere, mollis leo a, molestie nisl. Sed aliquet libero eu volutpat tincidunt. Vivamus posuere mauris ipsum, nec condimentum tortor tempus rutrum.

Problems Encountered and Solutions

Sed non ullamcorper orci, in blandit eros. Sed ultricies augue tempus, malesuada erat eget, porta dui. Donec eu faucibus purus, sed auctor turpis. Pellentesque dictum enim eros, in bibendum libero lacinia et. Vestibulum neque metus, molestie eget mauris id, placerat vulputate neque. Duis tristique ultricies pretium. Vivamus vel pharetra nisi, et finibus tellus. Etiam vitae metus eu mauris fringilla dapibus.

Lesson Learned (If Any)

I. 肝毋好，人生係黑白的；
   肝若好，作業係空白的。

II. Verilog 2001 added the `generate` block, which is very handy to instantiate an abundance of modules.

III. Xilinx Vivado Design Suite is much more powerful than its legacy EDA tool – Xilinx ISE Design Suite.