Computer Organization Lab 4

0113110 Po-han Chen (Lab1, Lab2, Lab3), 0316213 Yu-wen Pwu (Lab1, Lab4)

Detailed Description of the Implementation

My implementation is based on the works in the previous Lab. The main difference is that we store signals in registers this time, so that we can use them in the next clock cycle (i.e. the next stage).

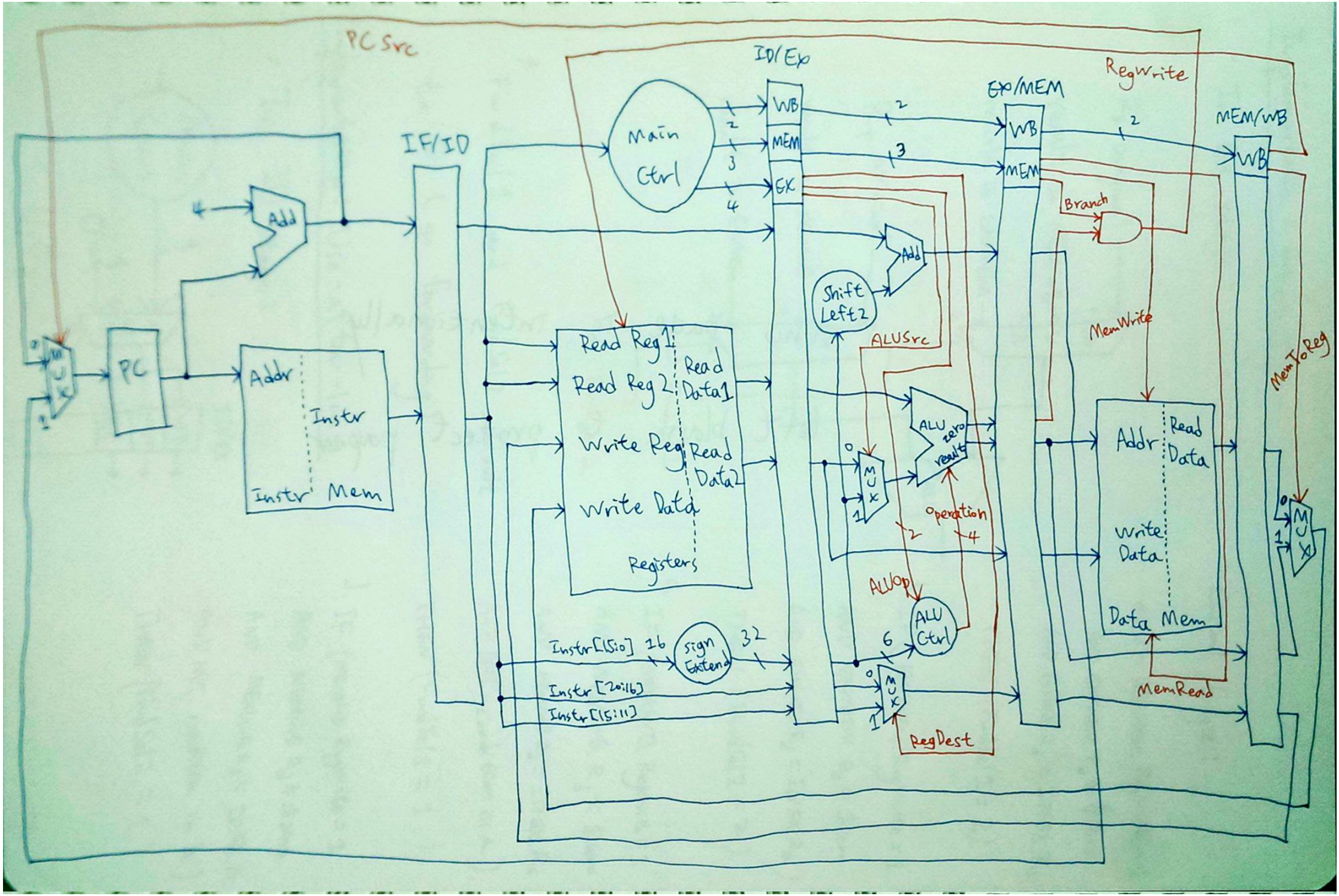
Problems Encountered and Solutions

It is possible to write to a register and read from that register at the same time. So we cannot update registers only at positive clock edges. Instead, we should update registers at all time.

Lesson Learned (If Any)

I hope there will be no more Labs. I only have 86,400 seconds a day! I don't have enough time to do these crazy assignments. So sad :(

Architecture Diagram


PC Src
ID/Ex
RegWrite
EX/MEM
MEM/WB
IF/ID
Main Ctrl
WB
MEM
EX
Add
4
PC
Addr
Instr
Instr Mem
Read Reg 1
Read Reg 2
Write Reg
Write Data
Read Data 1
Read Data 2
Registers
Shift Left 2
Branch
ALUSrc
MemWrite
MemToReg
ALU
zero
result
operation
ALUOp
ALU Ctrl
Instr[15:0]
16
sign Extend
32
Instr[20:16]
Instr[15:11]
6
RegDest
Data Mem
MemRead
MUX