Ve370 Introduction to Computer Organization
Project 2

PROJECT DESCRIPTION

Model both single cycle (individual work) and pipelined implementation (team work) of MIPS computer in Verilog that support a subset of MIPS instruction set including:

- The memory-reference instructions load word (`lw`) and store word (`sw`)
- The arithmetic-logical instructions `add`, `addi`, `sub`, `and`, `andi`, `or`, and `slt`
- The jumping instructions branch equal (`beq`), branch not equal (`bne`), and jump (`j`)

Use Figure 1 as a top-level block diagram of your single cycle implementation and Figure 2 for the pipelined structure. Note: there may be some components and control signals omitted from the figures that you will have to add to support all instructions listed above. Forwarding and Hazard Detection should be implemented in the pipelined structure to handle hazards. (*source: Computer Organization and Design, by Patterson and Hennessy, Morgan Kaufmann Publishers*)

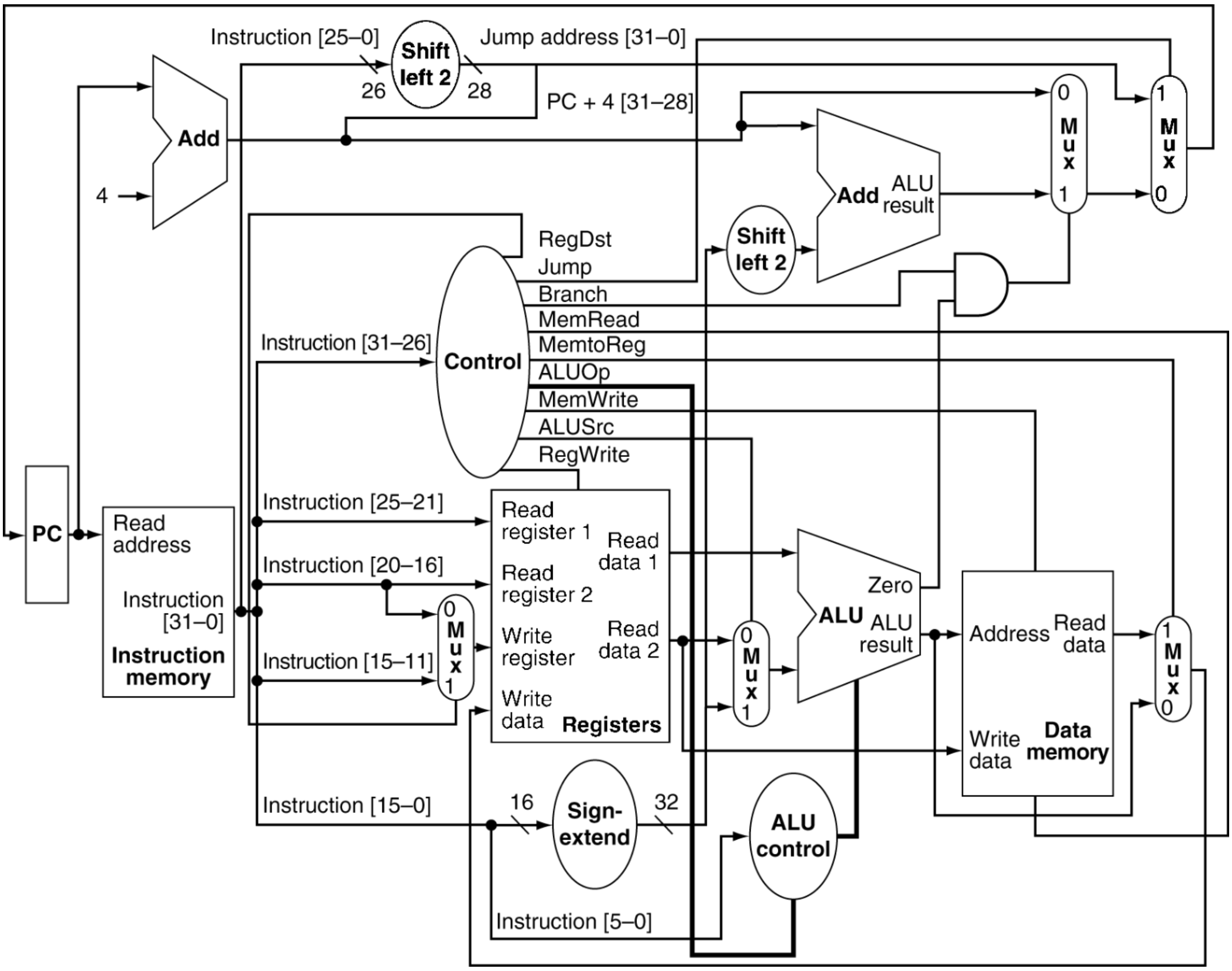

Figure 1. Single cycle implementation of MIPS architecture

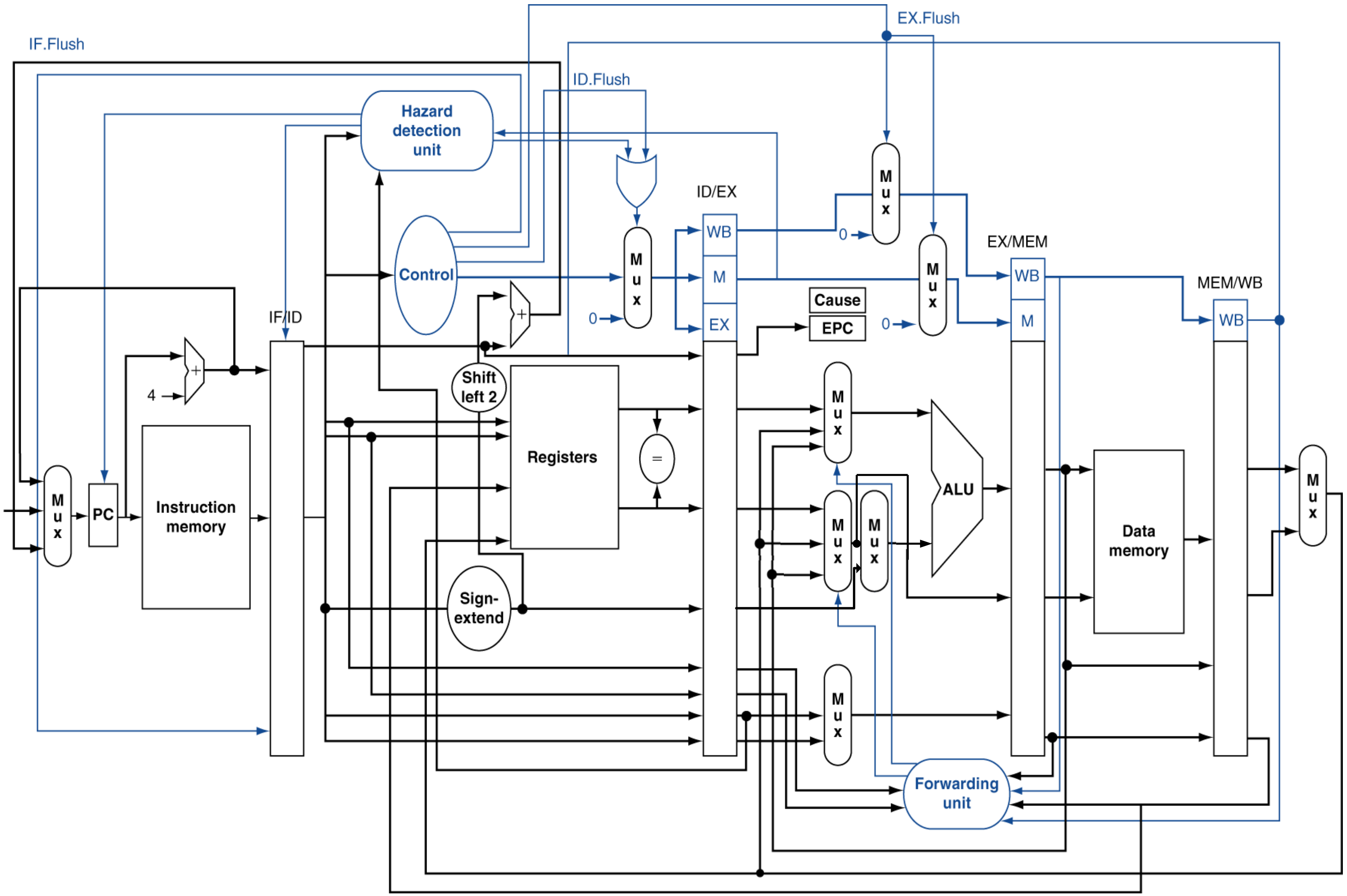

Figure 2. Pipelined implementation of MIPS architecture

PROJECT REQUIREMENTS

This project must be modeled and simulated in Verilog HDL and synthesized by using Xilinx synthesis tool. A simple MIPS assembly program using the supported instructions will be provided to you to verify that the processor can execute those instructions continuously and correctly.

Every student is required to model a single cycle processor individually. An individual written report should be submitted to show simulation results and source codes. FPGA implementation of the single cycle processor is NOT required.

Every team should then model and implement a pipelined processor together. The team must implement the pipelined processor in the Xilinx FPGA meeting the following requirements:

- Error free in the simulation
- Be able to demonstrate on the FPGA board
- Demonstration results must coincide with your simulation results
- Demonstrate before the specified deadline.

TEAM ORGANIZATION

The part of pipelined processor shall be team work. Each team is composed of 4 students, randomly grouped. The work should be appropriately divided and distributed among all team members. Students are not allowed to switch teams unless approved by the instructor.

DELIVERABLES

All deliverables should be submitted electronically on Canvas. The project must be demonstrated to the teaching group.

- **Team report** – The team report should be a written report. One submission is required for each team and should be submitted electronically by one of the team members. Make sure names of all team members are clearly shown on the cover page of the report. The report must include:
    1) Elaborated description of all aspects of the modeling and implementation of the pipelined processor;
    2) Screen shots and explanations of simulation results. This will help you to earn partial credits if a project is not completed;
    3) RTL schematic of your Verilog design generated with Xilinx Vivado software;
    4) All your Verilog source files and any other files, as appendix.
- **Individual report** – The individual report should include:
    1) Screen shots of simulation results for each type of instruction (sw, lw, add, beq, etc.);
    2) Verilog source files
    3) Peer evaluation describing your own contribution to the lab as well as contributions of every other team member, as explained below.

GRADING

- Individual report: 30%
- Team effort: 70%, including
    - Working Verilog model (simulation): 20%
    - Team report: 20%
    - Working FPGA implementation: 30%

PEER EVALUATION

Each team member is required to provide a peer evaluation for the team effort of Project 2. The marks of the peer evaluation should be integers ranging between 0 to 5, inclusively, with 5 indicating the biggest contribution. A mark should be given to each team member including yourself according the team member's contribution based on your observation. A brief description of contribution of each team member should also be provided, as shown in the following table.

Name	Level of contribution (0 ~ 5)	Description of contribution
(yourself)		
(your lab partner)		
(your lab partner)		
(your lab partner)		

Additionally, the teaching team (instructor and/or TAs) will give an oral examination to each team member during the demonstration. We will ask some basic but important questions related to the project. Basing on your answers, we will give an evaluation mark, ranging in between 0 to 5 as well.

An average mark for individual contribution of each student is calculated as:

Individual_Average = (sum of all team member's marks + teaching team's mark * 2) / (size of the student team + 2)

A group average is calculated as:

Group_Average = sum of Individual_Average of all team members / size of student team

Then we calculate a difference ratio with the following equation:

Individual_Difference = Individual_Average / Group_Average – 1.0

Using the calculated Individual_Difference, we find a factor from the following lookup table.

Individual_Difference	Factor	Individual_Difference	Factor
>=0 and < +10%	1.0	> -10% and < 0	1.0
>= +10% and < +20%	1.1	> -20% and <= -10%	0.9
>= +20% and < +30%	1.2	> -30% and <= -20%	0.8
>= +30%	1.3	<= -30%	0.7

Your final Project 2 grade is calculated as:

Final grade of Project 2 = points for Individual report + points for team effort * factor

The final grade of Project 2 will not exceed the maximum points assigned to the project.

DUE DATE

The project report and all required source code are due by **11:59pm, November 5, 2020**
Demonstration is due by **6:00pm, November 6, 2020**

BONUS

The data hazards involving `beq` instruction are not required to be resolved in Project 2. For example:

```
lw $8, 0($9)
beq $8, $0, LOOP
```

or

```
and $8, $9, $10
beq $8, $0, LOOP
```

Students who can resolve this kind of data hazard using **as much of forwarding as possible and as few stalls as possible (all in hardware)** will receive 5 bonus points added to the overall Project 2 grade, providing the basic requirements of Project 2 are all satisfied.