1. **Describe the input fields of each pipeline register**
2. IF/ID pipeline register
   1. [63:32]: PC+4
   2. [31:0]: current instruction
3. ID/EX pipeline register(190 bits):
   1. [189:188]: control lines for WB stage(RegWrite, MemtoReg)
   2. [187:185]: control lines for MEM stage(Branch, MemRead, MemWrite)
   3. [184:181]: control lines for EX stage(RegDst, ALUOp, ALUsrc)
   4. [180:149]: PC+4
   5. [148:117]: RSdata
   6. [116:85]: RTdata
   7. [84:53]: extendData
   8. [52:21]: zeroData
   9. [20:0]: last 20 bits of current instruction
4. EX/MEM register(139 bits):
   1. [138:137]: control lines for WB stage(RegWrite, MemtoReg)
   2. [136:134]: control lines for MEM stage(Branch, MemRead, MemWrite)
   3. [133:129]:write register number(RegAddrTemp)
   4. [128:97]:pc of branch instruction(pc\_branch)
   5. [96:65]: input address to data memory(RegData)
   6. [64:33]: RTdata
   7. [32:1]: PC+4
   8. [0]: zero output from ALU(zero)
5. MEM/WB register(71 bits):
   1. [70:69]: control lines for WB stage(RegWrite, MemtoReg)
   2. [68:37]: MemData
   3. [36:5]: input address to data memory(RegData)
   4. [4:0]: write register number(RegAddrTemp)

2. Explain your control signals in the sixth cycle(both test data test\_1.txt

and test\_2.txt are needed)