Camera & LCD Implementation

Main solution:

- Camera Part:
  - Camera mode control;
  - Transform camera data to LCD data form;
  - Transfer data to memory

- LCD Part:
  - LCD configuration
  - Transfer data from memory to display picture on LCD

reported by:
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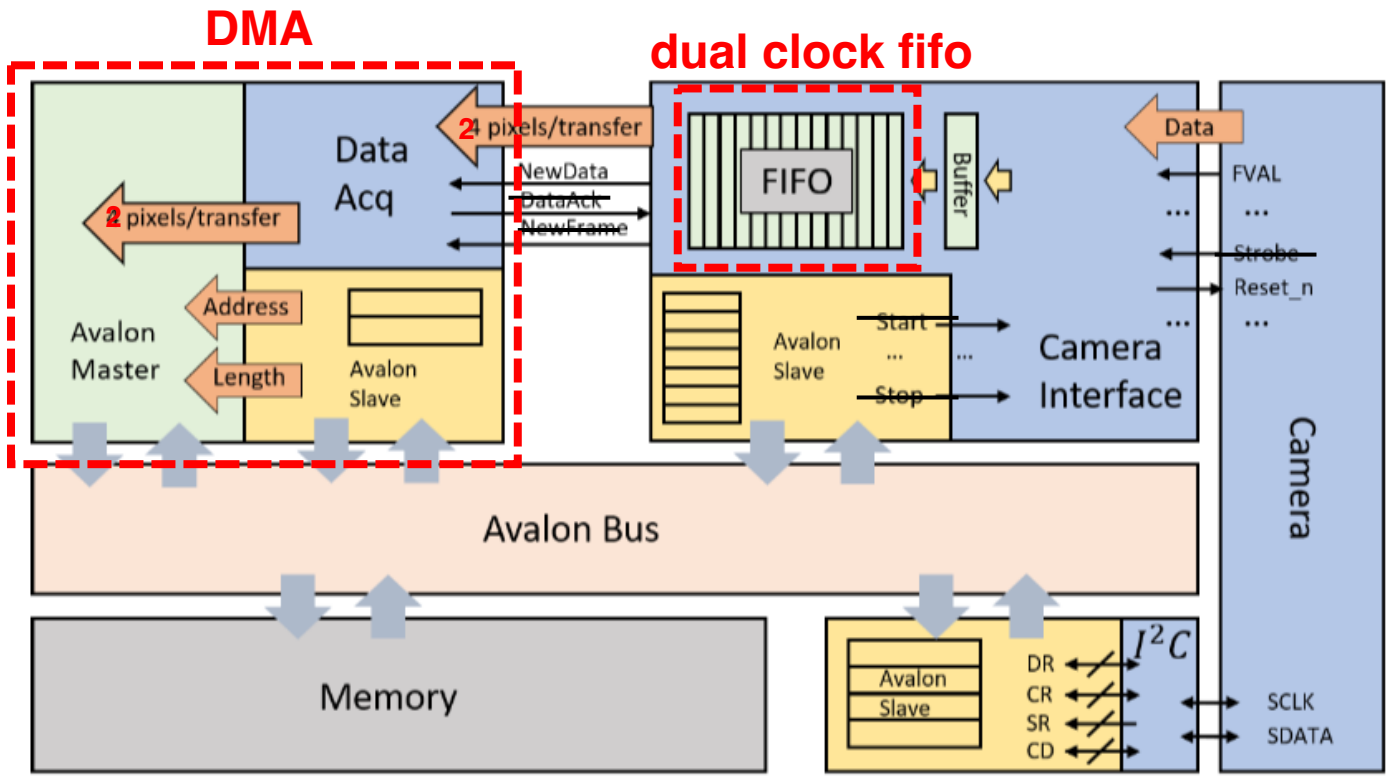
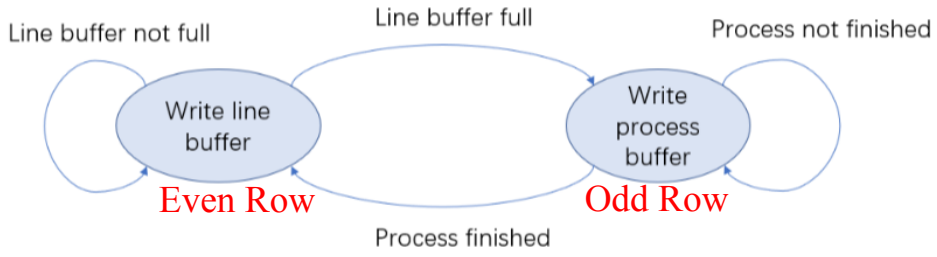
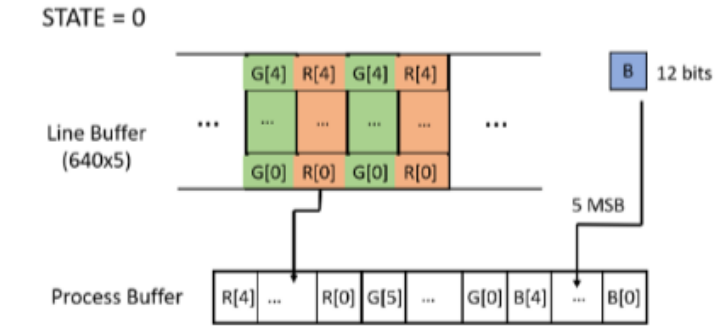
Camera TRDB_D5M Implementation Module

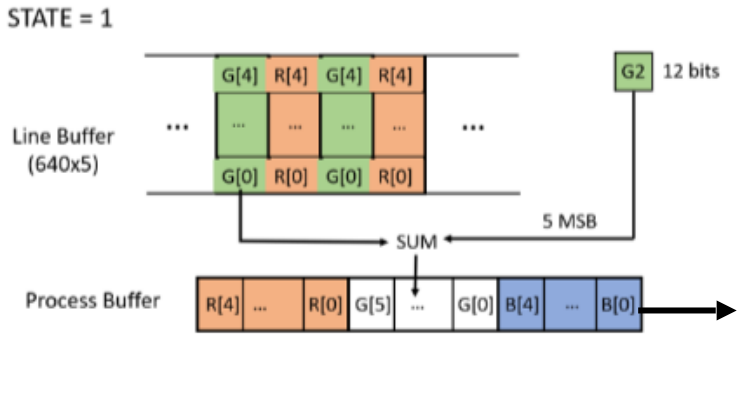


- **Avalon Master**
  - 2 pixels in 32 bits;
  - burst transfer;
- **Dual clock FIFO**
  - read clock from fpga;
  - write clock from camera;
  - 16-bit in, 32-bit out;
- **Camera configuration**
  - with I2C;
  - 2x binning, not snapshot mode;
  - row size = 240, column size = 320;
  - no trigger/strobe signals used.

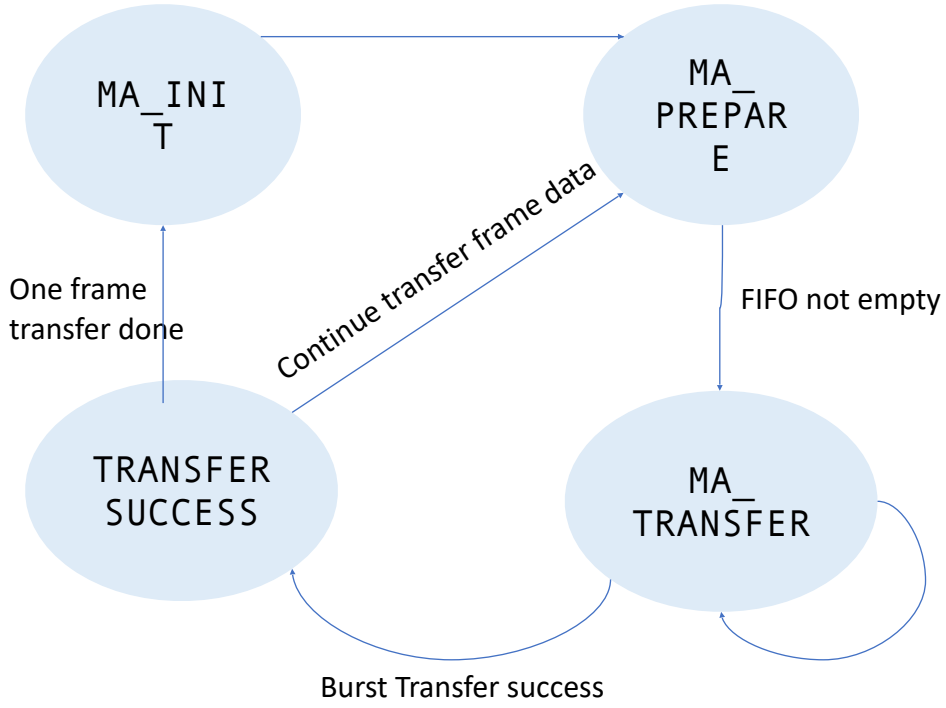
Camera TRDB_D5M Writing to Memory





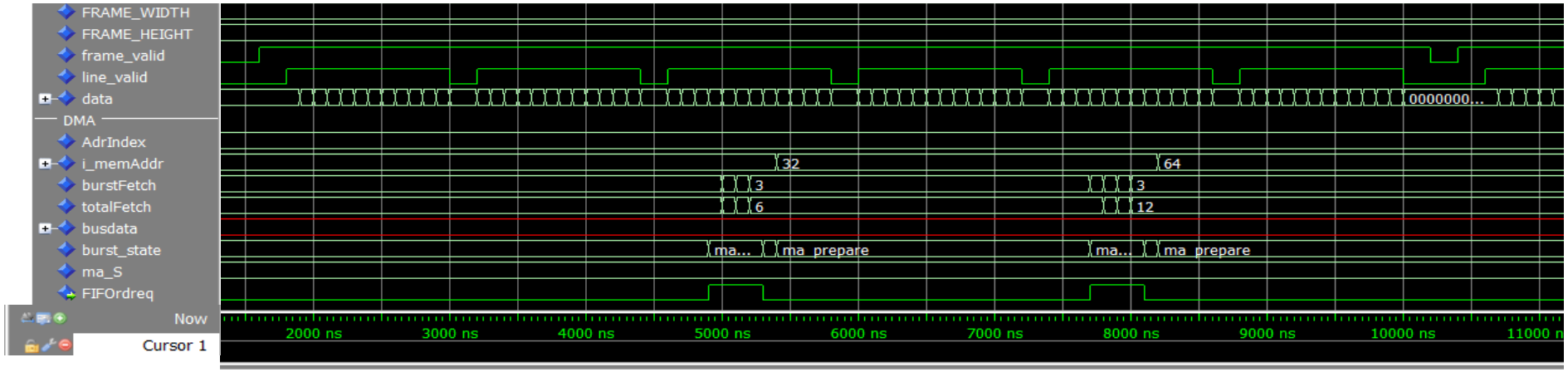


- Row and column states alternates between odd and even (index starting from 0);
- Write to FIFO when data in process buffer is ready.
- Burst transfer to memory when there is enough data.

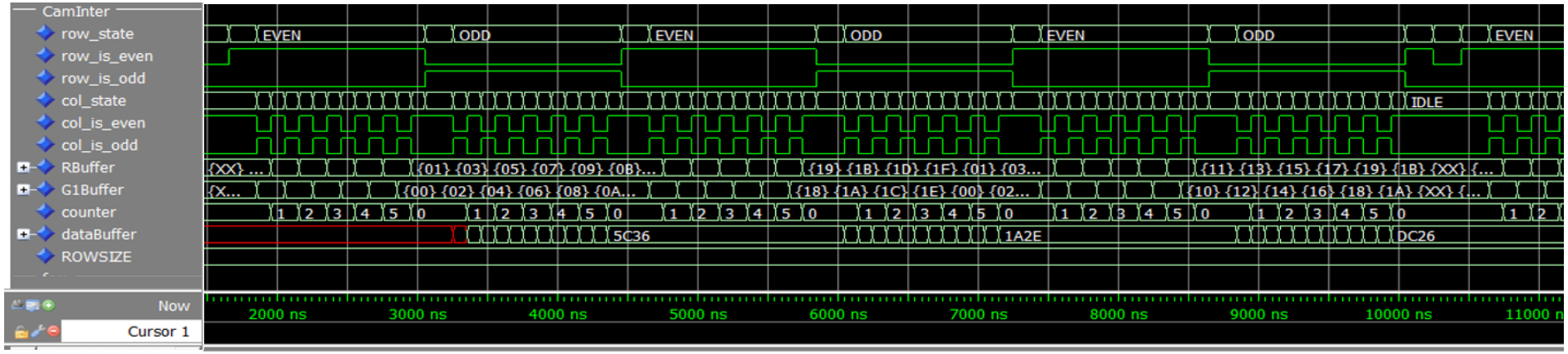


Camera TRDB_D5M Modelsim Simulation

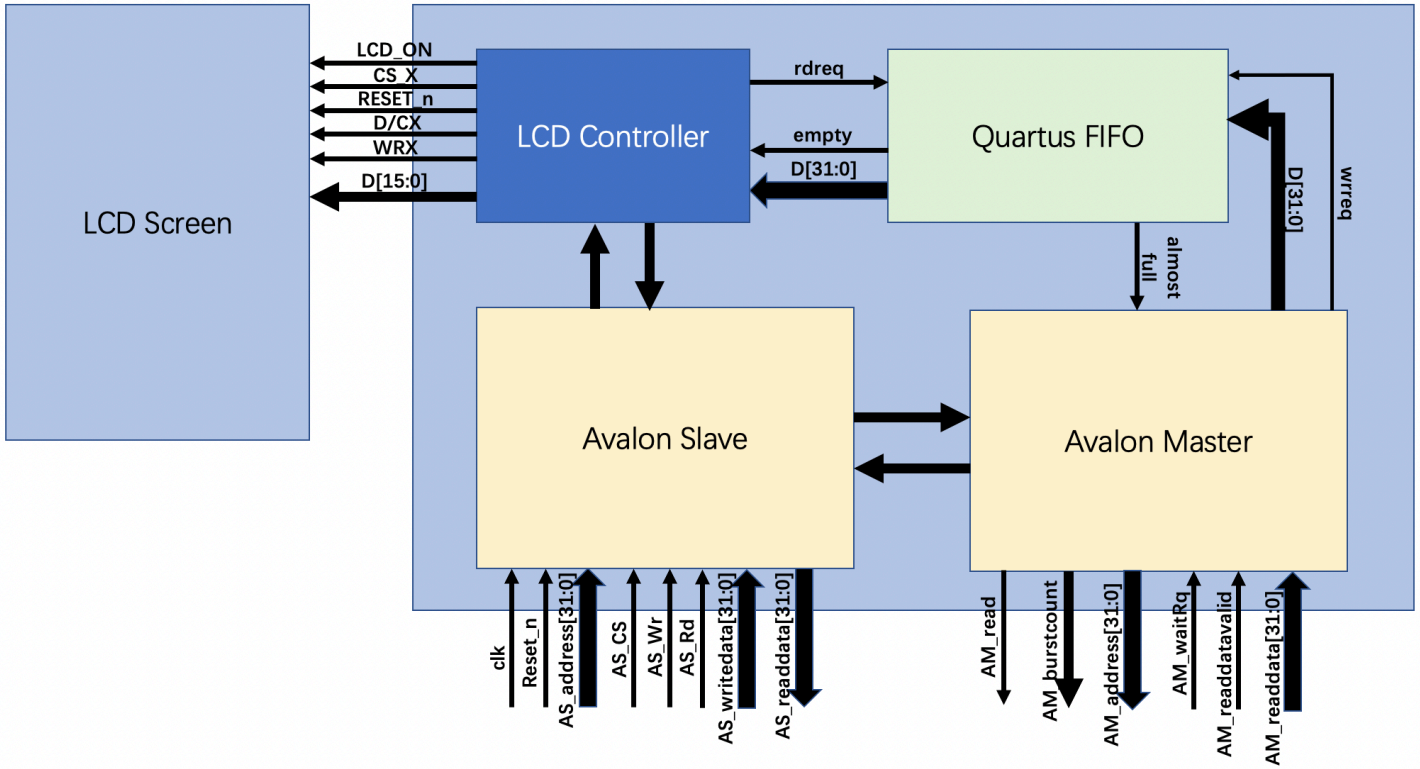
- **Avalon Master signals**



- **Camera interface signals**



LCD LT24 Implementation Module



- CPU operates R/W on Avalon Slave
- Avalon Master data fetch controlled by register written by Slave
- Fetched data stored in FIFO if not full
- Data transmission controlled by LCD controller

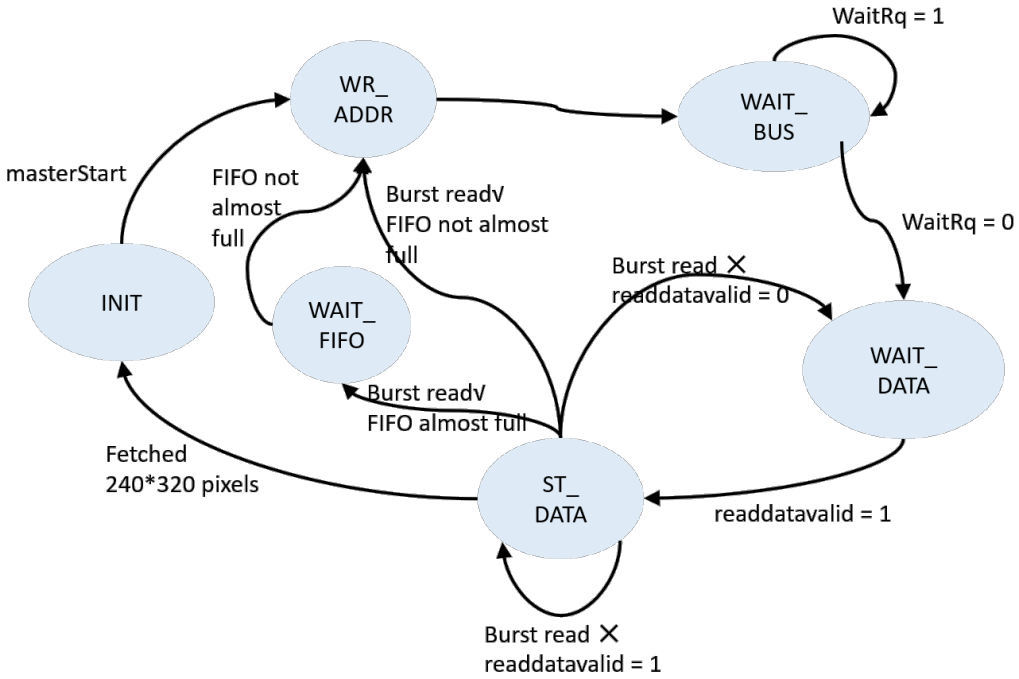
Avalon Slave & Master for LCD

All registers are R/W registers

For LCD control

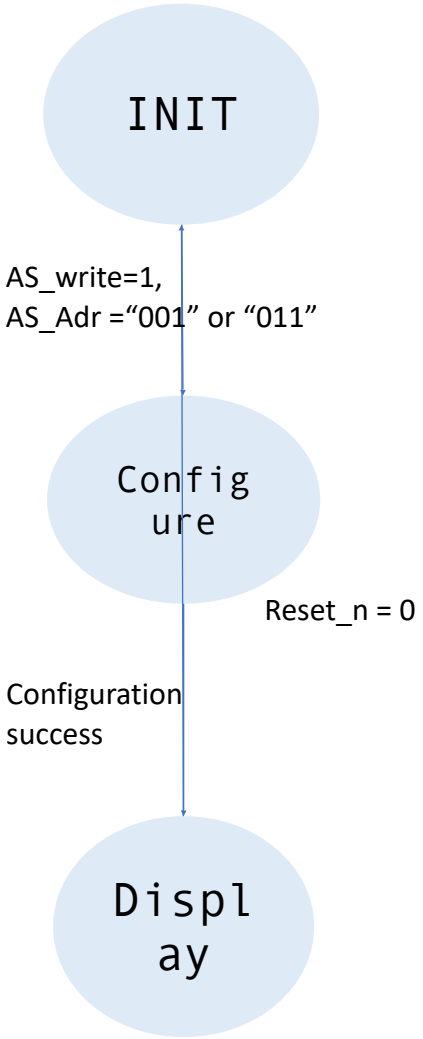
For Master

Avalon Slave register	Address	Description
RESET_Reg	000	RESX control
LCDAdr	001	Register address for Configuration
SlaveData	011	Data for Configuration
ConfOK	101	Configuration finished
Masterstart	010	Data Ready! Start Fetch
memaddr	100	Start address for Master

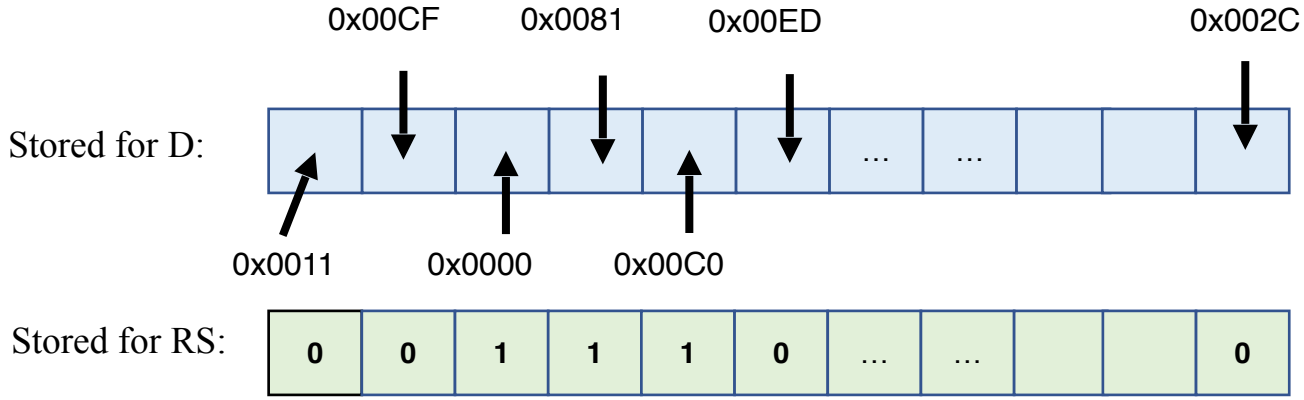


States	Description
INIT	Initial state
WR_ADDR	Issue read request to the Avalon Bus
WAIT_BUS	Wait until bus available
WAIT_DATA	Wait until data available
ST_DATA	Store pixel to FIFO
WAIT_FIFO	Wait until FIFO has space

LCD Controller



Do nothing

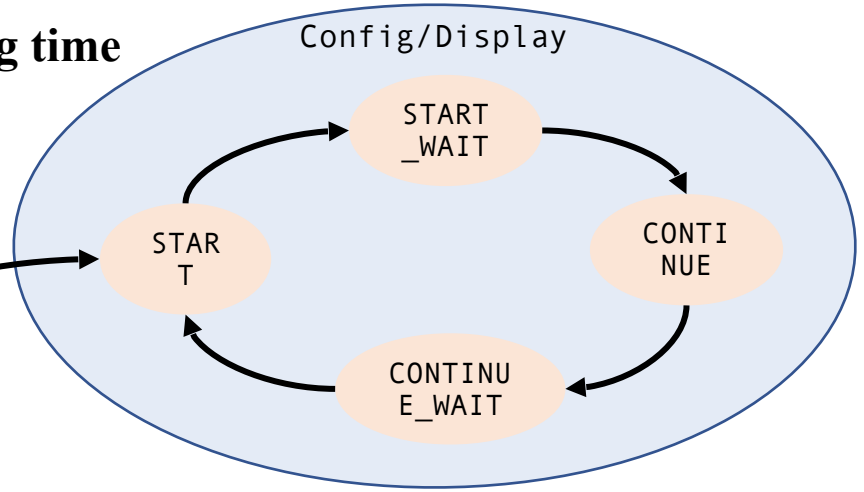


Store all the command addresses and data

If ConfOK = 1, start configuration

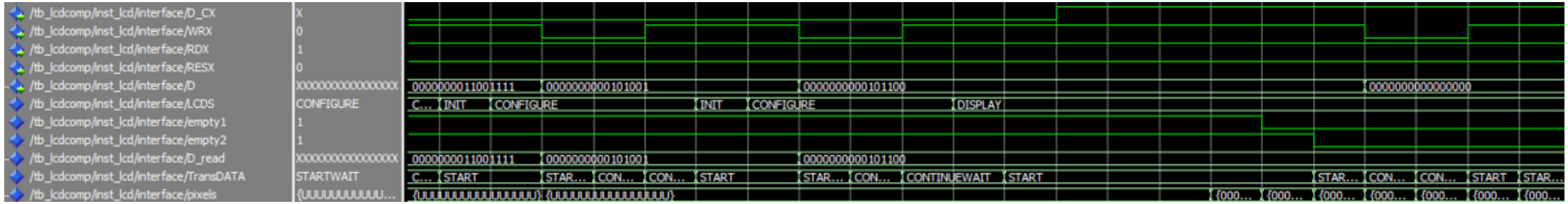
Configure: 4-State Loop for WRX maintaining time

4-State Loop for WRX maintaining time

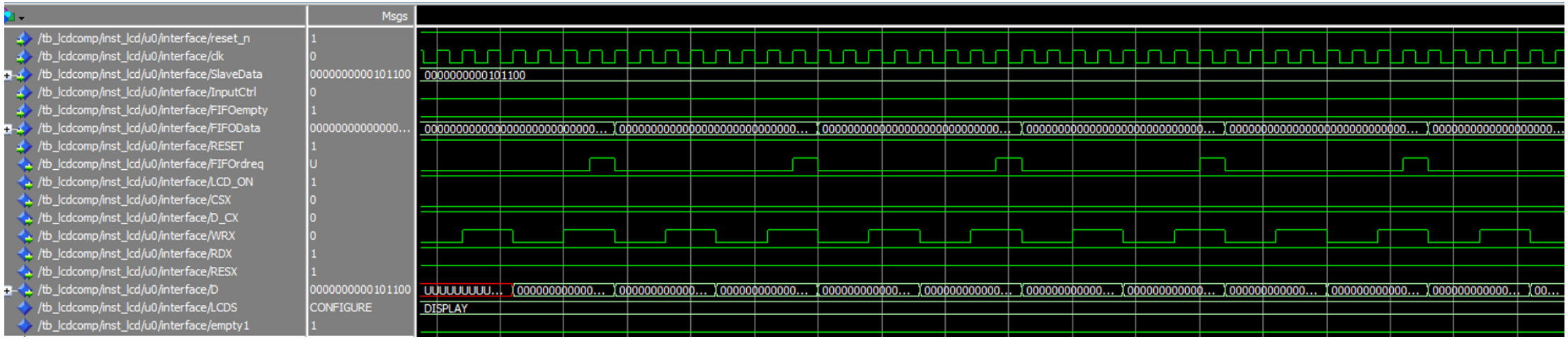


LCD ModelSim Simulation

LCD Configure Correct in Simulation

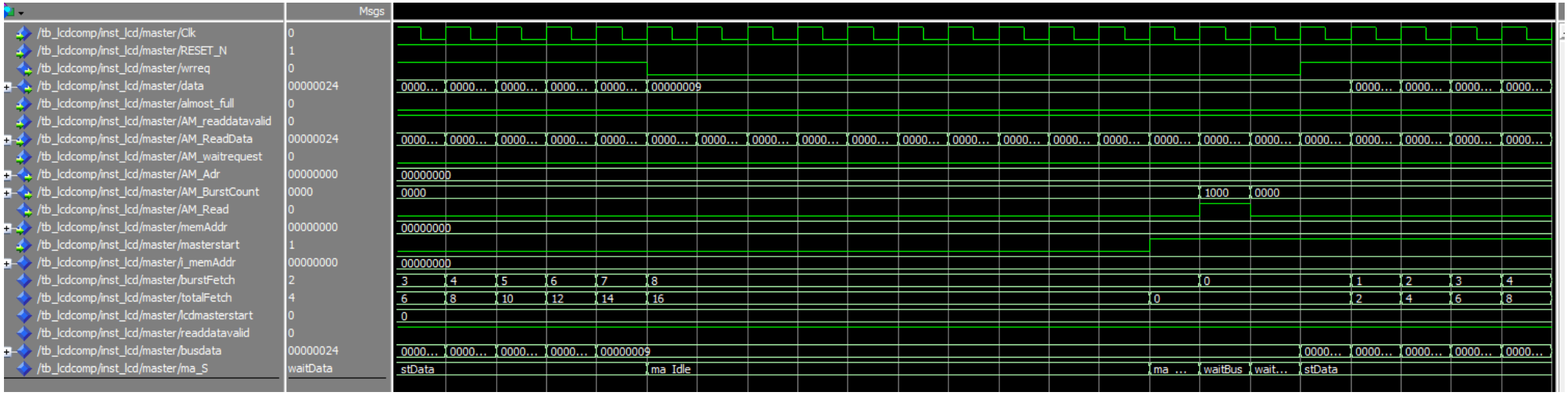


LCD Display Correct in Simulation



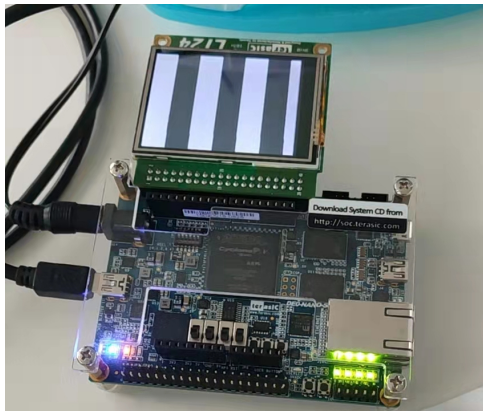
LCD ModelSim Simulation

LCD Master Unit Correct in Simulation

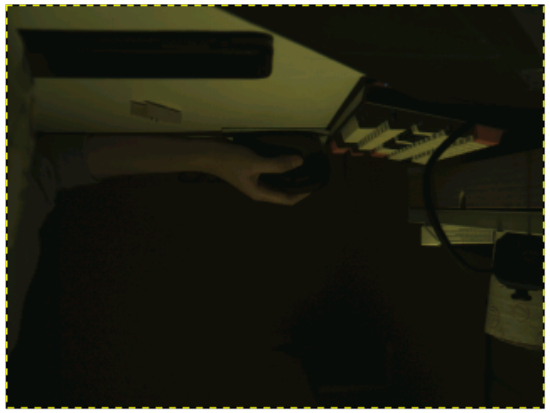


On Board Experiments

LCD



Camera



IOWR/RD offset should match the slavedata width

AS_WriteData width = 32 bit

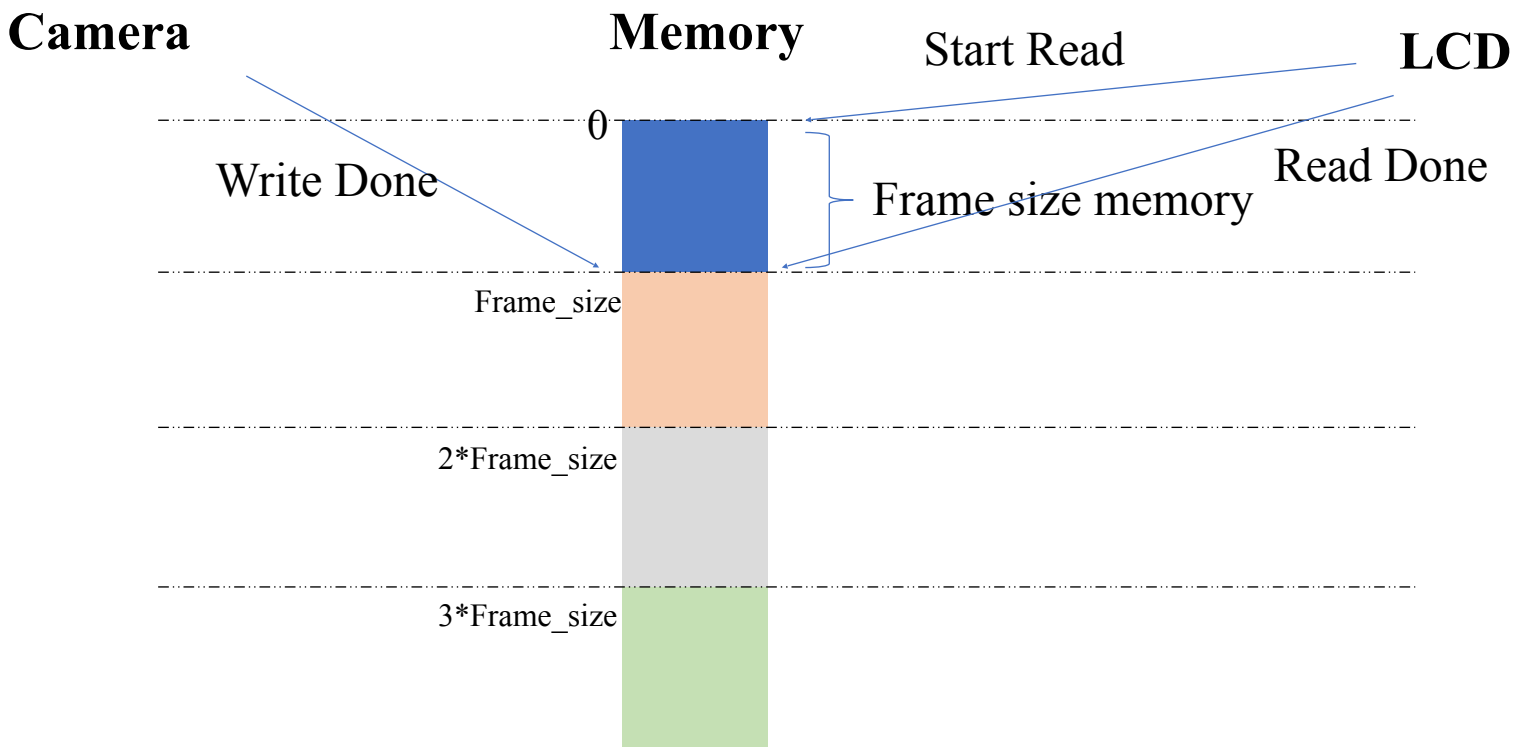
Original

Register	IOWR/RD
00	00
04	04

Correct

Register	IOWR/RD
00	00
01	04

System Implementation & DEMO



Demo