HW4 report

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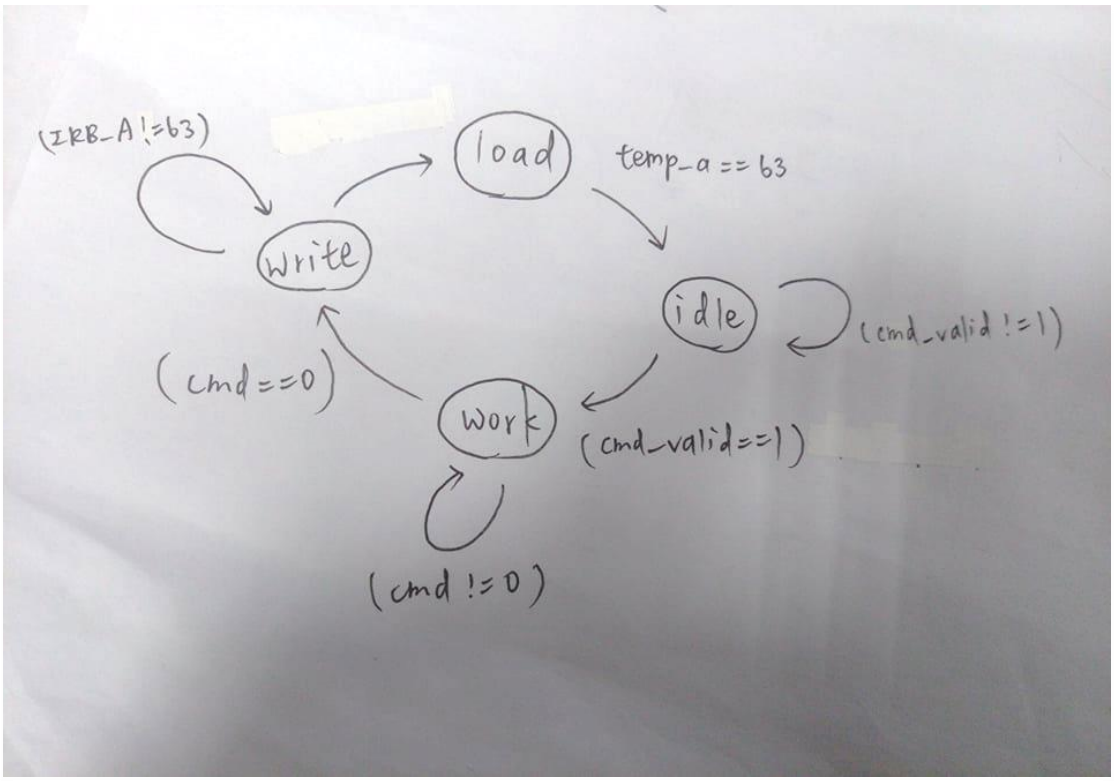
1、 Design principle :



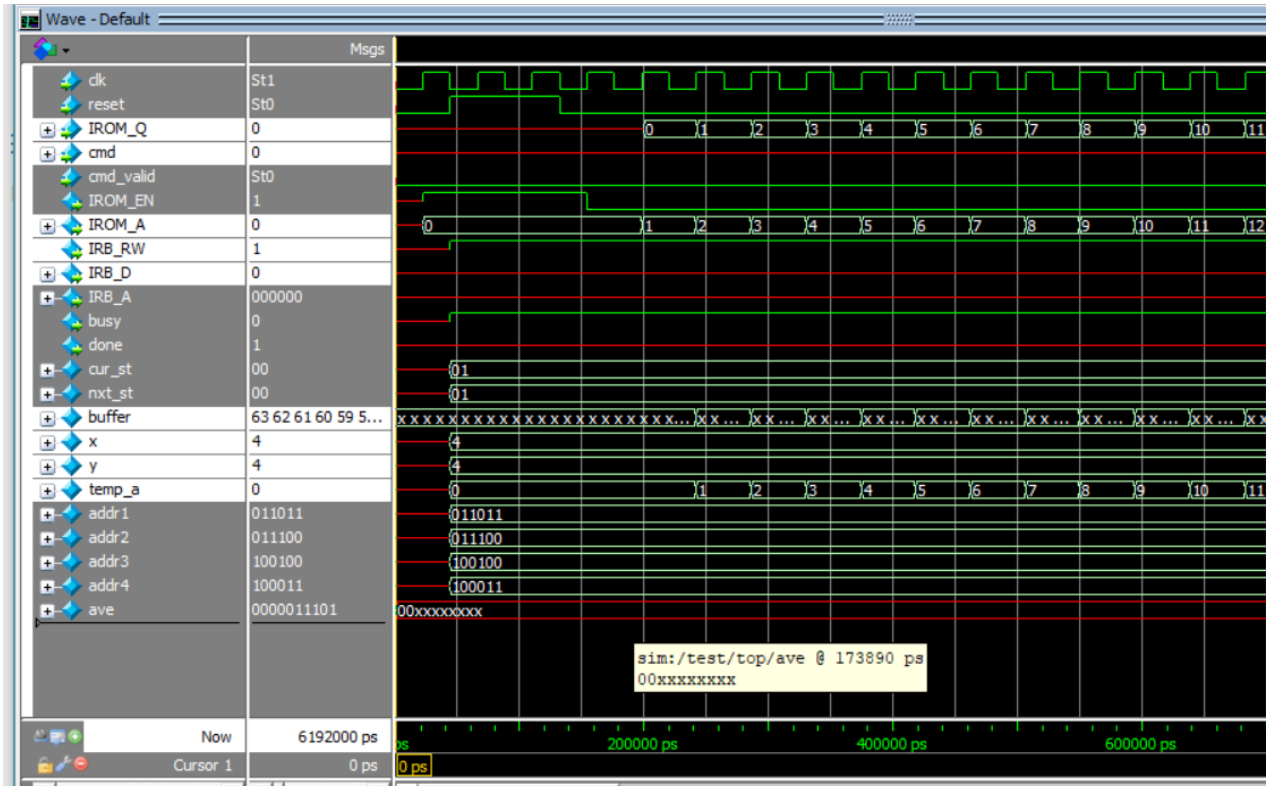
設 reg x,y 作為座標，以 x,y 得出上下左右四個位置

(8y+x)-9	(8y+x)-8
(8y+x)-1	(8y+x)

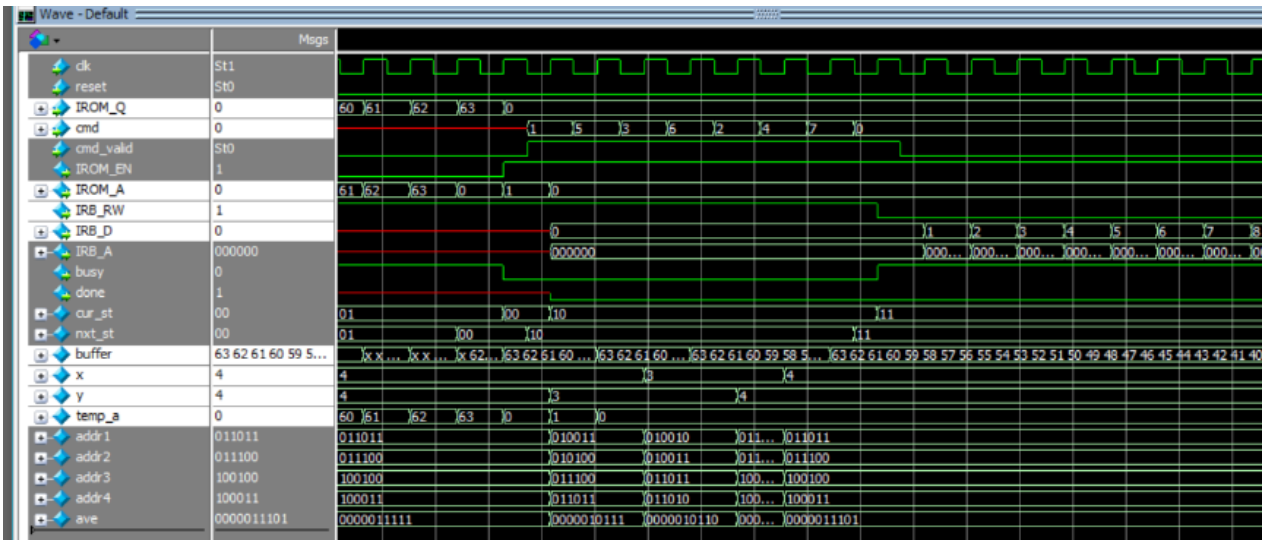
(x,y)

2、 pre-sim 波形圖

load state



work state & write state

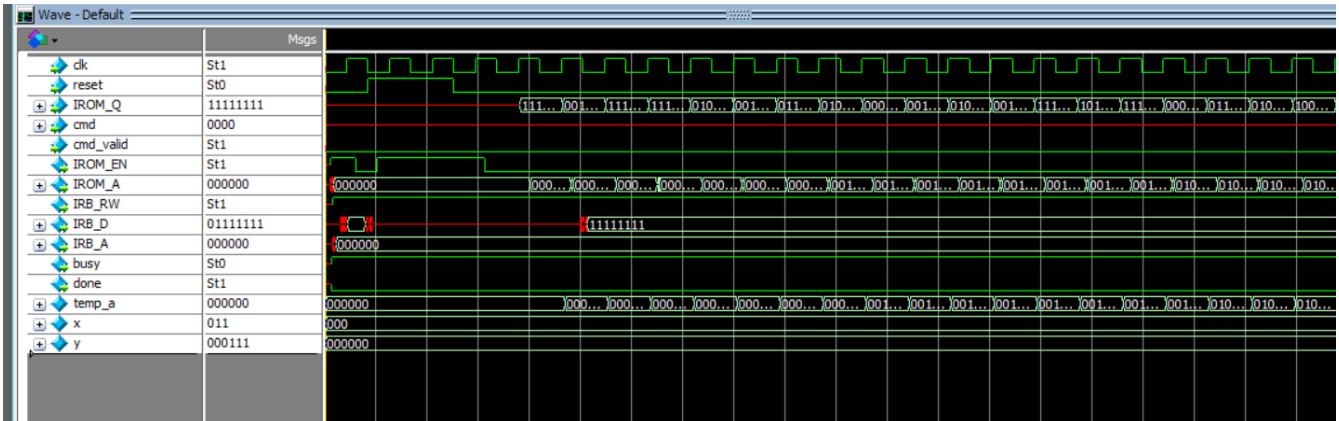


3、 flow summary result

Flow Summary

Flow Status	Successful - Fri Dec 21 19:21:12 2018
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	LCD_CTRL
Top-level Entity Name	LCD_CTRL
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	7,385 / 68,416 (11 %)
Total combinational functions	7,385 / 68,416 (11 %)
Dedicated logic registers	545 / 68,416 (< 1 %)
Total registers	545
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

4、 pos-sim 波形圖



5、 minimum CYCLE in post-sim : 42

6、 gate level Simulation

通過測資截圖如下: