HW1 report

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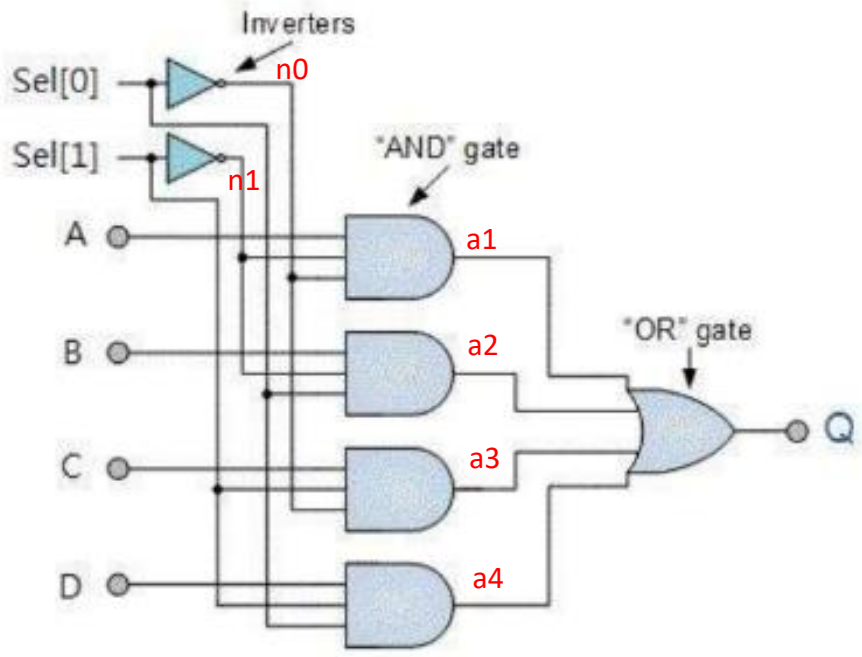
1、 Design principle

依照作業給的 Gate-level structure 來設計。



2、flow summary result

Flow Summary

Flow Status	Successful - Fri Nov 02 15:45:46 2018
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	mux
Top-level Entity Name	mux
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	2 / 68,416 (< 1 %)
Total combinational functions	2 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	7 / 622 (1 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

3、minimum CYCLE in post-sim : 5

4、gate level Simulation

通過測資截圖如下: