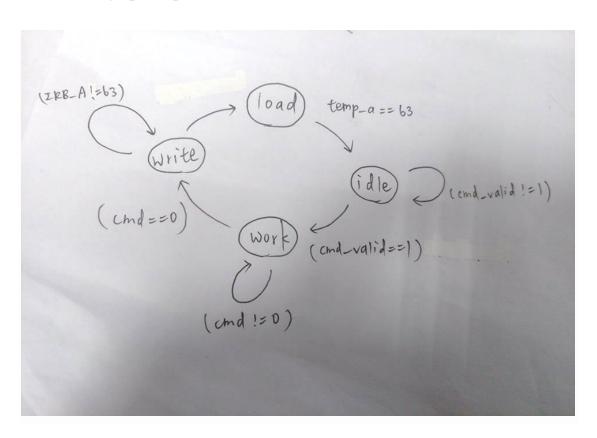
HW4 report

工科 109 黄郁雲 E94051136

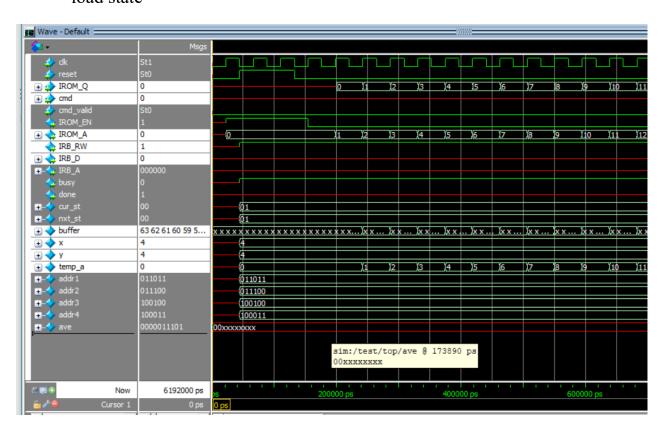
1 • Design principle:



設 reg x,y 作為座標,以 x,y 得出上下左右四個位置

(8y+x)-9	(8y+x)-8							
(x,	/)							
(8y+x)-1	(8y+x)							
,	,							

2、 pre-sim 波形圖 load state



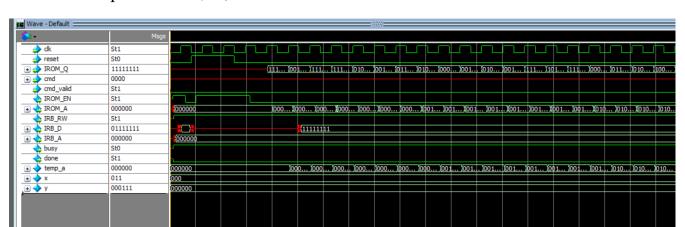
work state & write state

	Msgs																			
♠ dk	St1														$\overline{\Box}$		$\overline{\Box}$			
reset	St0															طاك	راك			
→ IROM_Q	0	60)61)62	63	(0)															
🕳 紣 cmd	0				1	15)3),5	2)4	7)								
cmd_valid	St0	\blacksquare																		
IROM_EN	1																			
→ IROM_A	0	61 62	63	(0)1)O														
♣ IRB_RW	1															4				
± 🔷 IRB_D	0					0							-)2	13	14)5)6	7	▇
IRB_A	000000					000000		-			_		000	1000	1000	1000)000.)000.	1000.	≖
busy .	0										-									
done	1										_									
cur_st	00	01		V)00	_		=		_	<u> </u>	111		=		#				
nxt_st	00	01		(00	(10		V			L	—	1								
◆ buffer	63 62 61 60 59 5	JX X	XX	Jx 62.)63 62	51 60	163 62 6	1 60 6	62616			261605	9 58 57 5	6 55 54	53 52	1 50 49	48 47	46 45 4	14342	116
• • x	4	4				Va		3	Va	(4	=						==			
● ❖ Y • ❖ temp_a	0	60 (51)62	(63	Va.)3)1	Vo)4							==	▆			
	011011	011011	/02	/ps	Nu .	01001		010010	Vo	1)(01	1011					==	▆			
B-4 addr2	011100	0111011				010100		010010		1)01	_					▆	▆			
o-4 addr3	100 100	100100				011100		011011		0 /10						▆	▆			
■-4 addr4	100011	100011				01101		011010		0 (10	_									
■- 4 ave	0000011101	000001	1111			00000		00000101			00011101					==	==			

3 · flow summary result

```
Flow Summary
   Flow Status
                                       Successful - Fri Dec 21 19:21:12 2018
   Quartus II Version
                                       10.0 Build 262 08/18/2010 SP 1 SJ Full Version
   Revision Name
                                       LCD_CTRL
   Top-level Entity Name
                                       LCD_CTRL
   Family
                                       Cyclone II
                                       EP2C70F896C8
   Device
   Timing Models
                                       Final
   Met timing requirements
                                       Yes
                                       7,385 / 68,416 ( 11 % )
 ☐ Total logic elements
      Total combinational functions
                                       7,385 / 68,416 ( 11 % )
      Dedicated logic registers
                                       545 / 68,416 ( < 1 % )
                                       545
   Total registers
   Total pins
                                       39 / 622 ( 6 % )
   Total virtual pins
                                       0
   Total memory bits
                                       0 / 1,152,000 ( 0 % )
   Embedded Multiplier 9-bit elements
                                       0/300(0%)
   Total PLLs
                                       0/4(0%)
```

4、 pos-sim 波形圖



- 5 \ minimum CYCLE in post-sim: 42
- 6 · gate level Simulation

通過測資截圖如下:

```
VSIM 31> run -all

# All data have been generated successfully!

# 
# ------PASS------

# 
*** Note: $finish : D:/ic_design/DIC_HW4/testfixture.v(143)

# Time: 5920374 ps Iteration: 0 Instance: /test

# 1
```