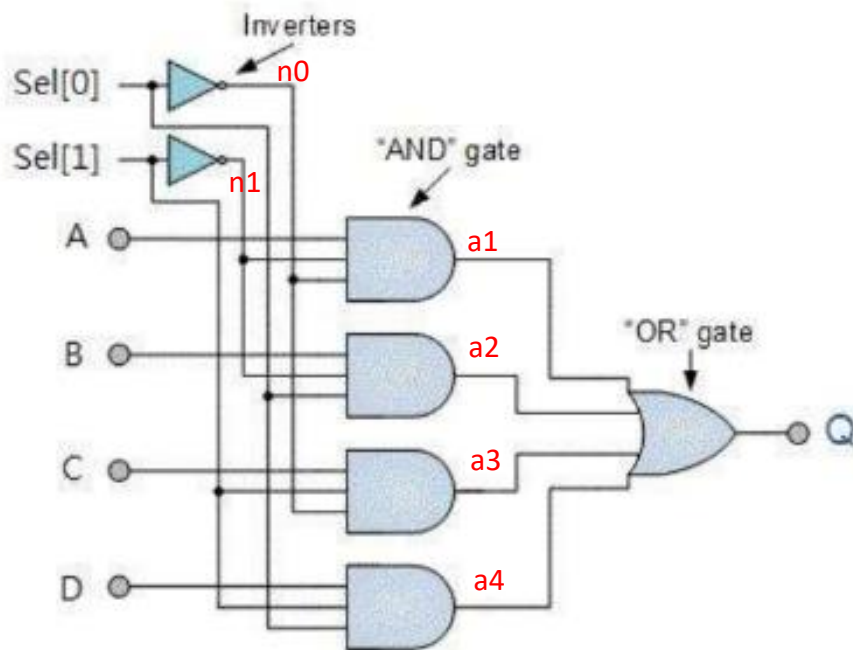


HW1 report

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1、 Design principle

依照作業給的 Gate-level structure 來設計。



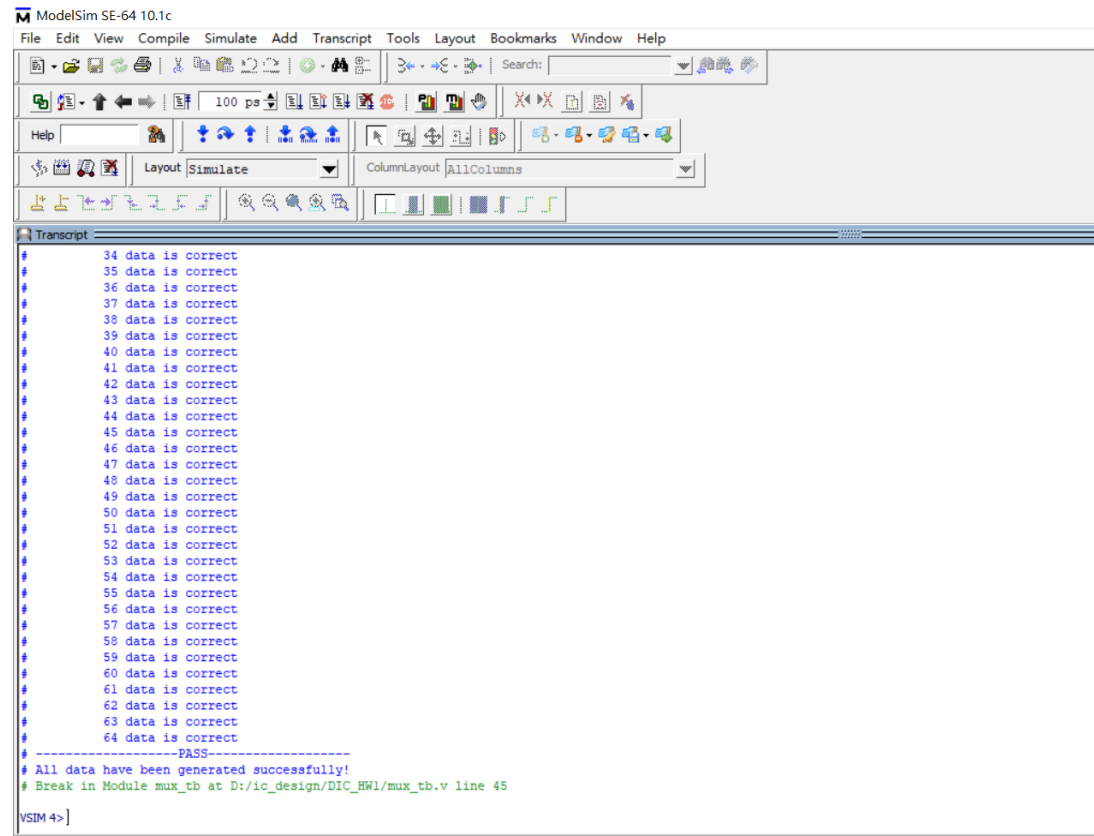
2、 flow summary result

Flow Summary	
Flow Status	Successful - Fri Nov 02 15:45:46 2018
Quartus II Version	10.0 Build 262 08/18/2010 SP 1 SJ Full Version
Revision Name	mux
Top-level Entity Name	mux
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Met timing requirements	Yes
Total logic elements	2 / 68,416 (< 1 %)
Total combinational functions	2 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	7 / 622 (1 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

3、minimum CYCLE in post-sim : 5

4、gate level Simulation

通過測資截圖如下：



The screenshot shows the ModelSim SE-64 10.1c interface. The top menu bar includes File, Edit, View, Compile, Simulate, Add, Transcript, Tools, Layout, Bookmarks, Window, and Help. Below the menu is a toolbar with various icons for file operations, simulation control, and viewing. The main window displays the 'Transcript' tab, which contains the following text:

```
# 34 data is correct
# 35 data is correct
# 36 data is correct
# 37 data is correct
# 38 data is correct
# 39 data is correct
# 40 data is correct
# 41 data is correct
# 42 data is correct
# 43 data is correct
# 44 data is correct
# 45 data is correct
# 46 data is correct
# 47 data is correct
# 48 data is correct
# 49 data is correct
# 50 data is correct
# 51 data is correct
# 52 data is correct
# 53 data is correct
# 54 data is correct
# 55 data is correct
# 56 data is correct
# 57 data is correct
# 58 data is correct
# 59 data is correct
# 60 data is correct
# 61 data is correct
# 62 data is correct
# 63 data is correct
# 64 data is correct
# -----PASS-----
# All data have been generated successfully!
# Break in Module mux_tb at D:/ic_design/DIC_HW1/mux_tb.v line 45
VSIM 4>]
```