NCKU-ES
Digital IC Design

Lab1

Design of Multiplexers

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VLSI signal processing LAB

Objectives

To familiarize with the basics of Verilog HDL
To learn the operations of Modelsim

LAB contents

LAB1-1: 2-1 Mux
LAB1-2: 4-1 Mux

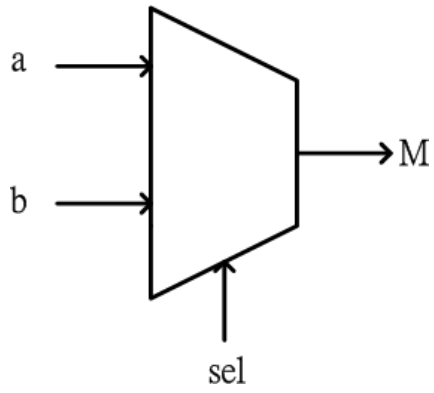
LAB1-1: 2-1 Mux

Design Description

A multiplexer (mux) is a device that chooses one of several input signals and forwards the selected input into a single line. A mux of 2^n inputs has n select lines, which are used to choose which input line to send to the output.

Design a 2-1 mux by writing **Verilog structural code**

Block Diagram



Specifications

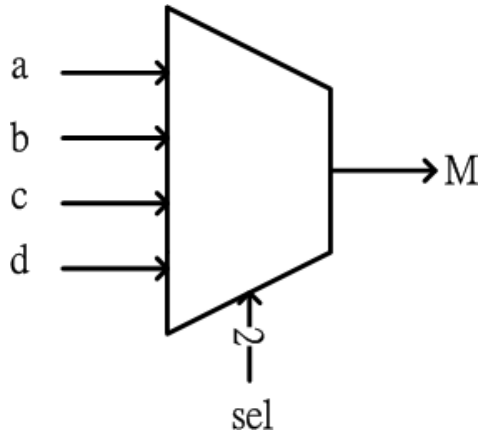
Top module name : mux_2_to_1 (File name: mux_2_to_1.v)
Input pins: a, b, sel
Output pins: M
All of the inputs and outputs are 1bit

LAB1-2: 4-1 Mux

Design Description

Please design a 4-1 mux by 2-1muxes you design in LAB1-1

Block Diagram



Specifications

Top module name : mux_4_to_1 (File name: mux_4_to_1.v)
Input pins: a, b, c, d, sel[0:1]
Output pins: M

- Note

須自行撰寫測試程式(Testbench)去驗證自己的作業

書面報告需包含

1. 設計原理(Design principle)
2. 邏輯閘(Gate level)架構
3. 波型(Waveform)分析

書面報告請勿手寫

繳交的作業資料夾組織與命名請與下頁圖示相同

作業繳交給人豪 jfslmarco@gmail.com

Due date: 2018/7/31(二)

- Directory Organization