NCKU-ES
Digital IC Design

Lab3

Bit-stream Pattern Detector

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VLSI signal processing LAB

- ## Objectives

  To familiarize with RTL code

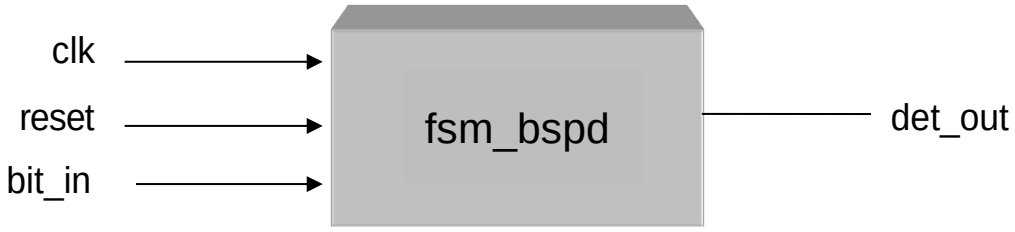
- ## LAB contents

  LAB3: bit-stream pattern detector

Design Description

- Please design a serial input bit-stream pattern detector module.
- Function：serial input bit-stream pattern detector. Using finite state Mealy-machine. “det_out” is to be low(logic0), unless the input bit-stream is “0010” sequentially. Example:
  bit_in：. . . . . 0 0 1 0 0 1 0 0 0 1 0 . . .
  det_out：. . . . 0 0 0 1 0 0 1 0 0 0 1 0 . . .
- All inputs are synchronized at clock(clk) rising edge.
- It is synchronous reset architecture.

Block Diagram



Specifications

- Top module name：fsm_bspd (File name: fsm_bspd.v)
- Input pins：clk , reset , bit_in
- Output pins：det_out

- Note

本測驗提供測試程式(testbench)，各位同學之作業需能通過 testbench 的驗證，通過測試的截圖，如下