Digital IC Design Training

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Outline

- Finite State Machine
- Example: Bit-stream Pattern Detector

Finite State Machine

What is FSM?

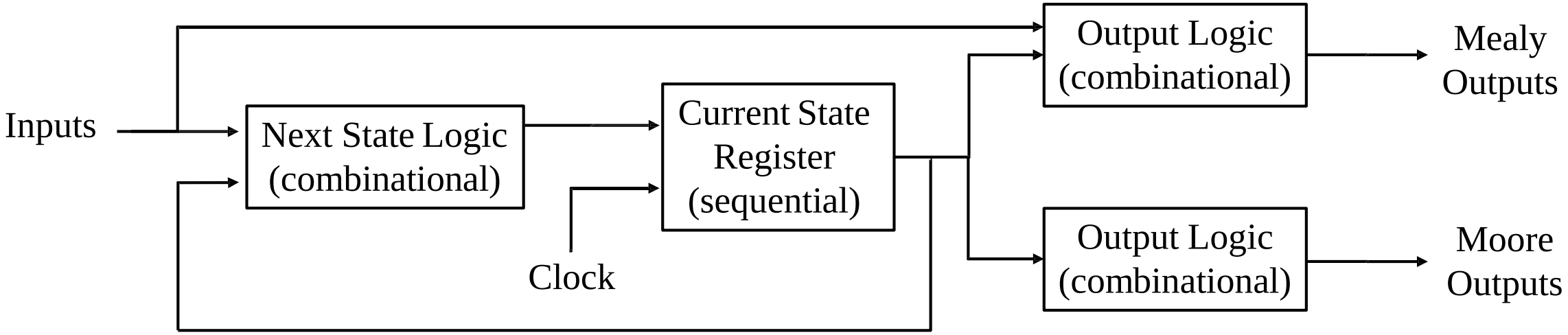
- A desired relationship between the input and the output sequences.
- FSM structures
  - Mealy machine
  - Moore machine

Finite State Machine

- FSM structures
  - Contains sequential networks and combinational logic.
  - The sequential network is a set of flip-flops.
  - Mealy machine: the output follows the input and current state.
  - Moore machine: the output depends on the current state only.

Finite State Machine

- FSM structures



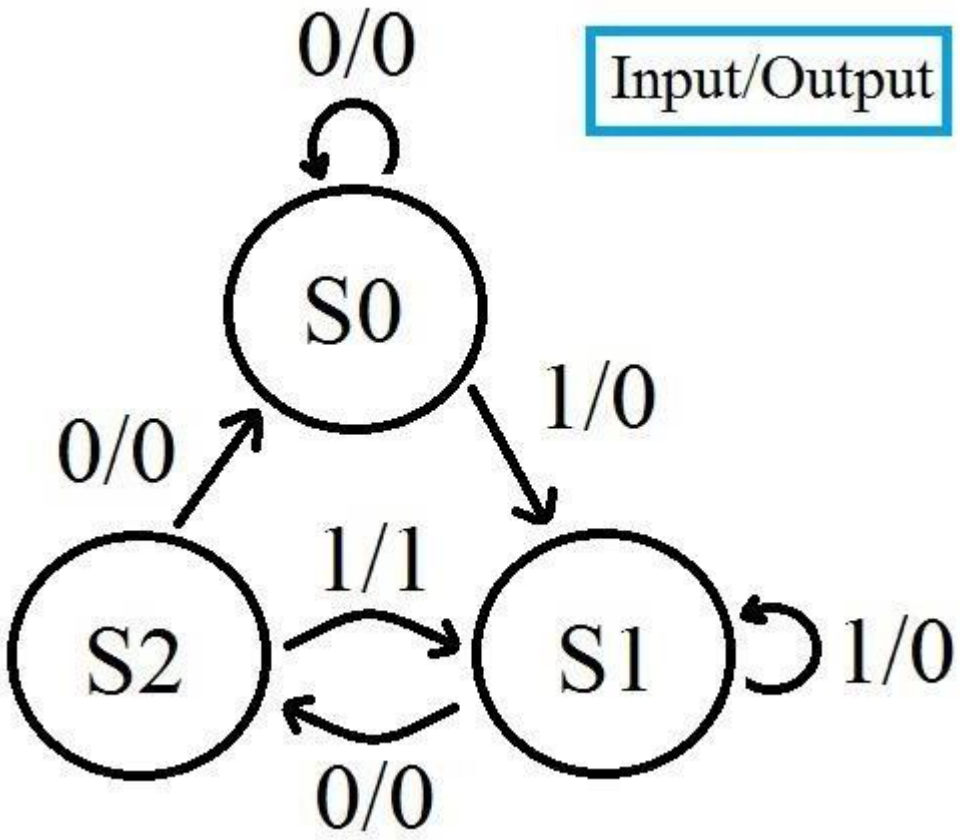
Example: Bit-stream Pattern Detector

- Input 1-bit *bit_in*. Output 1-bit *det_out*.
- *det_out* gives 1 when *bit_in* is 101.

bit_in = 001011010110011

det_out = 000010010100000

Current State	Next state		Output (det_out)	
	bit_in=0	*bit_in*=1	*bit_in*=0	*bit_in*=1
S0	S0	S1	0	0
S1	S2	S1	0	0
S2	S0	S1	0	1



```
1  module fsm_bspd2(clk, reset, bit_in, det_out);
2  input clk, reset, bit_in;
3  output det_out;
4
5  reg [1:0] current_state;
6  reg [1:0] next_state;
7  wire det_out;
8
9  parameter    S0 = 2'b00,
10              S1 = 2'b01,
11              S2 = 2'b10;
12
13 //FSM current state register
14 always@(posedge clk or posedge reset)
15     if(reset==1)
16         current_state <= S0;
17     else
18         current_state <= next_state;
19
```

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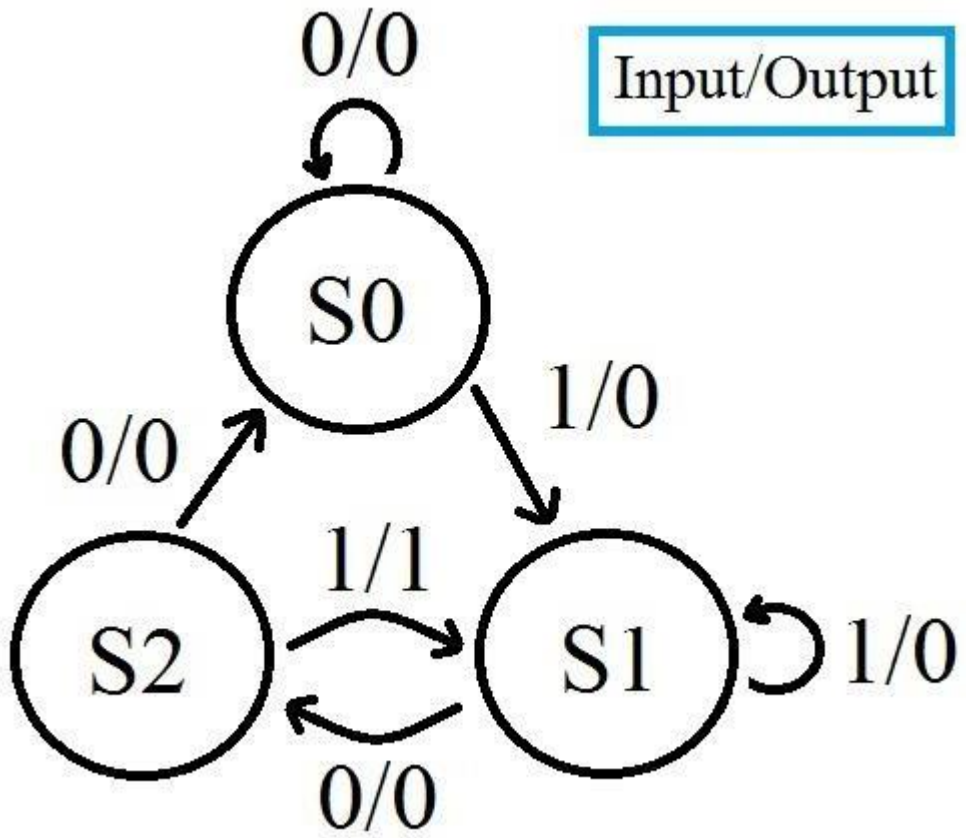

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S2	S0	S1	0	1

```
20  //FSM next state logic
21  always@(*)
22      case(current_state)
23          S0:  next_state = (bit_in==1) ? S1 : S0;
24          S1:  next_state = (bit_in==0) ? S2 : S1;
25          S2:  next_state = (bit_in==1) ? S1 : S0;
26          default: next_state = S0;
27      endcase
28
29  //FSM output logic
30  assign det_out = ((current_state==S2)&&(bit_in==1)) ? 1 : 0;
31
32  endmodule
```