

# LAB 3 Report

Team 4

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## Hierarchy

→ DE2\_115.sv

→ Altpll.v

→ Top.sv

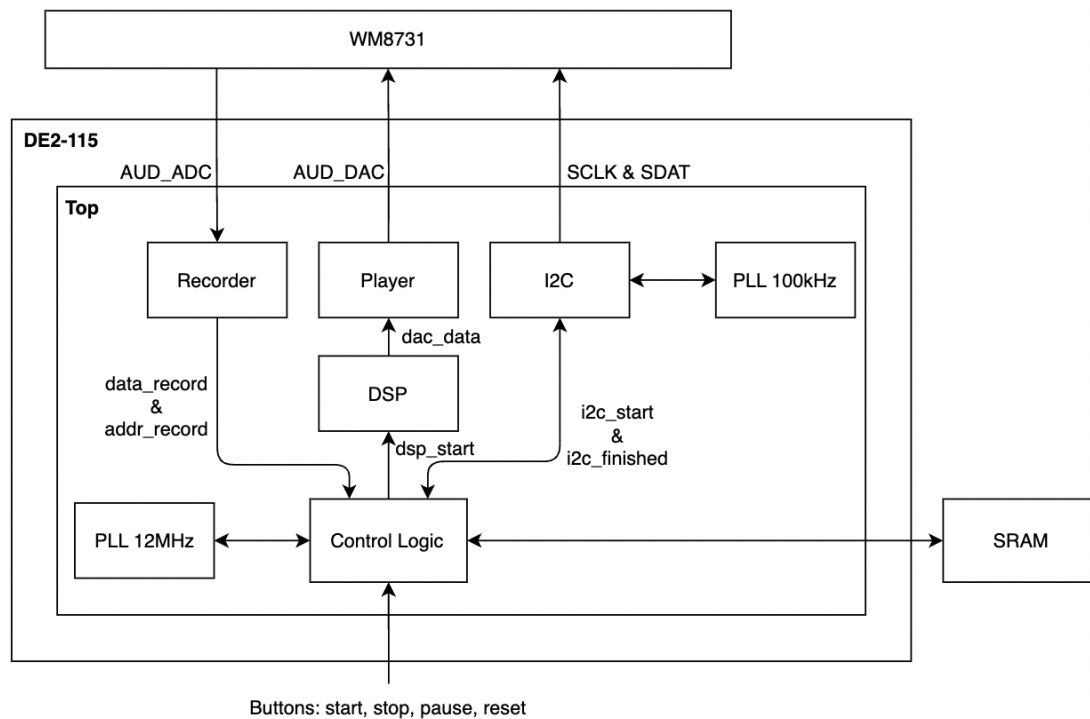
→ I2C.sv

→ AudRecorder.sv

→ AudPlayer.sv

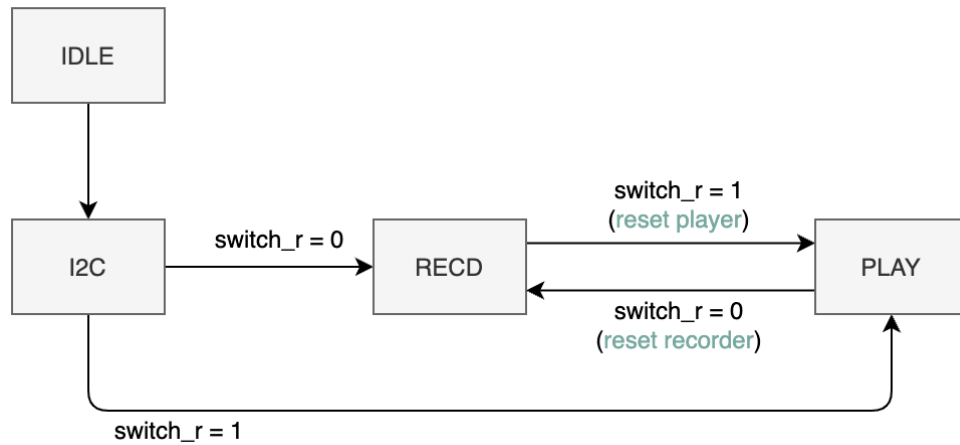
→ AudDSP.sv

## Block Diagram

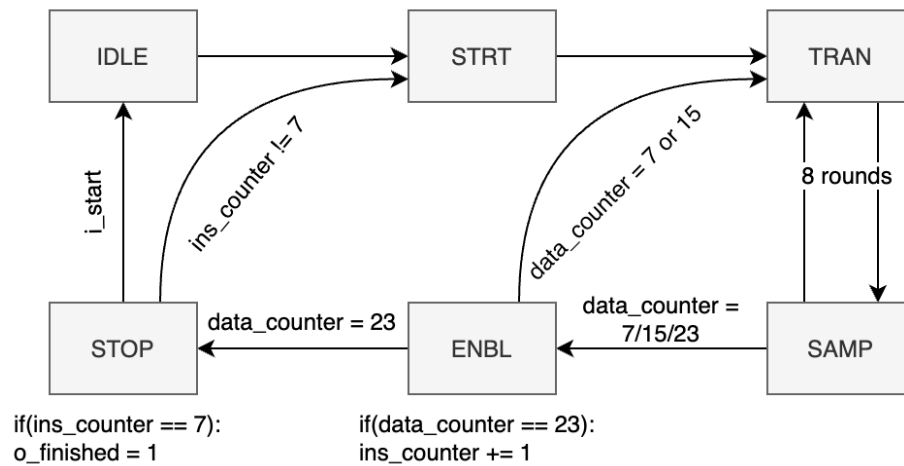


# FSM

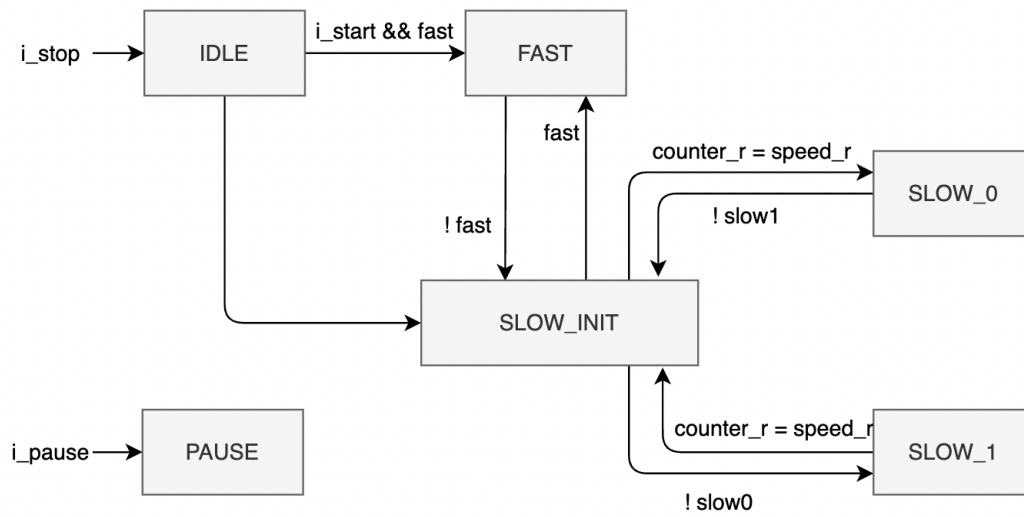
[Top Level]



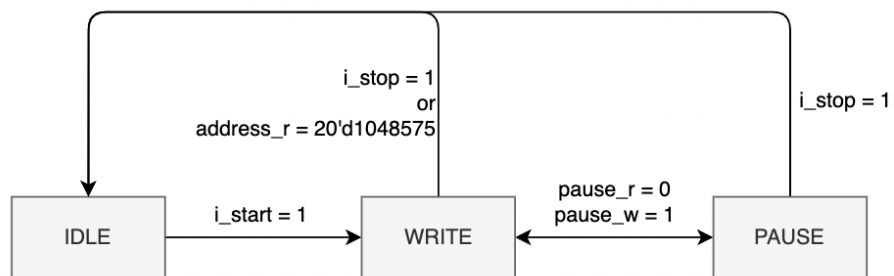
[I2C]



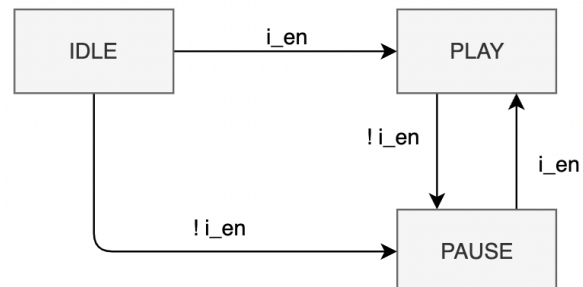
[DSP]



[Recorder]



[Player]



## Fitter Summary

**Fitter Summary**

Fitter Status	Successful - Thu Nov 03 13:58:18 2022
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	612 / 114,480 ( < 1 % )
Total combinational functions	587 / 114,480 ( < 1 % )
Dedicated logic registers	223 / 114,480 ( < 1 % )
Total registers	223
Total pins	518 / 529 ( 98 % )
Total virtual pins	0
Total memory bits	0 / 3,981,312 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 532 ( 0 % )
Total PLLs	1 / 4 ( 25 % )

## Timing Analyzer

**TimeQuest Timing Analyzer Summary**

Quartus II Version	Version 15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Device Family	Cyclone IV E
Device Name	EP4CE115F29C7
Timing Models	Final
Delay Model	Combined
Rise/Fall Delays	Enabled

**Slow 1200mV 85C Model Setup Summary**

	Clock	Slack	End Point TNS
1	AUD_BCLK	-3.278	-11.179
2	pll0 altpll_1 sd1 pll7 clk[1]	40.289	0.000
3	pll0 altpll_1 sd1 pll7 clk[0]	79.255	0.000

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Slow 1200mV 85C Model Recovery Summary

	Clock	Slack	End Point TNS
1	AUD_BCLK	-2.807	-149.491
2	pll0 altpll_1 sd1 pll7 clk[1]	79.207	0.000

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      - Hold: 'pll0|altpll\_1|sd1|pll7|clk[0]'
      - Hold: 'AUD\_BCLK'
      - Recovery: 'AUD\_BCLK'
      - Recovery: 'pll0|altpll\_1|sd1|pll7|clk[1]'
      - Removal: 'AUD\_BCLK'
      - Removal: 'pll0|altpll\_1|sd1|pll7|clk[1]'
      - Minimum Pulse Width: 'CLOCK\_50'

Slow 1200mV 85C Model Setup: 'AUD\_BCLK'

	Slack	From Node	To Node
1	-3.278	Top:top0 AudDSP:dsp0 o_dac_data_r[6]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
2	-3.228	Top:top0 AudDSP:dsp0 o_dac_data_r[14]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
3	-3.227	Top:top0 AudDSP:dsp0 o_dac_data_r[5]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
4	-3.225	Top:top0 AudDSP:dsp0 o_dac_data_r[4]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
5	-3.214	Top:top0 AudDSP:dsp0 o_dac_data_r[1]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
6	-3.176	Top:top0 AudDSP:dsp0 o_dac_data_r[12]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
7	-3.171	Top:top0 AudDSP:dsp0 o_dac_data_r[2]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
8	-3.159	Top:top0 AudDSP:dsp0 o_dac_data_r[0]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
9	-3.058	Top:top0 AudDSP:dsp0 o_dac_data_r[9]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
10	-3.006	Top:top0 AudDSP:dsp0 o_dac_data_r[8]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
11	-2.897	Top:top0 AudDSP:dsp0 o_dac_data_r[11]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
12	-2.859	Top:top0 AudDSP:dsp0 o_dac_data_r[7]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
13	-2.796	Top:top0 recorder_start_r	Top:top0 AudRecorder:recorder0 state_r_S_WRITE
14	-2.794	Top:top0 AudDSP:dsp0 o_dac_data_r[3]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
15	-2.747	Top:top0 recorder_pause_r	Top:top0 AudRecorder:recorder0 state_r_S_PAUSE
16	-2.673	Top:top0 AudDSP:dsp0 o_dac_data_r[15]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
17	-2.639	Top:top0 AudDSP:dsp0 o_dac_data_r[10]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
18	-2.542	Top:top0 recorder_stop_r	Top:top0 AudRecorder:recorder0 state_r_S_PAUSE
19	-2.522	Top:top0 recorder_pause_r	Top:top0 AudRecorder:recorder0 state_r_S_WRITE
20	-2.516	Top:top0 recorder_stop_r	Top:top0 AudRecorder:recorder0 state_r_S_WRITE
21	-2.493	Top:top0 AudDSP:dsp0 o_dac_data_r[13]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
22	-2.358	Top:top0 recorder_pause_r	Top:top0 AudRecorder:recorder0 pause_r
23	75.556	Top:top0 AudPlayer:player0 counter_r[0]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
24	76.092	Top:top0 AudPlayer:player0 counter_r[1]	Top:top0 AudPlayer:player0 o_aud_dacdat_r
25	76.407	Top:top0 AudRecorder:recorder0 counter_r[1]	Top:top0 AudRecorder:recorder0 data_r[9]

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      - Recovery: 'pll0|altpll\_1|sd1|pll7|clk[1]'
      - Removal: 'AUD\_BCLK'
      - Removal: 'pll0|altpll\_1|sd1|pll7|clk[1]'
      - Minimum Pulse Width: 'CLOCK\_50'

Slow 1200mV 85C Model Recovery: 'AUD\_BCLK'

	Slack	From Node	To Node	Launch Clock
1	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[15]	pll0 altpll_1 sd1 pll7 clk[1]
2	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[14]	pll0 altpll_1 sd1 pll7 clk[1]
3	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[13]	pll0 altpll_1 sd1 pll7 clk[1]
4	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[7]	pll0 altpll_1 sd1 pll7 clk[1]
5	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[6]	pll0 altpll_1 sd1 pll7 clk[1]
6	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[5]	pll0 altpll_1 sd1 pll7 clk[1]
7	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[4]	pll0 altpll_1 sd1 pll7 clk[1]
8	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[2]	pll0 altpll_1 sd1 pll7 clk[1]
9	-2.807	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[0]	pll0 altpll_1 sd1 pll7 clk[1]
10	-2.721	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[3]	pll0 altpll_1 sd1 pll7 clk[1]
11	-2.682	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[1]	pll0 altpll_1 sd1 pll7 clk[1]
12	-2.682	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 state_r_S_WRITE	pll0 altpll_1 sd1 pll7 clk[1]
13	-2.682	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 state_r_S_PAUSE	pll0 altpll_1 sd1 pll7 clk[1]
14	-2.636	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 pause_r	pll0 altpll_1 sd1 pll7 clk[1]
15	-2.506	Top:top0 player_rst_r	Top:top0 AudPlayer:player0 counter_r[3]	pll0 altpll_1 sd1 pll7 clk[1]
16	-2.506	Top:top0 player_rst_r	Top:top0 AudPlayer:player0 counter_r[4]	pll0 altpll_1 sd1 pll7 clk[1]
17	-2.506	Top:top0 player_rst_r	Top:top0 AudPlayer:player0 counter_r[5]	pll0 altpll_1 sd1 pll7 clk[1]
18	-2.506	Top:top0 player_rst_r	Top:top0 AudPlayer:player0 counter_r[6]	pll0 altpll_1 sd1 pll7 clk[1]
19	-2.506	Top:top0 player_rst_r	Top:top0 AudPlayer:player0 counter_r[7]	pll0 altpll_1 sd1 pll7 clk[1]
20	-2.501	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[12]	pll0 altpll_1 sd1 pll7 clk[1]
21	-2.501	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[11]	pll0 altpll_1 sd1 pll7 clk[1]
22	-2.501	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[10]	pll0 altpll_1 sd1 pll7 clk[1]
23	-2.501	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[9]	pll0 altpll_1 sd1 pll7 clk[1]
24	-2.501	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 data_r[8]	pll0 altpll_1 sd1 pll7 clk[1]
25	-2.491	Top:top0 recorder_rst_r	Top:top0 AudRecorder:recorder0 counter_r[0]	pll0 altpll_1 sd1 pll7 clk[1]

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**Multicorner Timing Analysis Summary**

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	▼ Worst-case Slack	-3.278	0.181	-2.807	0.500	9.400
1	AUD_BCLK	-3.278	0.201	-2.807	0.500	40.694
2	CLOCK2_50	N/A	N/A	N/A	N/A	16.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	16.000
4	CLOCK_50	N/A	N/A	N/A	N/A	9.400
5	pll0 altpll_1 sd1 pll7 clk[0]	79.255	0.183	N/A	N/A	4999.710
6	pll0 altpll_1 sd1 pll7 clk[1]	40.289	0.181	79.207	1.764	41.374
2	▼ Design-wide TNS	-11.179	0.0	-149.491	0.0	0.0
1	AUD_BCLK	-11.179	0.000	-149.491	0.000	0.000
2	CLOCK2_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
4	CLOCK_50	N/A	N/A	N/A	N/A	0.000
5	pll0 altpll_1 sd1 pll7 clk[0]	0.000	0.000	N/A	N/A	0.000
6	pll0 altpll_1 sd1 pll7 clk[1]	0.000	0.000	0.000	0.000	0.000

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**Unconstrained Paths**

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	30	30
4	Unconstrained Input Port Paths	333	333
5	Unconstrained Output Ports	47	47
6	Unconstrained Output Port Paths	114	114

## Difficulties & Solutions

- [I2C] 一開始我是另外拉一個小module去define每一輪的8 bits, 但這樣會增加define SDA的難度以及增加counter的數量:
  - Solution: 用matrix的方式define 7 個24 bit的instructions, 我也是在這次lab中才學到如何在verilog中define/使用 matrix
- [I2C] 在助教的github上有看到好像每傳24b要經過114 cycles, 但我們怎麼想/計算都算不到那麼多:
  - Solution: 後來實作上好像沒出什麼問題, 所以應該只有52 cycles 也是ok的
- [PLAYER] 播放時出現大量雜音
  - Solution: 在送完16bit音訊後, o\_AUD\_DACDAT不能設0或dacdata[LSB], 而是要

設為dacdata[MSB]

- [DSP] 在一次內差慢速播放時會有雜音
  - Solution: 在計算內差值時可能會有超過16b的值而發生overflow的問題，因此在計算時需要使用更多的bit做計算才能保證計算結果的正確

## Bonus!

把播放狀態印出來：

顯示	狀態
0	IDLE
1	initialize
2	record
3	play