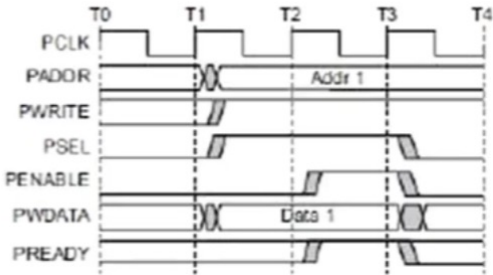
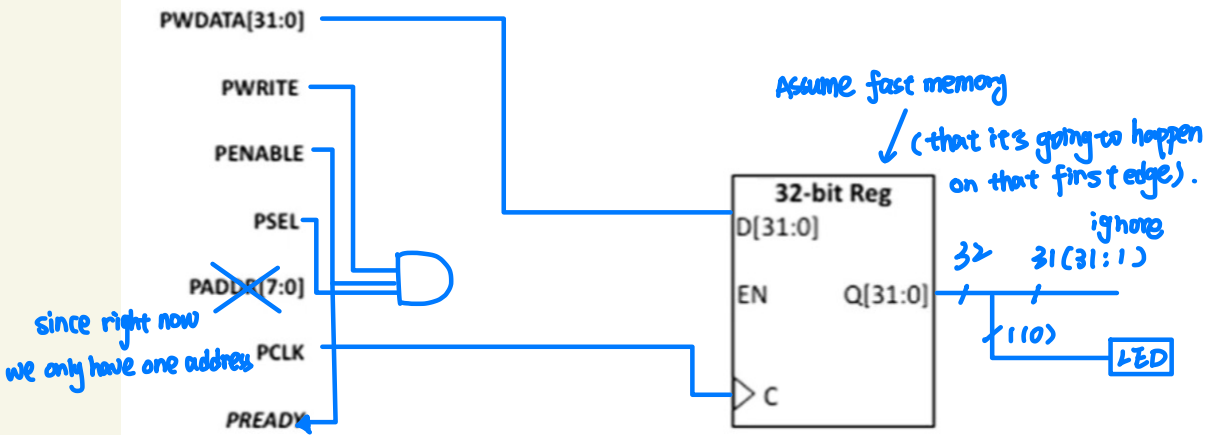
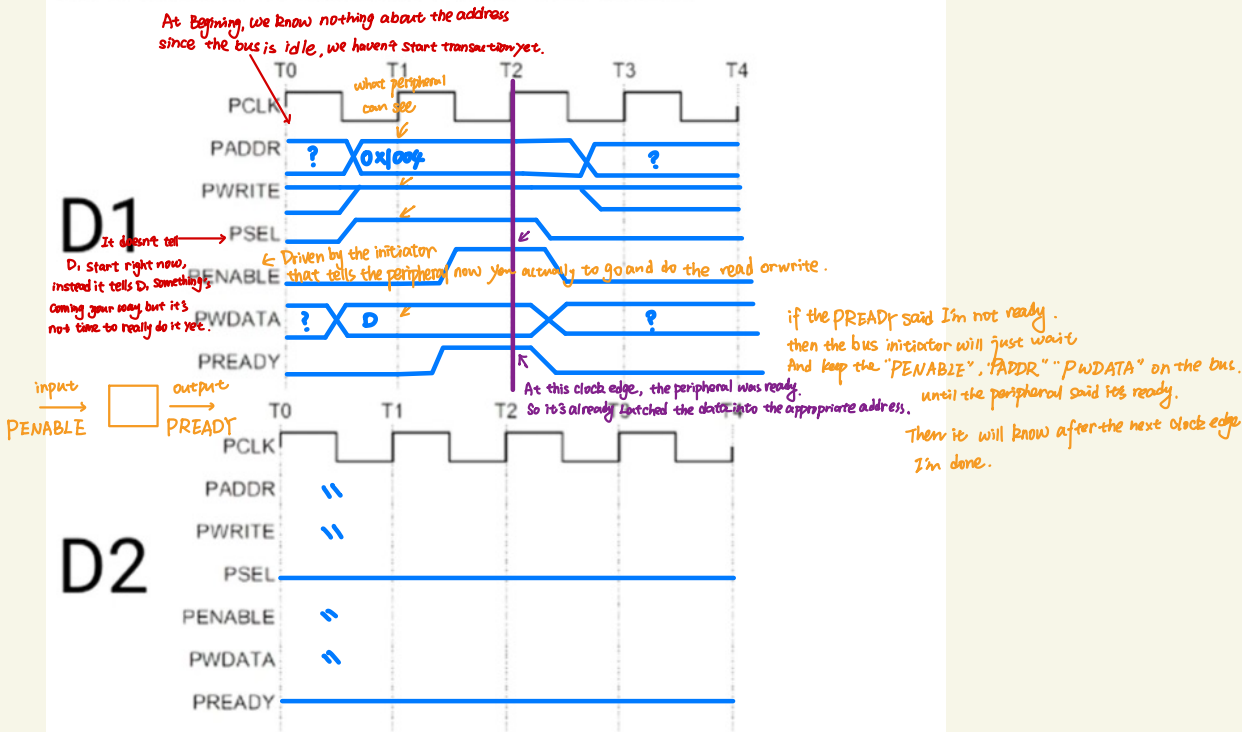
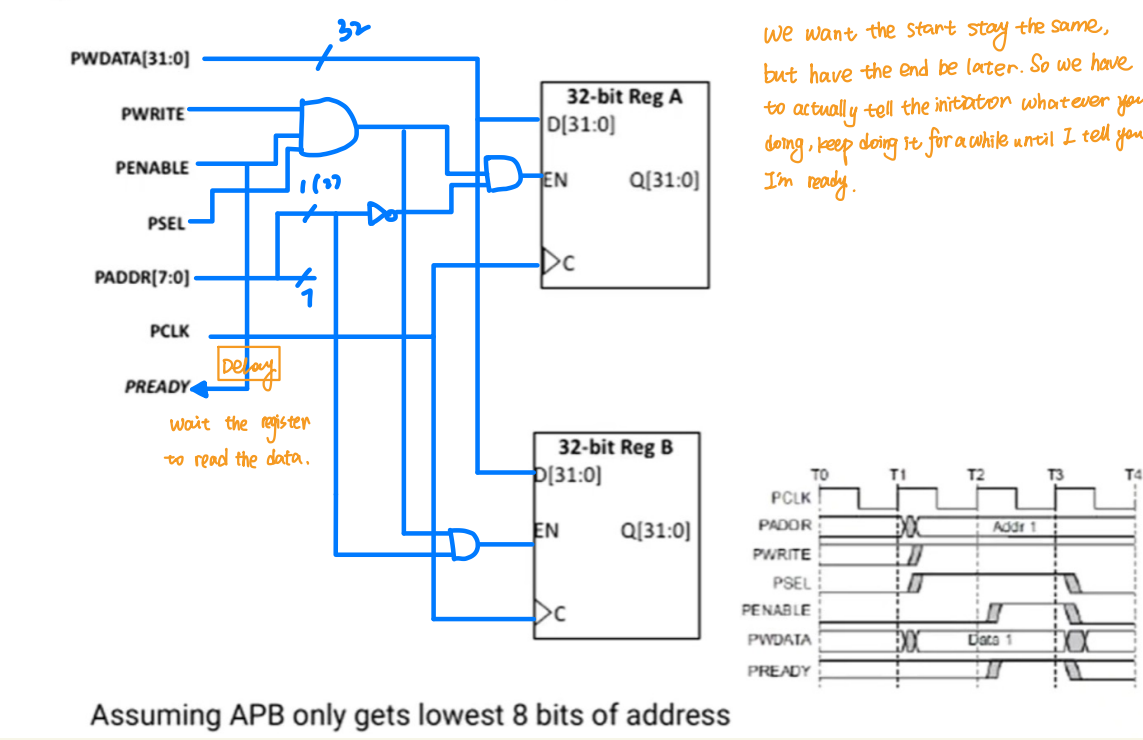


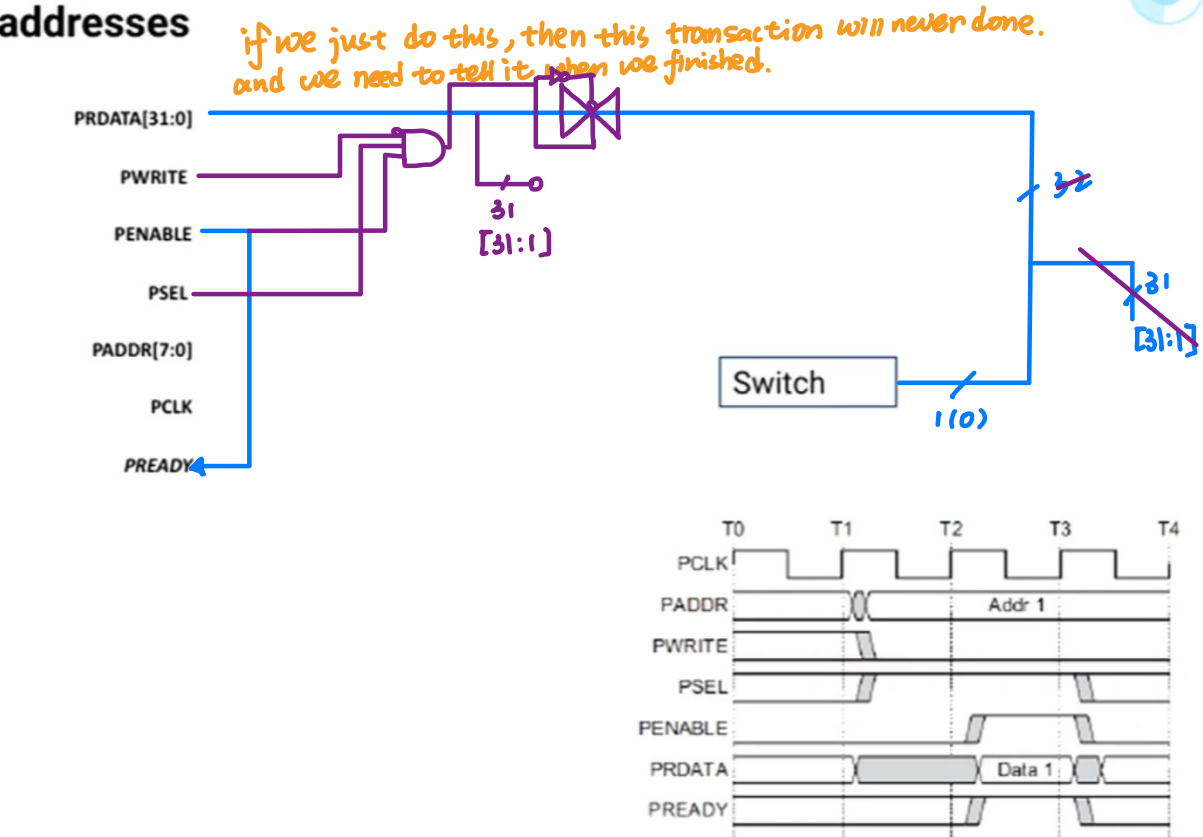
### CPU stores to 0x00001004 w.o. stalls



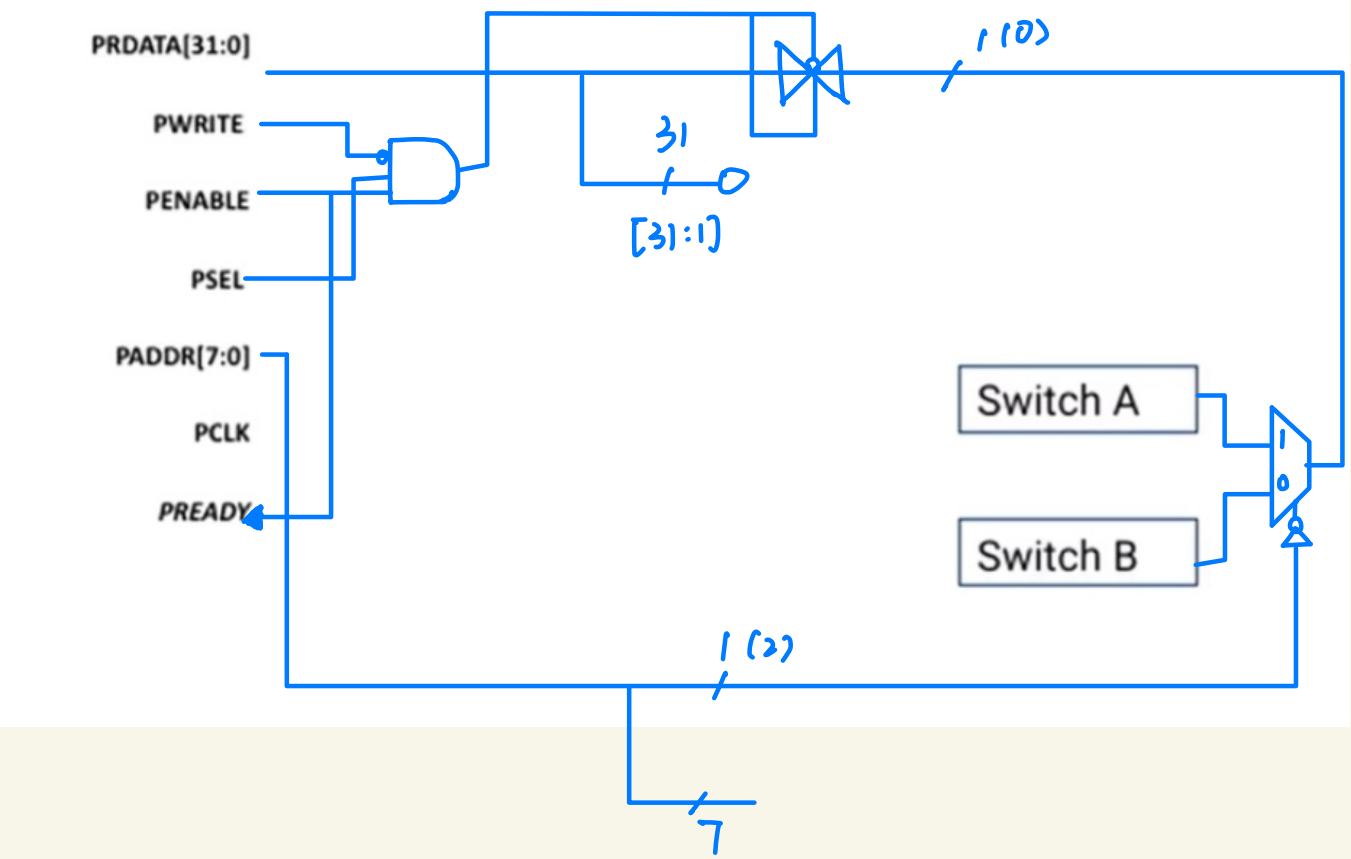
Reg A should be written at address 0x00001000  
Reg B should be written at address 0x00001004



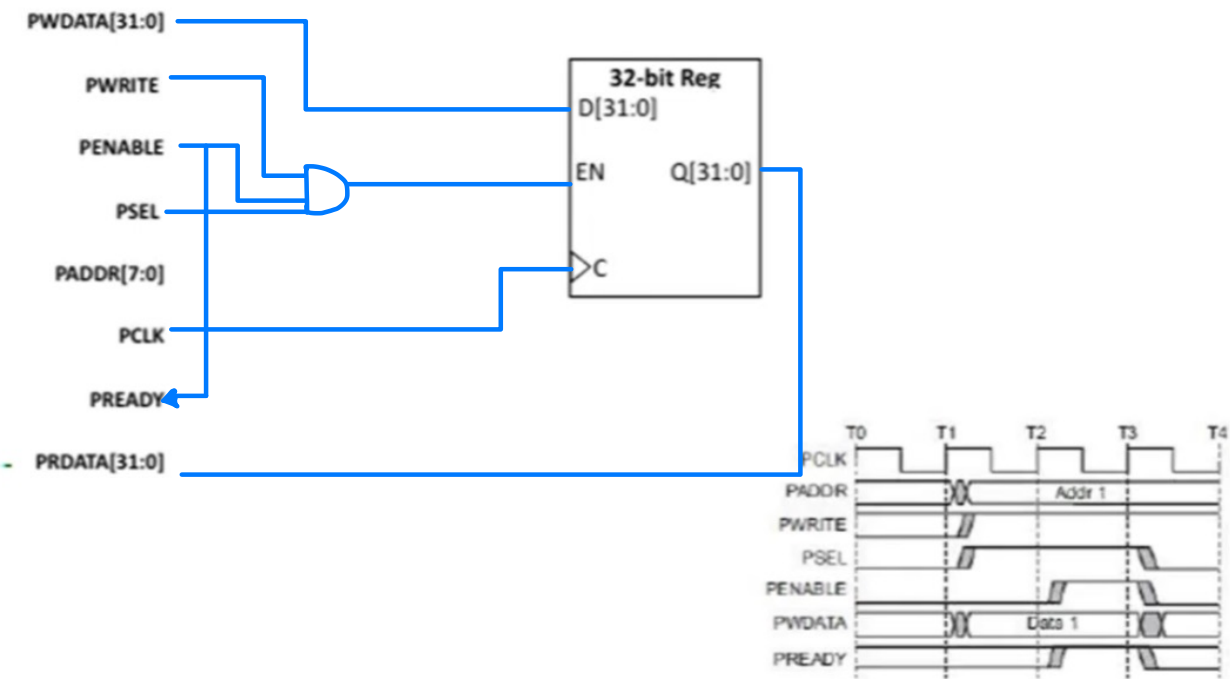
Device provides data from switch for any of its addresses



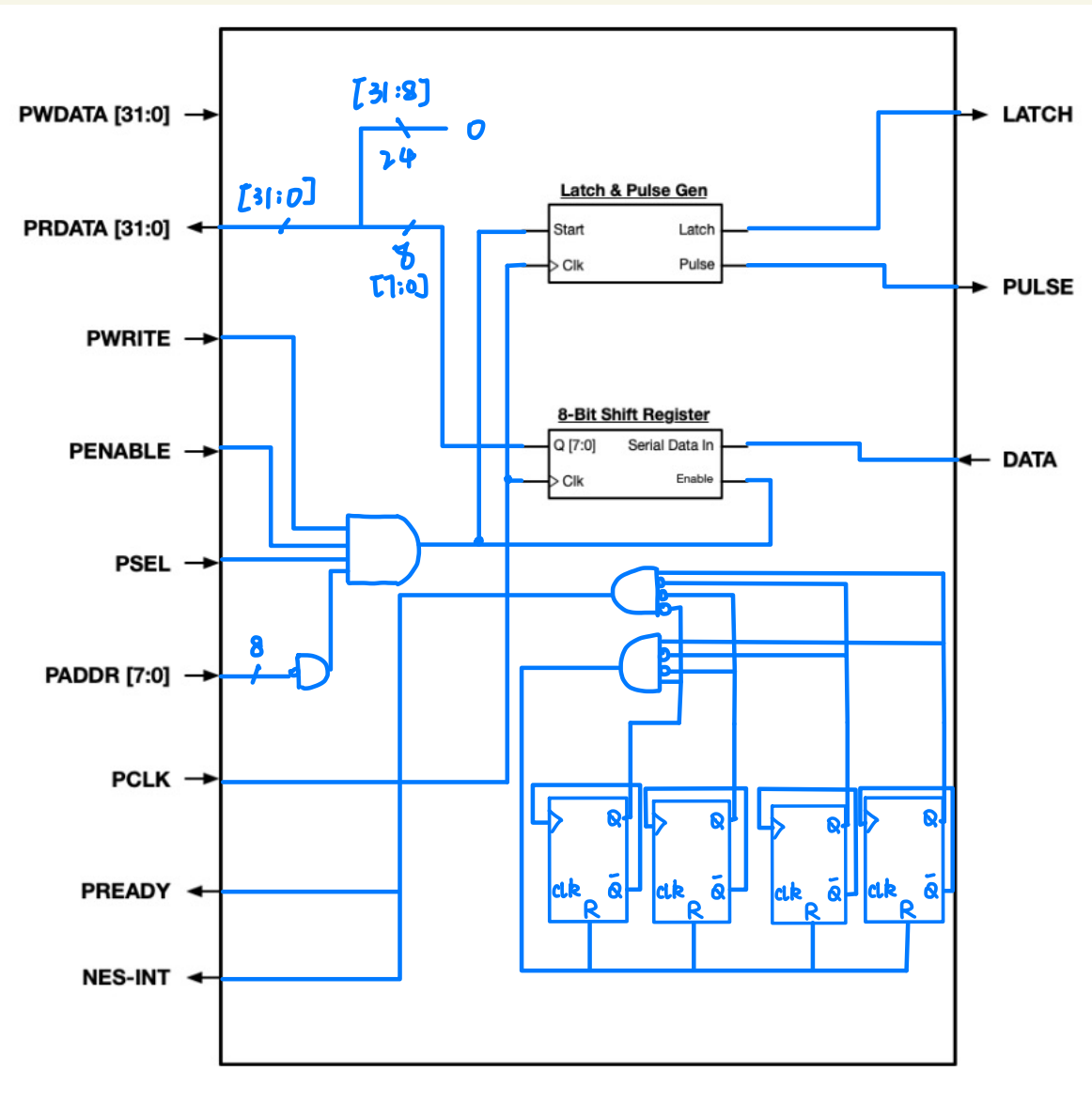
Switch A for 0x00001000, B for 0x00001004



All reads read from register, all writes write



Assuming APB only gets lowest 8 bits of address



The diagram shows the timing of an I2C transaction. The SDA signal (blue) starts with a start condition (low-to-high transition). It then transmits a series of data bytes. Each byte is represented by a high level for the MSB (Most Significant Bit) and a low level for the LSB (Least Significant Bit). The R/W (Read/Write) bit is indicated by a high level for read and a low level for write. The ACK (Acknowledge) signal is shown as a low level on the SDA line. The SCL signal (grey) provides the clock pulses. The transaction ends with a stop condition (high-to-low transition on SDA).

