UNIVERSITY OF MICHIGAN

EECS 270: Intro to Logic Design

Makeup for Exam 2

Prof. Karem A Sakallah

Friday November 18, 2022
9:00-11:00 a.m.

2725 BBB

Name: _____

UMID: _____

Honor Pledge:
"I have neither given nor received aid on this exam, nor have I concealed any violation of the Honor Code."

Signature: _____

Instructions:

- The exam is closed book except for two 8.5"x11" sheets of notes No electronics of any kind may be used.
- Print your name and student ID number and sign the honor pledge.
- Make sure your answers and meaningful work are on the pages with numbers at the bottom. We will be scanning and looking at only these pages: all work on the backs of pages will **not** checked for determining partial credit.
- The exam consists of 8 problems with the point distribution indicated here. Please keep this in mind as you work through the exam. Use your time wisely.
- There are 10 pages in this exam. Make sure that you have all 10 pages and notify an instructor if you do not.

1.	/10
2.	/15
3.	/15
4.	/6
5.	/16
6.	/10
7.	/10
8.	/18
Total:	/100

1 [Miscellaneous–10 points]

a. **[1 points]** All minterms of a Boolean function are implicants. **TRUE** **FALSE**

b. **[1 points]** A minterm that is a prime implicant must be essential. **TRUE** **FALSE**

c. **[1 points]** The implicant $b'cd'$ for a function f of 7 variables covers 8 minterms **TRUE** **FALSE**

d. **[1 points]** If $xy'z$ is an implicant of a function f, then xy' is too. **TRUE** **FALSE**

e. **[6 points]** The table below lists the next-state equations for three different types of 5-bit counters. Complete the table by writing the corresponding counter type and modulus.

Next-State Equations	Counter Type	Counter Modulus
$Q_4^+ = Q_3$ $Q_3^+ = Q_2$ $Q_2^+ = Q_1$ $Q_1^+ = Q_0$ $Q_0^+ = Q_4$		
$Q_4^+ = Q_3$ $Q_3^+ = Q_2$ $Q_2^+ = Q_1$ $Q_1^+ = Q_0$ $Q_0^+ = Q'_4$		
$Q_4^+ = Q_4 \oplus (Q_3 \cdot Q_2 \cdot Q_1 \cdot Q_0)$ $Q_3^+ = Q_3 \oplus (Q_2 \cdot Q_1 \cdot Q_0)$ $Q_2^+ = Q_2 \oplus (Q_1 \cdot Q_0)$ $Q_1^+ = Q_1 \oplus Q_0$ $Q_0^+ = Q'_0$		

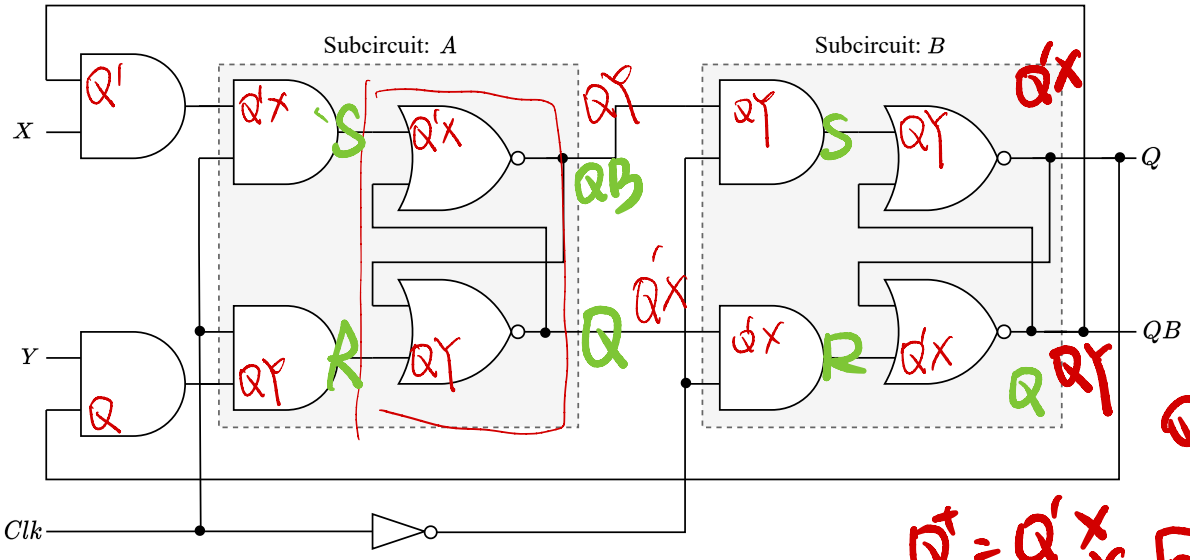
a. TRUE
b. TRUE
c. FALSE
d. FALSE

e. Counters

- Ring, 5.
- Johnson, 10.
- Binary, 32.

2 [Latches and Flipflops–15 points]

Consider the following gate-level diagram of a memory circuit:



a. **[6 points]** For each of the indicated sub-circuits, which of the options correctly describes the behavior of the circuit with respect to the clock input?

Sub-circuit A:
- ◯ Positive edge triggered
- ◯ Negative edge triggered
- ◯ Positive level sensitive
- ◯ Negative level sensitive

Sub-circuit B:
- ◯ Positive edge triggered
- ◯ Negative edge triggered
- ◯ Positive level sensitive
- ◯ Negative level sensitive

Entire Circuit:
- ◯ Positive edge triggered
- ◯ Negative edge triggered
- ◯ Positive level sensitive
- ◯ Negative level sensitive

b. **[9 points]** Complete the following transition table and indicate what operation the row corresponds to by filling in the correct bubble.

Input X	Input Y	Next Output Q^+	Next Output QB^+	Operation: Set	Reset	Hold	Toggle
0	0	0	0	◯	◯	●	◯
0	1	0	1	◯	●	◯	◯
1	0	1	0	●	◯	◯	◯
1	1	QB	Q	◯	◯	◯	●

a. Subcircuit A: Positive level sensitive
Subcircuit B: Negative level sensitive
Entire Circuit: Negative edge triggered

b.

Input		Next Output		Operation			
X	Y	Q^+	QB^+	Set	Reset	Hold	Toggle
0	0	Q	QB	◯	◯	●	◯
0	1	0	1	◯	●	◯	◯
1	0	1	0	●	◯	◯	◯
1	1	QB	Q	◯	◯	◯	●

3 [Karnaugh map–15 points]

Consider the following K-Map for the 4-variable function $f(w, x, y, z)$:

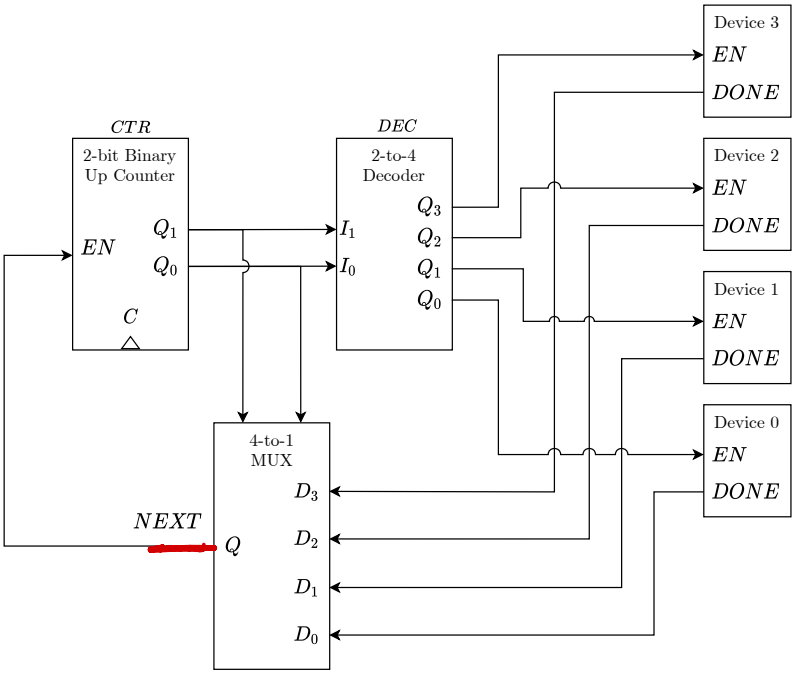
wx \ yz	00	01	11	10
00	1	d	d	1
01	d	1	0	1
11	1	0	1	d
10	1	1	0	1

For each of the product terms in the following table, indicate if the product term is an implicant of f, and whether it is prime and/or essential. Indicate your answer by filling in the bubbles below. *Hint: It helps if you first find **all** the prime implicants before filling the table!*

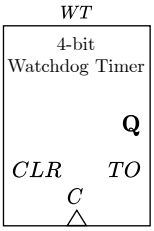
Product Term	x'	z'	$w'x'$	$w'xz'$	$w'x'z$	$x'y'$	wxy	$x'z'$	$w'y'$	wy
Implicant?	◯	◯	◯	◯	◯	◯	◯	◯	◯	◯
Prime Implicant?	◯	◯	◯	◯	◯	◯	◯	◯	◯	◯
Essential PI?	◯	◯	◯	◯	◯	◯	◯	◯	◯	◯

Product Term	x'	z'	$w'x'$	$w'xz'$	$w'x'z$	$x'y'$	wxy	$x'z'$	$w'y'$	wy
Implicant?	◯	●	●	●	◯	●	●	●	●	◯
Prime Implicant?	◯	●	●	◯	◯	●	●	◯	●	◯
Essential PI?	◯	●	◯	◯	◯	●	●	◯	●	◯

4 [Polling–6 points]



As was pointed out in lecture, the above polling circuit is not robust since it may enter a possibly indefinite waiting state if one of the devices is non-responsive (device does not send a DONE signal or sends it after a very long delay).



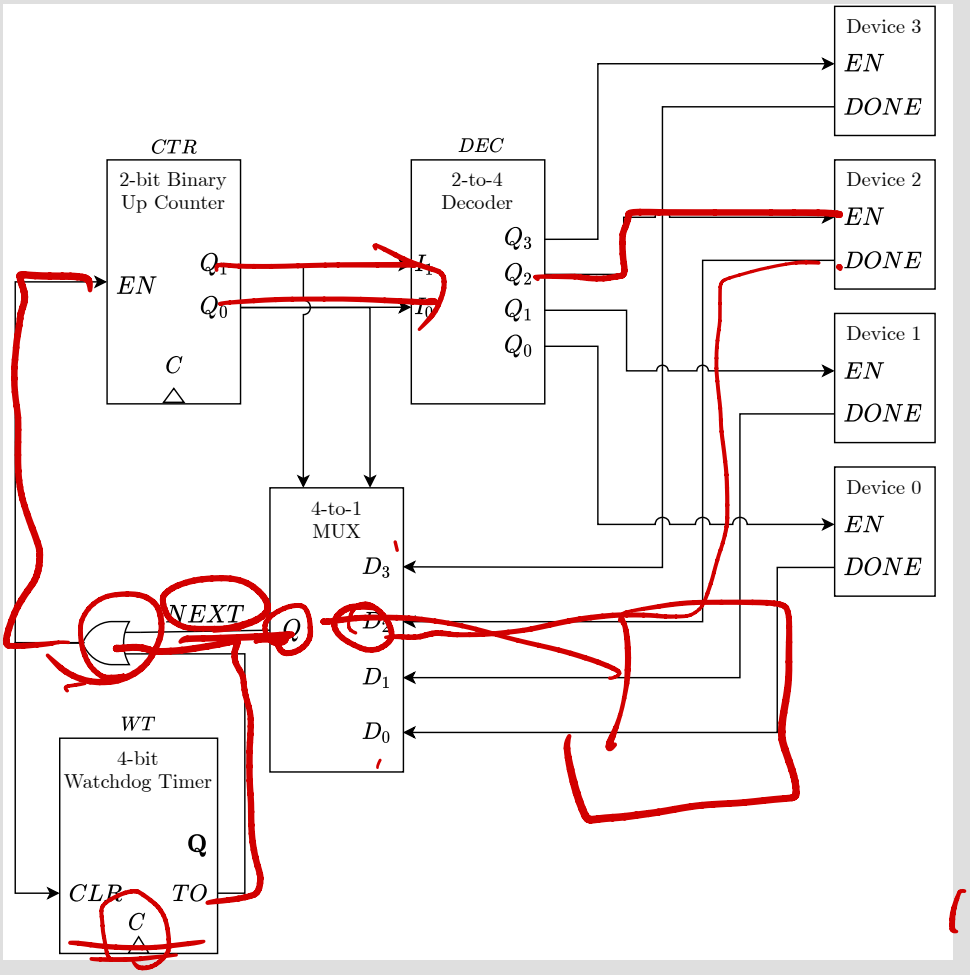
A simple modification to this circuit uses a Watchdog Timer that overrides a non-responsive device after a specified *Time-Out* period. For this problem assume that the Watchdog Timer is implemented by a 4-bit binary up-counter which can be cleared to 0000 and which asserts a time-out signal *TO* when the count reaches 1111.

Using $CTR.EN$, $WT.CLR$, and $WT.TO$ to denote the counter's enable input and the Watchdog timer's clear input and time-out output, write the simplest possible expressions in the modified design for enabling the counter and clearing the Watchdog timer.

a. **[2 points]** $CTR.EN =$

b. **[2 points]** $WT.CLR =$

c. **[2 points]** Assuming a 100MHz clock, what is the time-out interval?



a. **[2 points]** $CTR.EN =$ $Next + WT.TO$

b. **[2 points]** $WT.CLR =$ $Next + WT.TO$

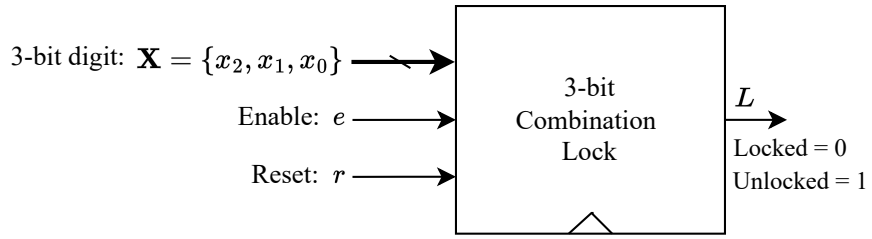
c. **[2 points]** Assuming a 100MHz clock, what is the time-out interval?

150 ns

Should accept answers given as a fraction as well

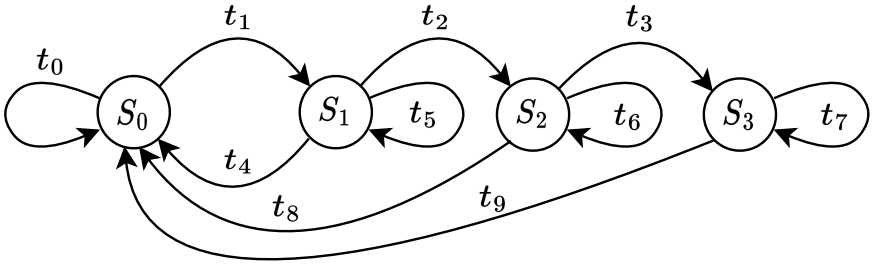
5 [Sequential Combination Lock–16 points]

Consider the following block diagram of a 3-bit sequential combination lock:



The circuit begins in the "locked" state ($L = 0$) and only becomes "unlocked" ($L = 1$) if the sequence of digits "2, 7, 0" is entered on $\mathbf{X}$. Only one 3-bit digit may be entered at a time, and if an incorrect digit is entered, the user must restart from the beginning. To enter a digit, the user sets the enable to $e = 1$, otherwise no digit is entered (to avoid unintentional inputs). The combination lock may be reset (synchronously) at any time by setting $r = 1$, which clears any numbers that have been entered previously. Once the circuit is unlocked ($L = 1$), it stays unlocked until it is reset.

The combination lock circuit can be implemented with a finite-state machine containing 4 states. The following figure shows the state diagram with transitions.



a. **[1 points]** How many D-flipflops are required to implement this circuit?

b. **[13 points]** Specify the required conditions on e, r, and $\mathbf{X}$ for each transition to occur. Write your answers as Boolean expressions. Please use terms like ($\mathbf{X} = 2$), ($\mathbf{X} \neq 7$), etc. in your answers when $\mathbf{X}$ is involved. Your expressions do not need to be minimal, but it helps us with grading :)

[2 pt] $t_0 =$		**[1 pt]** $t_5 =$	
[1 pt] $t_1 =$		**[1 pt]** $t_6 =$	
[1 pt] $t_2 =$		**[1 pt]** $t_7 =$	
[1 pt] $t_3 =$		**[2 pt]** $t_8 =$	
[2 pt] $t_4 =$		**[1 pt]** $t_9 =$	

c. **[2 points]** In which states should the output Z be 1? Fill in one or more bubbles.

S_0: ◯ S_1: ◯ S_2: ◯ S_3: ◯

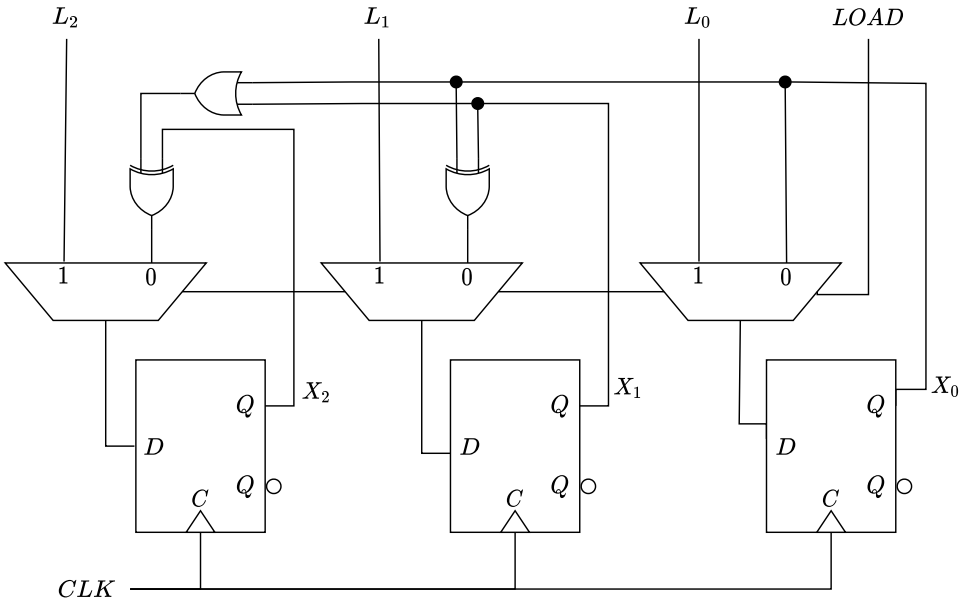
a. 2

b. $t_0 = r + e' + (\mathbf{X} \neq 2)$
$t_1 = r'e(\mathbf{X} = 2)$
$t_2 = r'e(\mathbf{X} = 7)$
$t_3 = r'e(\mathbf{X} = 0)$
$t_4 = r + e(\mathbf{X} \neq 7)$
$t_5 = r'e'$
$t_6 = r'e'$
$t_7 = r'$
$t_8 = r + e(\mathbf{X} \neq 0)$
$t_9 = r$

c. S_0: ◯ S_1: ◯ S_2: ◯ S_3: ●

6 [Sequential Circuit Analysis–10 points]

Consider the following sequential circuit:



a. **[4 points]** Complete the following transition table when $LOAD = 0$:

X_2	X_1	X_0	X_2^+	X_1^+	X_0^+
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

b. **[4 points]** Assuming that $\mathbf{L} \equiv L_2L_1L_0$ and $\mathbf{X} \equiv X_2X_1X_0$ respresent 3-bit two's complement numbers, complete the following transition table when $LOAD = 0$:

$\mathbf{X}$	$\mathbf{X}^+$
0	
1	
2	
3	

c. **[2 points]** Write a Verilog RTL expression for $\mathbf{X}^+$ in terms of $LOAD$, $\mathbf{L}$ and $\mathbf{X}$:

$\mathbf{X}^+ =$ [ ]

a. **[4 points]**

X_2	X_1	X_0	X_2^+	X_1^+	X_0^+
0	0	0	0	0	0
0	0	1	1	1	1
0	1	0	1	1	0
0	1	1	1	0	1
1	0	0	1	0	0
1	0	1	0	1	1
1	1	0	0	1	0
1	1	1	0	0	1

b. **[4 points]**

X	$\mathbf{X}^+$
0	0
1	-1
2	-2
3	-3
-4	-4
-3	3
-2	2
-1	1

c. **[2 points]**

$\mathbf{X}^+ = \boxed{LOAD?\ \mathbf{L} : -\mathbf{X}}$

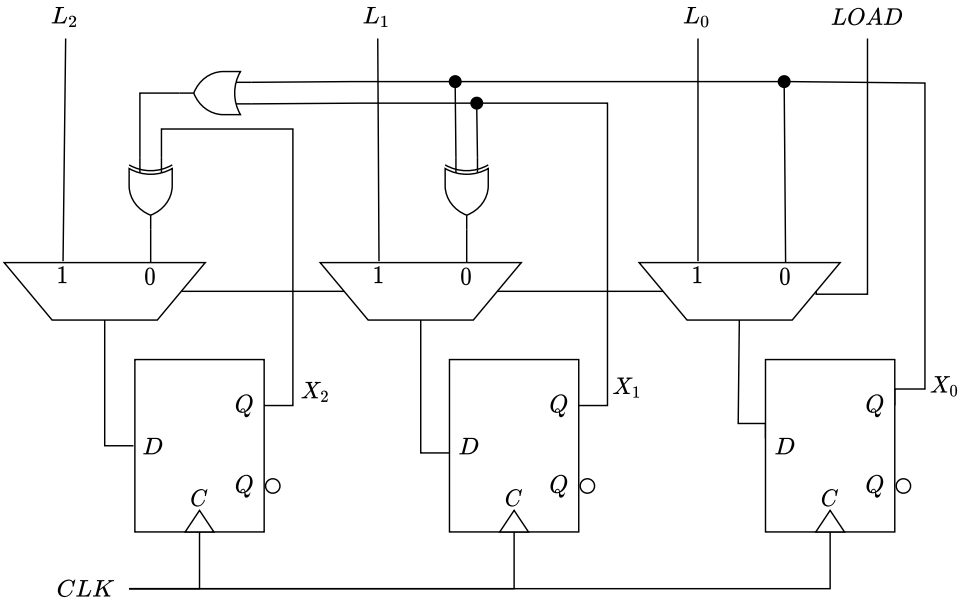
Accept other Verilog solutions that are equivalent to this.

7 [Sequential Timing Analysis–10 points]

Assume the following timing parameters for the sequential circuit from Problem 5 (repeated here for your convenience):

OR delay:	$t_p^{OR} = 3$ ns
XOR delay:	$t_p^{XOR} = 6$ ns
MUX delay:	$t_p^{MUX} = 4$ ns

FF clock-to-Q delay:	$t_p^{C \to Q} = 2$ ns
FF setup time:	$S = 5$ ns



a. **[4.5 points]** Compute the *maximum* path delays from X_i to D_j for $0 \leq i, j \leq 2$ and enter them in this table. Enter $-\infty$ if there is no path between X_i and D_j.

	D_0	D_1	D_2
X_0			
X_1			
X_2			

b. **[4.5 points]** Compute the *late* arrival times for the three flip-flops.

$A_0 =$ ____

$A_1 =$ ____

$A_2 =$ ____

c. **[1 points]** Compute the minimum clock period P_{min} for error-free operation.

$P_{min} =$ ____

a. **[4.5 points]**

	D_0	D_1	D_2
X_0	$t_p^{MUX} = 4$	$t_p^{XOR} + t_p^{MUX} = 6 + 4 = 10$	$t_p^{OR} + t_p^{XOR} + t_p^{MUX} = 3 + 6 + 4 = 13$
X_1	$-\infty$	$t_p^{XOR} + t_p^{MUX} = 6 + 4 = 10$	$t_p^{OR} + t_p^{XOR} + t_p^{MUX} = 3 + 6 + 4 = 13$
X_2	$-\infty$	$-\infty$	$t_p^{XOR} + t_p^{MUX} = 6 + 4 = 10$

b. **[4.5 points]**

$$A_0 = \boxed{t_p^{C\to Q} + \max(4, -\infty, \infty) = 2 + 4 = 6}$$

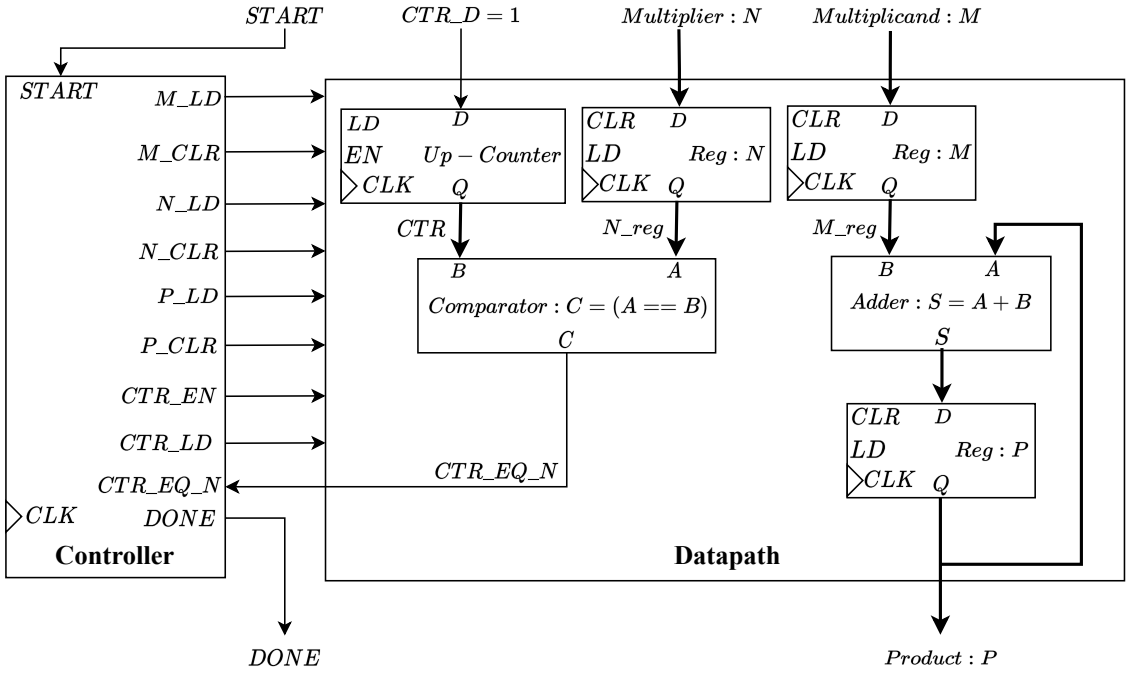
$$A_1 = \boxed{t_p^{C\to Q} + \max(10, 10, \infty) = 2 + 10 = 12}$$

$$A_2 = \boxed{t_p^{C\to Q} + \max(13, 13, 10) = 2 + 13 = 15}$$

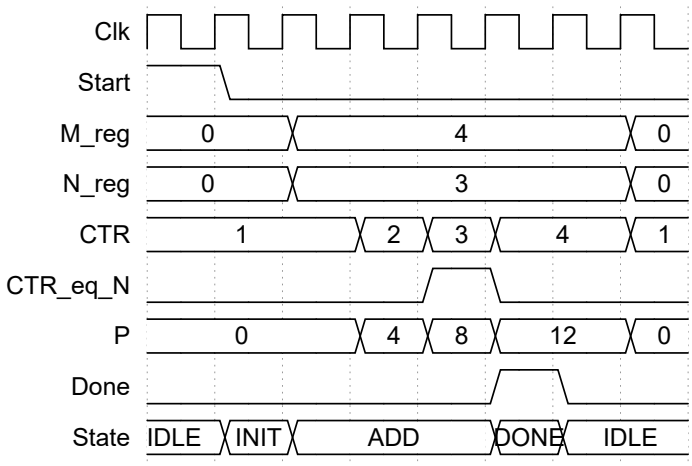
c. **[1 points]** $P_{min} = \boxed{\max(A_0, A_1, A_2) + S = \max(6, 12, 15) + 5 = 20}$

8 [Register Transfer Level Design–18 points]

The following diagram shows an RTL circuit that is meant to perform the unsigned multiplication $P = N * M$ by simply adding the multiplicand M to itself N times. Assume $M > 0$ and $N > 0$. *Hint:* This circuit is quite similar to one you've seen in a quiz.



The multiplier's controller consists of a finite-state machine with 4 states: $IDLE$, $INIT$, ADD, and $DONE$. An example of its operation is shown in the waveform on the right for $N = 3$ and $M = 4$. Only some of the signals are shown; you need to interpret the waveform to complete this problem.

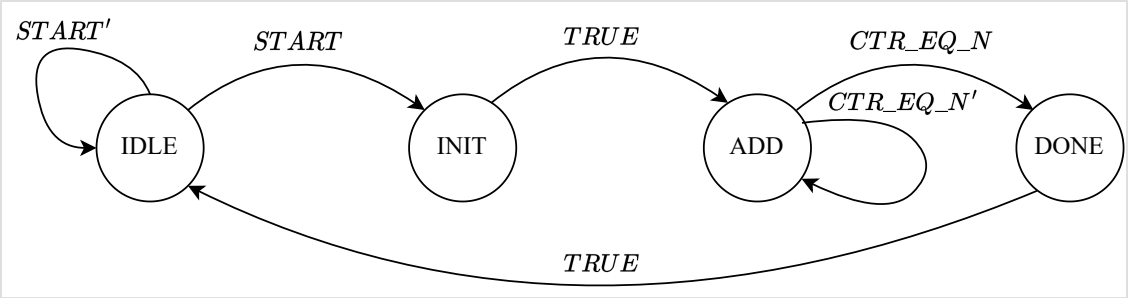


a. **[12 points]** Complete the following state transition diagram. For each transition, draw an arrow connecting the correct states, and label it with its transition condition.

b. **[6 points]** For each of the following control signals, fill in the bubble that represents the state in which the signal should be 1. Unfilled bubbles mean that the signal should remain at 0. *Hint:* You only need to fill in one bubble per row.

Signal	IDLE	INIT	ADD	DONE
M_LD	◯	◯	◯	◯
M_CLR	◯	◯	◯	◯
P_LD	◯	◯	◯	◯
P_CLR	◯	◯	◯	◯
CTR_EN	◯	◯	◯	◯
CTR_LD	◯	◯	◯	◯

a.



One point for each of the state transitions (6) and labels (6)

b.

Signal	IDLE	INIT	ADD	DONE
M_LD	◯	●	◯	◯
M_CLR	●	◯	◯	◯
P_LD	◯	◯	●	◯
P_CLR	●	◯	◯	◯
CTR_EN	◯	◯	●	◯
CTR_LD	●	◯	◯	◯