UNIVERSITY OF MICHIGAN

# EECS 270: Intro to Logic Design

## Midterm Exam 2

**Prof. Karem A Sakallah**

**Monday March 30, 2020**
**6:00-8:00 p.m.**

**A - K: 1013 DOW ‖ L - R: 1014 DOW ‖ S - Z: 1005 DOW**

**Name:** _____

**UMID:** _____

**Honor Pledge:**
"I have neither given nor received aid on this exam, nor have I concealed any violation of the Honor Code."

**Signature:** _____

**Instructions:**

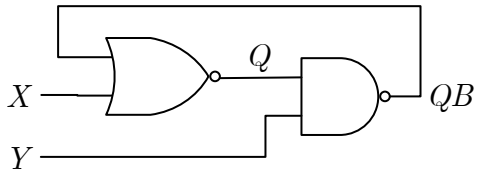
- The exam is closed book except for two 8.5"x11" sheets of notes. No electronics of any kind may be used.
- Print your name and student ID number and sign the honor pledge.
- The exam consists of 6 problems with the point distribution indicated here. Please keep this in mind as you work through the exam. Use your time wisely.
- There are 13 sheets in this exam. Make sure that you have all 13 sheets and notify an instructor if you do not.

| | |
|---|---|
| 1. | /20 |
| 2. | /20 |
| 3. | /20 |
| 4. | /10 |
| 5. | /20 |
| 6. | /10 |
| Total: | /100 |

# 1 [Weird Latches–20 points]

a. **[7 points]**

[6 Points] Complete the function table for this proposed latch.



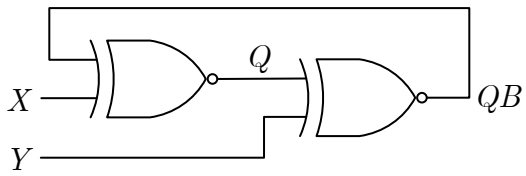

| $X$ | $Y$ | $Q^+$ | $QB^+$ | Function |
|---|---|---|---|---|
| 0 | 0 | | | |
| 0 | 1 | | | |
| 1 | 0 | | | |
| 1 | 1 | | | |

[0.5 Points] Is this a valid latch? _____

[0.5 Points] If not valid, why not? _____

b. **[7 points]**

[6 Points] Complete the function table for this proposed latch.




| $X$ | $Y$ | $Q^+$ | $QB^+$ | Function |
|---|---|---|---|---|
| 0 | 0 | | | |
| 0 | 1 | | | |
| 1 | 0 | | | |
| 1 | 1 | | | |

[0.5 Points] Is this a valid latch? _____

[0.5 Points] If not valid, why not? _____

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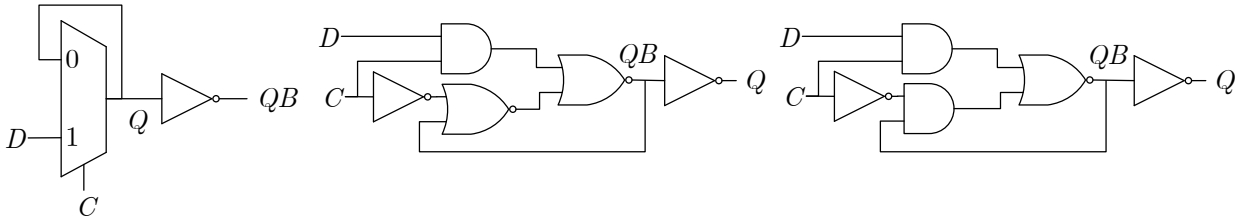
c. **[6 points]** Circuits 1, 2, and 3 below are proposed as possible implementations of a D latch. Which of the following statements is true?




(1) (2) (3)

(a) Only one of the circuits is a D latch.

(b) Only circuits 1 and 2 are D latches.

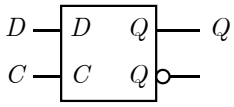
(c) Only circuits 2 and 3 are D latches.

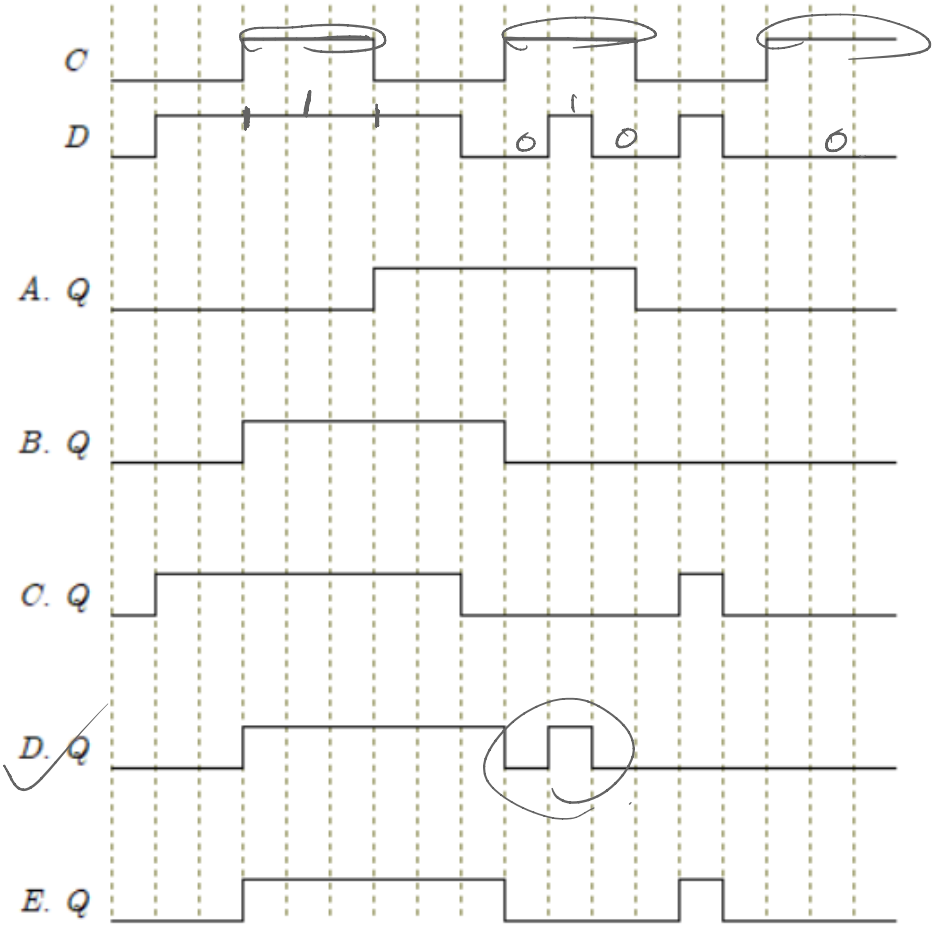
(d) Only circuits 1 and 3 are D latches.

(e) All three circuits are D latches.

## 2 [Timing Analysis–20 points]

a. **[4 points]** Consider the positive level-sensitive D latch shown below along with the given waveforms for its $C$ and $D$ inputs. Which of the following choices is the correct response at the output $Q$? You may ignore propagation delays.

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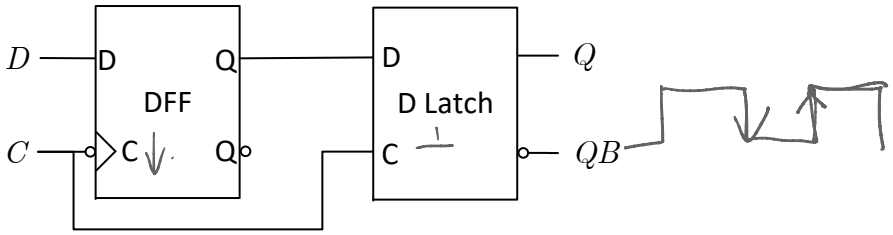
B

b. **[4 points]** Consider the back-to-back negative edge-triggered flip-flop and positive level-sensitive latch shown here as a *single flip-flop*. Let $C \uparrow$ and $C \downarrow$ denote, respectively, the rising and falling edges of the clock input $C$. Let $S$ and $H$ denotes the setup and hold constraints. Which of the following statements is true?




(a) $S$ and $H$ must be checked against $C \uparrow$; Q changes shortly after $C \uparrow$.

(b) $S$ and $H$ must be checked against $C \downarrow$; Q changes shortly after $C \uparrow$.

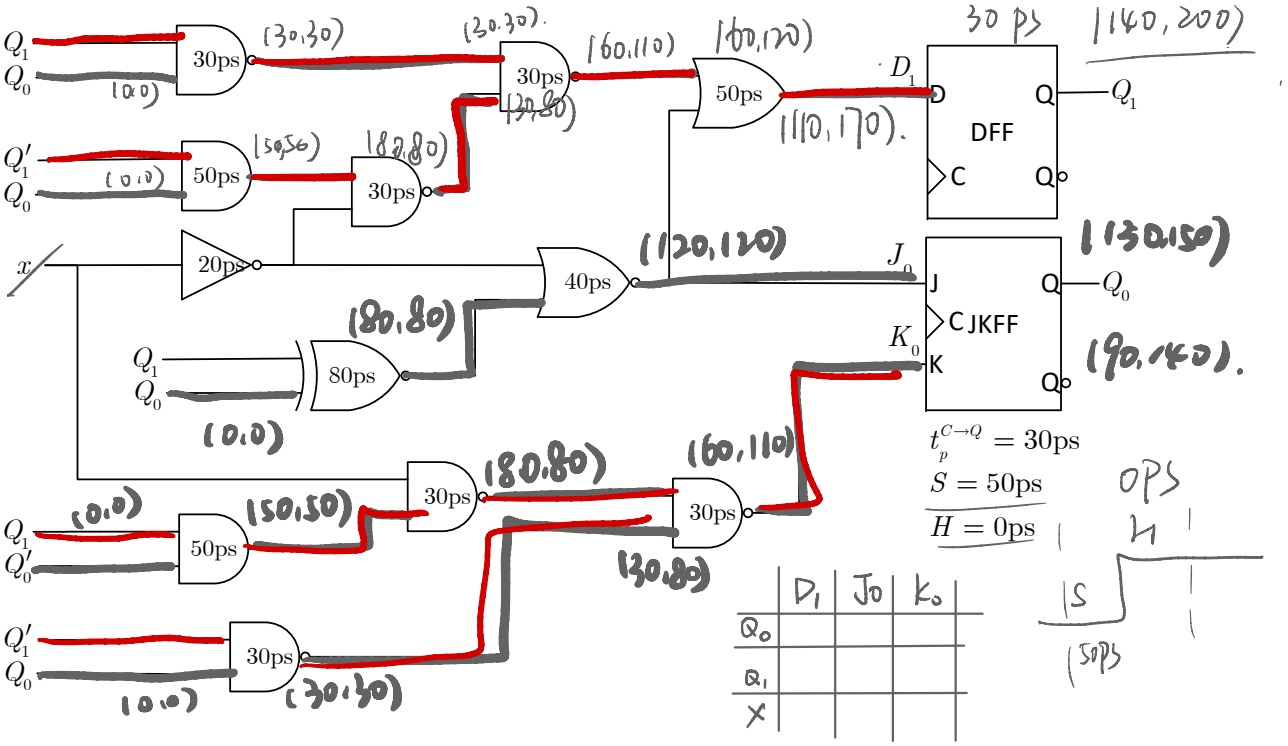
(c) $S$ and $H$ must be checked against $C \downarrow$; Q changes shortly after $C \downarrow$.

(d) $S$ and $H$ must be checked against $C \uparrow$; Q changes shortly after $C \downarrow$.

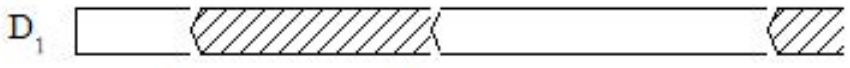
(e) $S$ must be checked against $C \uparrow$, and $H$ against $C \downarrow$; Q changes shortly after $C \downarrow$.

*Continued on next page*

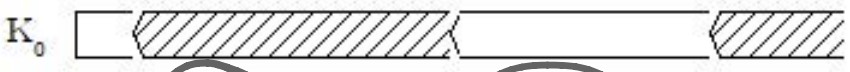
c. **[12 points]** Annotate the waveforms for $D_1$, $J_0$, and $K_0$ in the following sequential circuit with their early $a$ and late $A$ arrival times and calculate the maximum frequency that allows this circuit to operate without timing violations. *Note that waveform transitions in the timing diagram are not meant to be exact, just representative.*












$f_{max} =$ 200+50 = 250 ns. $f_{max} = \frac{1}{250ns} = 4GHz$.

# 3 [Two-level Minimization–20 points]

a. **[6 points]** Which of the following K-maps is for a function that has no essential prime implicants in a minimal SOP expression for the function?

A.

| $ab$ \ $cd$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | | |
| 01 | | | | |
| 11 | 1 | | | 1 |
| 10 | 1 | | | 1 |

B.

| $ab$ \ $cd$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | 1 | |
| 01 | | | 1 | |
| 11 | | 1 | 1 | |
| 10 | | 1 | | |

C.

| $ab$ \ $cd$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | 1 | |
| 01 | | | | |
| 11 | | 1 | 1 | 1 |
| 10 | 1 | | 1 | |

D.

| $ab$ \ $cd$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | 1 | |
| 01 | | | | |
| 11 | 1 | 1 | | 1 |
| 10 | 1 | | 1 | |

E.

| $ab$ \ $cd$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | 1 | |
| 01 | | | 1 | |
| 11 | | 1 | 1 | |
| 10 | 1 | 1 | | |

Answer: _____

b. **[6 points]** Find minimal SOP and POS solutions for the function $f(w, x, y, z)$ whose K-map is shown below.

| $wx$ \ $yz$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 0 | X |
| 01 | 0 | 1 | 0 | 0 |
| 11 | 0 | X | X | X |
| 10 | 1 | X | 0 | 0 |

$f^{\text{SOP}}(w, x, y, z) =$ _____

$f^{\text{POS}}(w, x, y, z) =$ _____

c. **[8 points]** Consider the function $g(a, b, c, d)$ whose K-map is shown below.

| $ab$ \ $cd$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 1 |
| 01 | 1 | 0 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 0 |

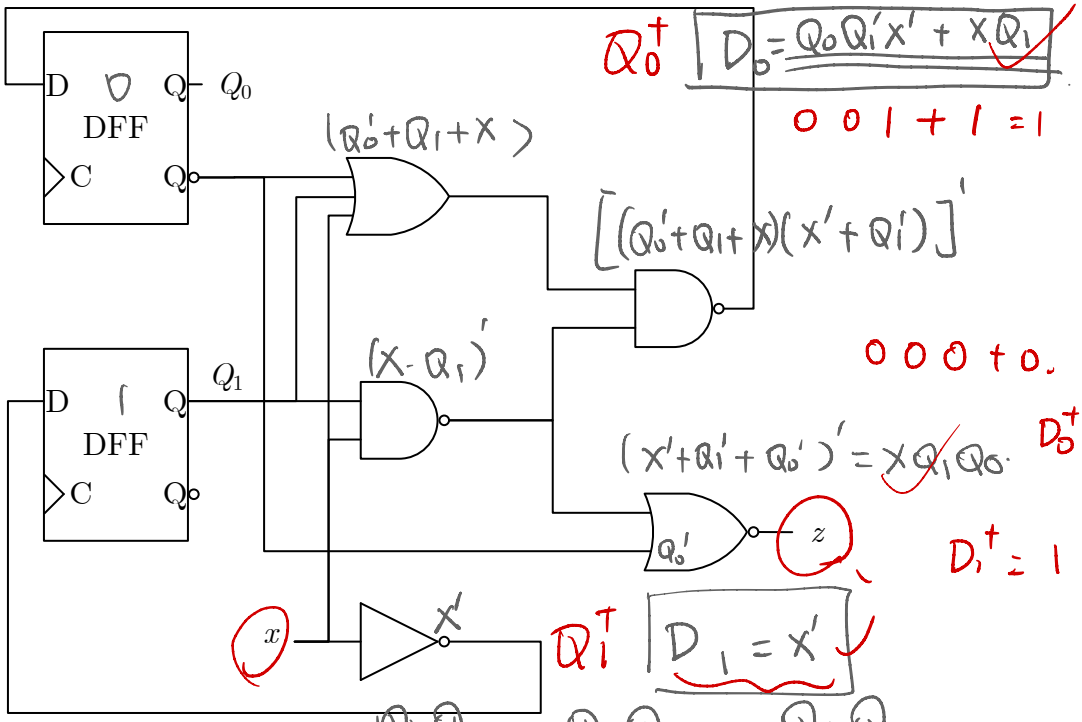
[4 Points] How many prime implicants does $g$ have? _____

[2 Points] How many essential prime implicants does $g$ have? _____

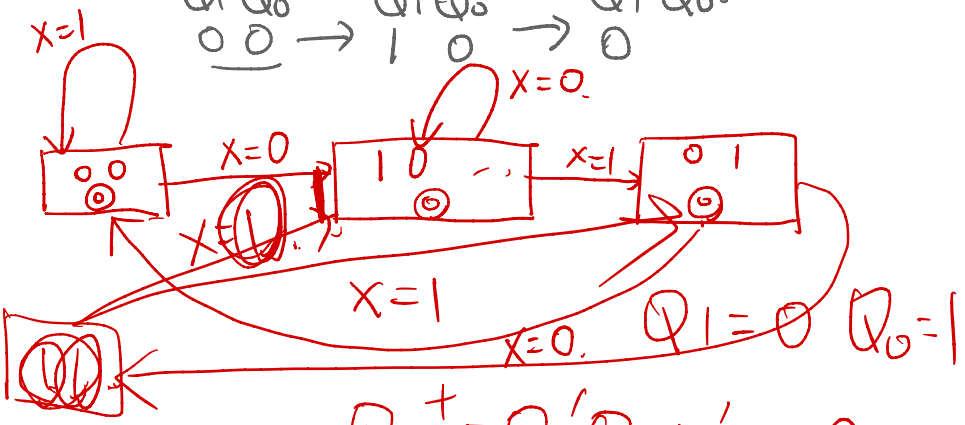
[2 Points] The number of literals in the minimal POS solution for $g$ is: _____

## 4 [Sequential Circuit Analysis–10 points]

a. **[2 points]** The following sequential circuit sets its output $z$ to 1 when the appropriate secret code is entered on its input line $x$. Your job is to figure out what that secret code is! Assuming that the circuit is reset to state $Q_1Q_0 = 00$ before application of any input, which of the following choices is the secret code?




(a) 0101
(b) 1010
(c) 1101
(d) 0110
(e) 0100

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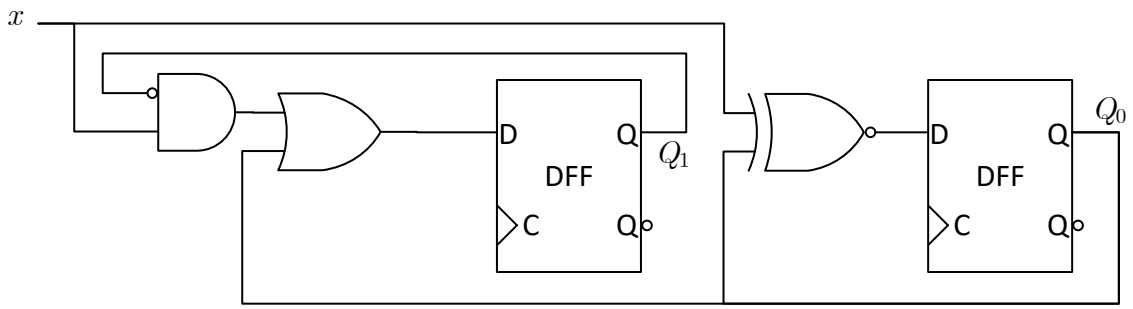
b. **[8 points]** Given the state assignment

| $Q_1Q_0$ | State Label |
|---|---|
| 00 | $A$ |
| 01 | $B$ |
| 10 | $C$ |
| 11 | $D$ |

derive the state table for the following synchronous sequential circuit.




| Present State | $x = 0$ | $x = 1$ |
|---|---|---|
| $A$ | | |
| $B$ | | |
| $C$ | | |
| $D$ | | |

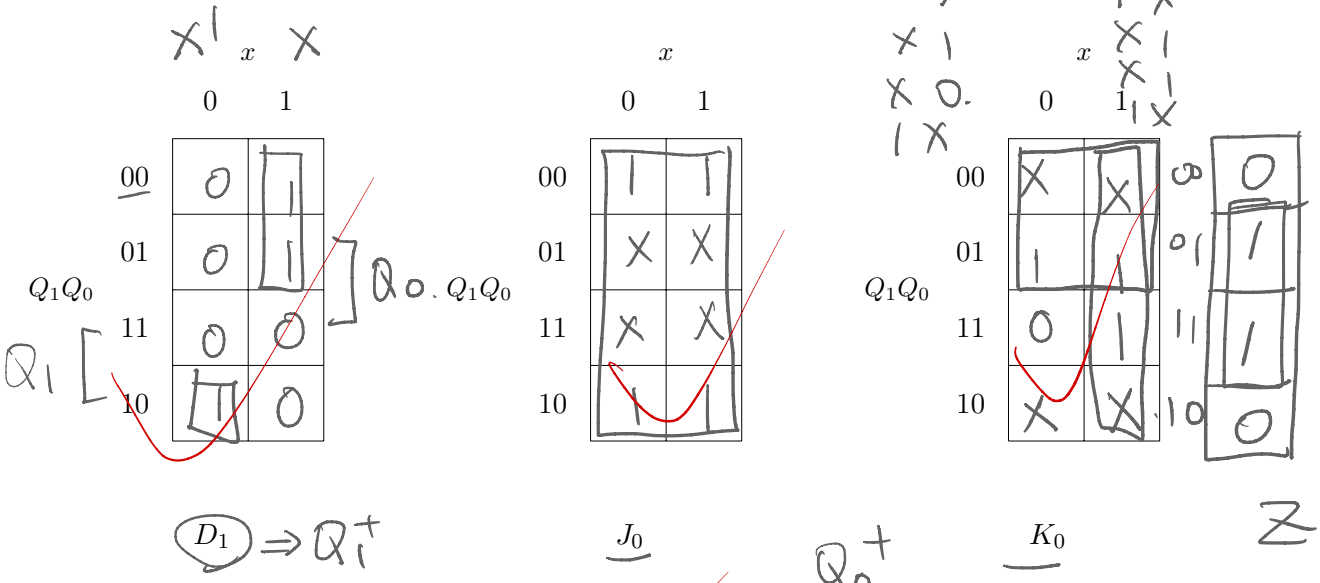
Next State

## 5 [Sequential Synthesis–20 points]

Complete the design of the sequential circuit which is described by the following transition and output table:

| $Q_1Q_0$ | $x=0$ | $x=1$ | $z$ |
|---|---|---|---|
| 00 | 01 | 11 | 0 |
| 01 | 00 | 10 | 1 |
| 11 | 01 | 00 | 1 |
| 10 | 11 | 01 | 0 |
| | $Q_1^+Q_0^+$ | | |

[12 Points] Using a $D$ flip-flop for $Q_1$ and a $JK$ flip-flops for $Q_0$, complete the following K-maps and derive minimal SOP solutions for $D_1$, $J_0$, $K_0$, and $z$.




[2 Points] $D_1^{\text{SOP}}(x, Q_1, Q_0) =$ _____

[2 Points] $J_0^{\text{SOP}}(x, Q_1, Q_0) =$ _____

[2 Points] $K_0^{\text{SOP}}(x, Q_1, Q_0) =$ _____

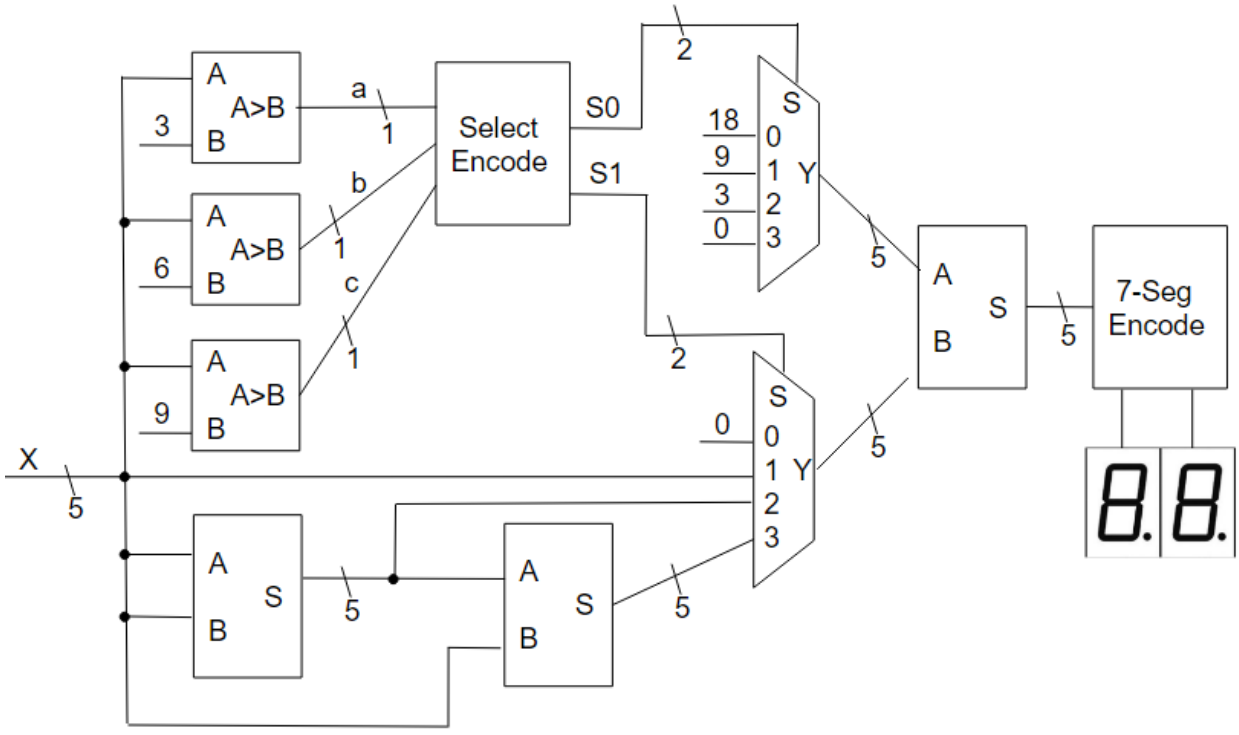
[2 Points] $z^{\text{SOP}}(x, Q_1, Q_0) =$ _____

# 6 [Lab Experience–10 points]

You are given the task of implementing a piecewise linear function in hardware for fast computation. It consists of 4 continuous functions. You start simple by limiting the input ranges as follows:

| | |
|---|---|
| y = 3x | x = 0 - 3 |
| y = 2x + 3 | x = 4 - 6 |
| y = x + 9 | x = 7 - 9 |
| y = 18 | x = 10 - 31 |

The FPGA and tools you are using will only synthesize adders, multiplexers, comparators and various combinational logic. Given these restrictions you come up with the following design that uses 5-bit comparators, 5-bit adders, 5-bit multiplexers and various logic. You can assume input x is limited to the unsigned integers 0 to 31.




Complete the following Verilog that implements this design. You will need to complete some declarations, connections between modules, the 5-bit 4 to1 multiplexer and the select encode module. You can assume the 5-bit adder, 5-bit comparator and 7-segment encoder are provided.
Point values are listed on each line for a **total of 10 points**.

```
module pwf(x, y10, y1);

input [4:0] x; //argument x
output [5:0] y10, y1; //7seg display


_____________________ a,b,c;                                  (1 point)
_____________________ s0, s1;                                 (1 point)
_____________ _______ sum2x, sum3x, y0, y1,  y;               (1 point)


five_bit_comparator c0(_____________________);                (0.5 point)
five_bit_comparator c1(_____________________);                (0.5 point)
five_bit_comparator c2(_____________________);                (0.5 point)
select_encode e0(a, b, c, s0, s1);

five_bit_adder a0(_________________________);                 (0.5 point)
five_bit_adder a1(_________________________);                 (0.5 point)
five_bit_4to1mux m0(0, 3, 9, 18, y0);
five_bit_4to1mux m1(0, x, sum2x, sum3x, y1);
five_bit_adder a2(y0, y1, y);
seven_seg_encoder e1(y, y1, y10); //
endmodule


_____________________________(a,b, c, s0, s1);              (0.5 point)
input a, b, c;
output [1:0] s0, s1;

assign s0[0] = _____________________________;                 (0.5 point)
assign s0[1] = _____________________________;                 (0.5 point)
assign s1[0] = _____________________________;                 (0.5 point)
assign s1[1] = _____________________________;                 (0.5 point)
endmodule

_____________________________(a0, a1, a2, a3, sel, y); (0.5 point)
input [4:0] a0, a1, a2, a3;
input [1:0] sel;
output [4:0] y;

_______________ = (sel == 0) ? a0:                            (0.5 point)
                  (sel == 1) ? _________________:             (0.5 point)
                  (sel == 2) ? _________________:             (0.5 point)
endmodule
```