$P = P_{SWITCH} + P_{SHORT} + P_{LEAK}$

$P_{SWITCH} = C \cdot V_{DD}^2 \cdot f \cdot A$

$P_{SHORT} = b/12 \cdot (V_{DD} - 2 \cdot VT)^3 \cdot f \cdot A \cdot t$

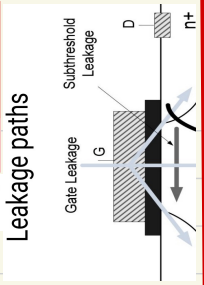
$P_{LEAK} = V_{DD} \cdot (I_{SUB} + I_{GATE} + I_{JUNCTION} + I_{GIDL})$

If utilization < ~80%, drop V, f.

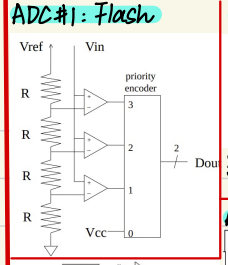
If utilization > ~80%, increase V, f.

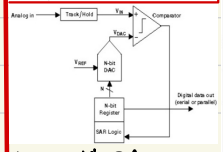
$I_{subthreshold} = A_S \, W/L \, v_T^2 \, (1 - \exp(-V_{DS}/v_T)) \cdot \exp((V_{GS} - V_{th}) / n v_T)$

温度越高，越明显.

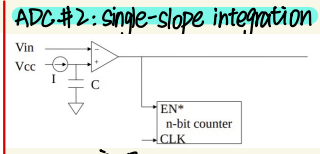


ADC#1：Flash



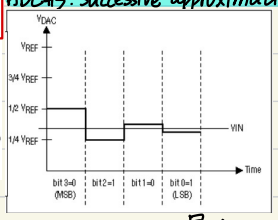


ADC#2：Single-slope integration



缺点：速度慢 . $O(2^n)$

ADC#3：Successive approximation

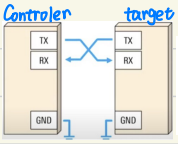


优点：快 $O(n)$

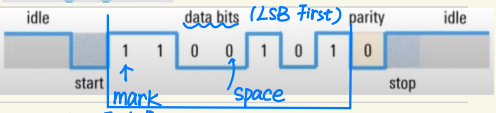
从MSB开始试，试到LSB，找到和Vin最接近的.

UART（2条线）（中等速度）

① Asynchronous ② half / full-duplex ③ data按frame



须知有统一的收发频率：baud rates



parity bit 的分类：

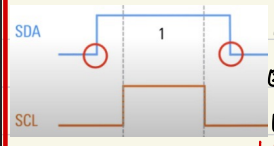
① Even parity：若"1"是even个，则是0.

② Odd parity：若"1"是odd个，则是0.

I^2C（2条线）

① Synchronous ② half-duplex ③ 先传地址后传value

SDA和SCL变化的相对位置关系.

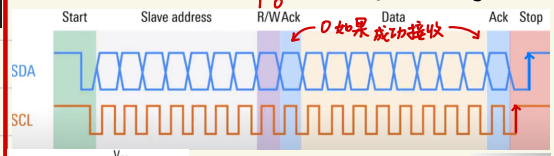


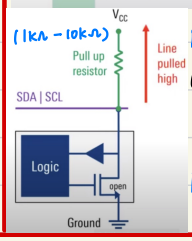
时变化.

① Start或Stop时SDA会在SCL高

② 剩下只在SCL低的时候变化.

③ 不在rousing / failing edge变化.



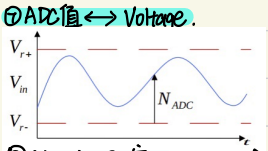


pull up resistors大小会影响什么

① R↑：↑pull up line的时间，限制了bus的计算速度，但节省了power

pull up时间：bus capacitance和pull up resistor有关.

① ADC值 ⟷ Voltage.



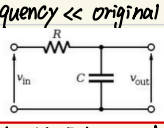
$N_{ADC} = 4095 \times \frac{V_{in} - V_{r-}}{V_{r+} - V_{r-}}$

$V_{in} = N_{ADC} \times \frac{V_{r+} - V_{r-}}{4095}$

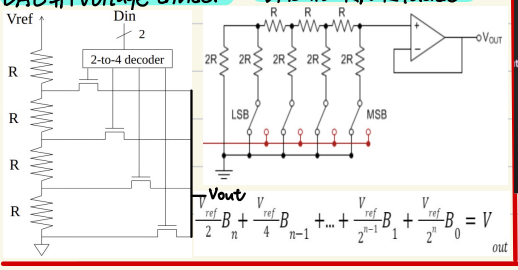
② Aliasing的定义：Sample frequency << original frequency

导致采样结果不真实似频.

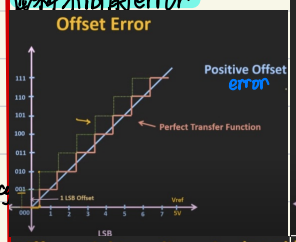
解决方法：low-pass filter

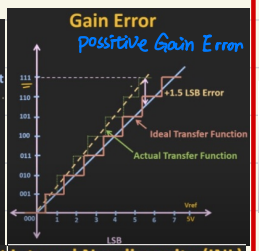


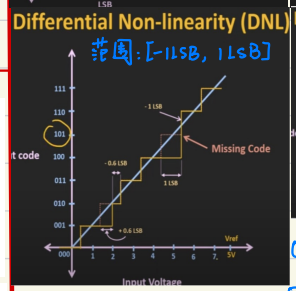
DAC#1 Voltage divider　DAC#2 R/2R ladder

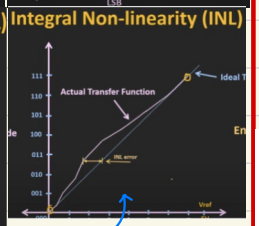


③ 种不同的error









INL有两种测量方法：

① Endpoint Method.

② Best fit Method.

法②保证一定比DNL Error小.

---

① Range 太小 ⟶ clipping　ADC & DAC

② Resolution：能用多少 discrete value 来表示 a range of analog value . Eg: 12 bit ADC 就是 4096.

③ step_size = Range / Resolution

④ Quantization Error：step_size /2 = Range /2× resolution

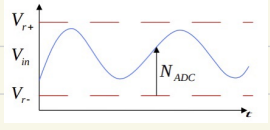
⑤ Shannon-Nyquist

$f_{sample} > 2 f_{max}$

⑥ Compressed Sensing：

有时我们也可使用低于Shannon的 frequency 采样，前提是了解 predictable properties of signal

① ADC值 ⟷ Voltage.



$N_{ADC} = 4095 \times \frac{V_{in} - V_{r-}}{V_{r+} - V_{r-}}$

$V_{in} = N_{ADC} \times \frac{V_{r+} - V_{r-}}{4095}$

PCB

① Traces：连接的细线

② Vias：用于连接不同层的小孔

1) Through-hole vias

2) Buried vias

3) Blind vias

③ SilkScreen：用于标记的白线

④ Solderpad：露出用于Solder元件的空位

Design Process

1. Create Schematic
2. Place Parts
3. Board Design
4. Generate Files

Prototyping

options

① Breadboard 优点：快，简单

缺点：• low-frequency <=1MHz (容抗效应)

• Nasty parasitics

② Soldering

• Sheath：焊枪外壳，使用前查看。

• desoldering的工具有：solder sucker / wick (带状金属)

• Salammoniac：用于除电烙铁前端氧化 (水对脂) • Rosin can etch iron (腐蚀)

• 使用 sponge (海绵) scrubber (刷子) tinning block 用于除去iron表面solder

• 在 traces 和 leads 上的 deposits 会影响 capillary action (毛细作用) (浸入)

• Iron 要 preheat traces，leads 使得 solder wick into junction

• 希望得到的最终形状：Spires。

③ Wire wrap

noise 产生的原因

① Capacitive Coupling：产生的原因有

• 将两个 wire 距离很近的并排放置。

• 将低压信号和高压信号放置过近

有时我们也需要利用 Capacitive Coupling 可在 Radio Frequency Circuit 中更高效。

② Motors & Solenoids & mechanical relays

解决方法：① 将 noise 和 Computer 相隔离。

② 使用 idependent power supplies。

③ Opto-isolators。

导线的种类：

Coaxial Cables：有很强的 interference resistance

outer jacket / braid shield / foil shield / dielectric / center conductor

Twisted pair：有很强的 noise resistance。因为其相互缠绕的结构抵消了 magnetic field 所带来的影响

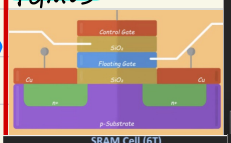
ESD：Electrostatic discharge.

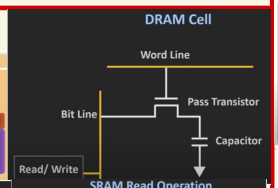
① High potential difference 会增加 momentary current (瞬时电流) locations

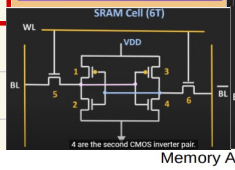
② 会击破 oxide 并 erase non-volatile memory

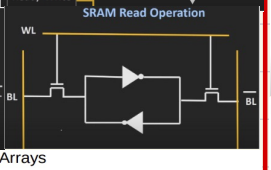
会引起 consistent faults.（不常见 intermittent fault）

FGMOS









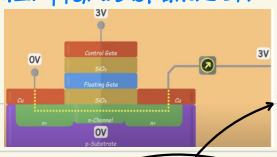
memory

Memory Arrays

- Random Access Memory
  - Read/Write Memory (RAM) (Volatile)
    - Static RAM (SRAM)
    - Dynamic RAM (DRAM)
  - Read Only Memory (ROM) (Nonvolatile)
    - Mask ROM（永远改不了）
    - Programmable ROM (PROM)（只能写一次）
    - Erasable Programmable ROM (EPROM)（使用 ultraviolet light 给 electron 足够能量）
    - Electrically Erasable Programmable ROM (EEPROM)
    - Flash ROM（移除时以 Chunk 为单位）
- Serial Access Memory
  - Shift Registers
    - Serial In Parallel Out (SIPO)
    - Parallel In Serial Out (PISO)
  - Queues
    - First In First Out (FIFO)
    - Last In First Out (LIFO)
- Content Addressable Memory (CAM)

wear leveling

检测 FGMOS 存储的是什么。

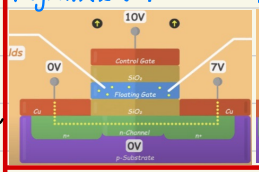


• 有电流就是"1"

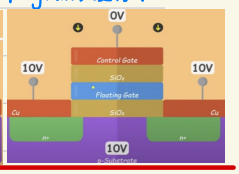
• 没有电流就是"0"

Fowler-Nordheim tunneling

Program 其变为 0.

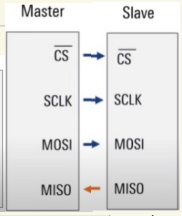


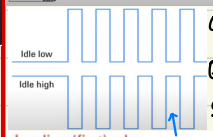
Program 其变为 1



SPI（四条线）② faster

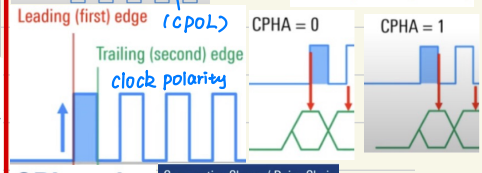
① Synchronize ② full-duplex





① Clock can idle low / idle high

② Data 可以在 rising / falling 被 sample. CPHA (clock phase)



SPI modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1