EECS 270 Fall 2021

Homework 5

Due Friday, October 29 @ **5:00 PM** on Gradescope

This is an individual assignment, all of the work should be your own.
Write neatly or type and show all your work for full credit.
Have your name and unique name on the front page of your submission.

d)

Current state Q_1Q_0		Input A,B: $A'B'$ (00)	$A'B$ (01)	AB' (10)	AB (11)	output YZ
0 0	A	C 1 0	C 1 0	A 0 0	A 0 0	0 1
0 1	B	A 0 0	A 0 0	A 0 0	A 0 0	1 *0
1 0	C	B 0 1	A 0 0	D 1 1	C 1 0	1 0
1 1	D	B 0 1	A 0 0	B 0 1	A 0 0	1 0
		$Q_1^+Q_0^+$	$Q_1^+Q_0^+$	$Q_1^+Q_0^+$	$Q_1^+Q_0^+$	
		$B'=1$	$B'=0$	$B'=1$	$B'=0$	

State	State variable
A	0 0
B	0 1
C	1 0
D	1 1

b) $Q_0^+ = D_0 = (Q_1' + B)' = Q_1 B'$

$Q_1^+ = D_1 = (A \odot Q_1) \cdot Q_0'$

c) $Y = Q_1 + Q_0$

$Z = Q_1' + Q_0'$ ~~$Z = Q_1' Q_0'$~~

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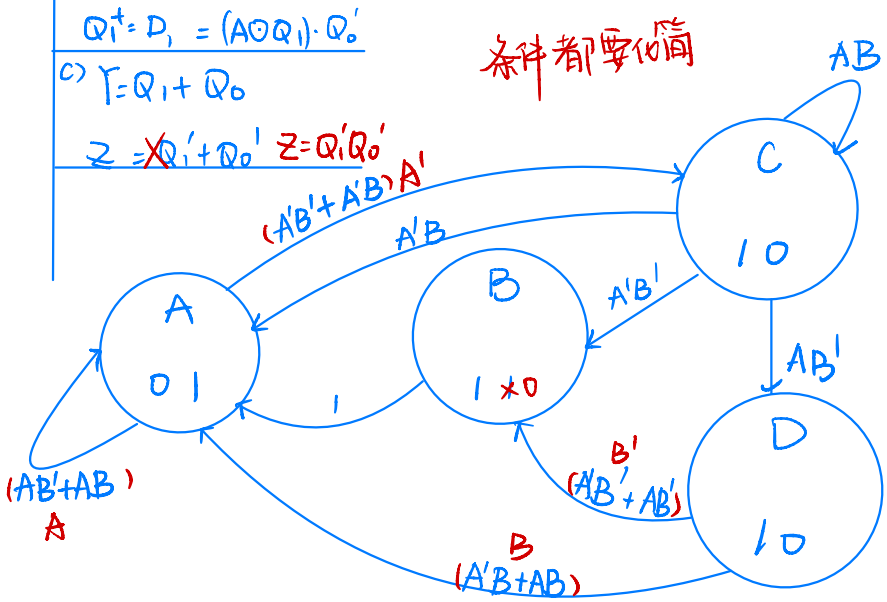


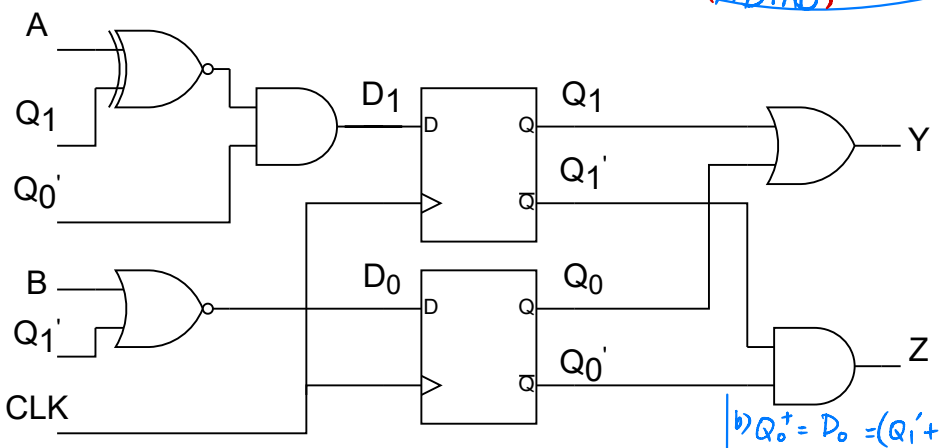


Figure 1: Sequential circuit using D flip-flops.

b) $Q_0^+ = D_0 = (Q_1' + B)' = Q_1 B'$

$Q_1^+ = D_1 = (A \odot Q_1) \cdot Q_0'$

c) $Y = Q_1 + Q_0$

$Z = Q_1' + Q_0'$

a. **[5]** Is this a Moore or a Mealy machine? Mealy
b. **[5]** Find the excitation/transition equations of the two flip-flops.
c. **[5]** Find the output equations.
d. **[5]** Create the transition/output table
e. **[5]** Draw the state diagram. Please label the states (00 = A, 01 = B, 10 = C, 11 = D).

3. **[25 points]** *State Machine Design:* You are designing a Moore state machine with two inputs, *A* and *clk*, and two outputs *X*, *Y*. The *A* input is latched on the rising edge of *clk*. The *X* output is 1 when the last three *A* inputs are 011 (*e.g.* a 0 was input first, then a 1, then another 1). The *Y* output is 1 when the last three *A* inputs are 010.

   a. **[5]** Draw a state diagram, ignoring *clk*. *Hint: use 8 states, one for each binary combination.*

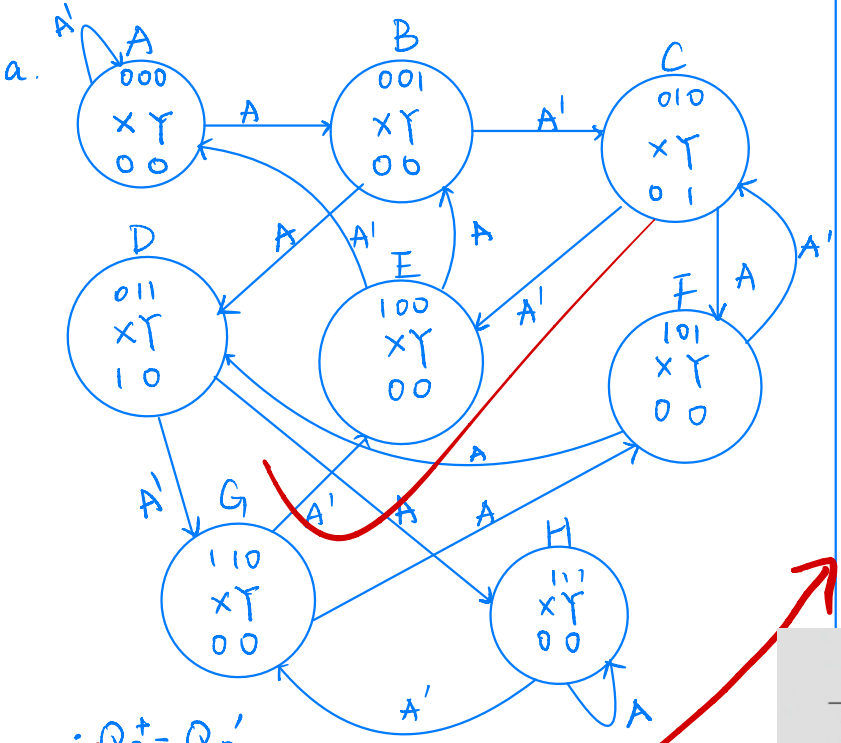
   b. **[5]** Derive the state table, ignoring *clk*.

   c. **[5]** Using the straightforward state assignment (*i.e.*, 000 for an input sequence of 000, 001 for a sequence of 001, etc), derive the next state equations for each bit, ignoring *clk*.

   d. **[5]** Determine the output equations, ignoring *clk*.

   e. **[5]** Draw a circuit using D flip-flops to implement your design, include *clk*.

a.



b)

S	Input A = 0	Input A = 1	X Y output
A	A	B	00
B	C	D	00
C	E	F	01
D	G	H	10
E	A	B	00
F	C	D	00
G	E	F	00
H	G	H	00

b.

$Q_2Q_1Q_0$	$D_2D_1D_0$ A'	$D_2D_1D_0$ A	Output X	Output Y
000	000	001	0	0
001	000	001	0	0
010	100	101	0	1
011	100	101	1	0
100	000	001	0	0
101	000	001	0	0
110	100	101	0	0
111	100	101	0	0

$Q_0^+ = A$
$Q_1^+ = Q_0$
$Q_2^+ = Q_1$

c) $Q_2 Q_1 Q_0$

000
001
010
011
100
101
110
111

- $Q_0^+ = Q_0'$
- $Q_1^+ = Q_1 \oplus Q_0$
- $Q_2^+ = Q_1 \oplus (Q_0 Q_1)$

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d) output equation:

$X = Q_2' Q_1 Q_0$

$Y = Q_2 Q_1 Q_0'$

e)