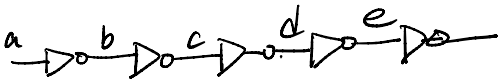
EECS 270 Fall 2021

Homework 2

Due Friday, September 17 @ **5:00 PM** on Gradescope

This is an individual assignment, all of the work should be your own.
Write neatly or type and show all your work for full credit.
Have your name and unique name on the front page of your submission.

Total Points: 60

1. **[10 points]** *Ring Oscillator:* Answer the following questions. 

   a. (5 pts) What is the average period and frequency of a 5-gate ring oscillator with a gate delay of 2 ns for both rising and falling edges?
   b. (5 pts) What is the average period and frequency of a 9-gate ring oscillator with a gate delay of 2 ns for rising edge and 1 ns for falling edge?

Questions continue on the next page.

a) period:
$2 \times 5 \times 2\,ns = 20\,ns$
frequency:
$\frac{1}{20 \times 10^{-9}\,s} = 0.5 \times 10^{8}\,Hz$
$= 5 \times 10^{7}\,Hz$ 50 MHz

b) period.
$9 \times (2+1) = 27\,ns$

frequency:
$\frac{1}{27 \times 10^{-9}\,s} = 3.7 \times 10^{7}\,Hz$ 37 MHz.

2. **[20 points]** *Max Circuit Frequency:* FPGAs can be designed as a series of re-configurable look-up tables (LUTs) to implement digital circuits. A simple LUT can be made with a series of MUXs. Use Figures 1 and 2 and Table 1 to answer the following questions.

   a. (8 pts) What is the longest possible propagation delay for the MUX?

   b. (2 pts) Using your value for part *a*, what is the maximum frequency a single MUX could be safely "clocked" at?

   c. (8 pts) What is the longest possible propagation delay for the LUT?

   d. (2 pts) Using your value for part *c*, what is the maximum frequency that the LUT could be safely "clocked" at?

Gate	Delay (ns)
NOT	1
OR	3
AND	4

Table 1: Gate delay times for problems 2a and 2b. Assume the same delay for rising and falling edges.

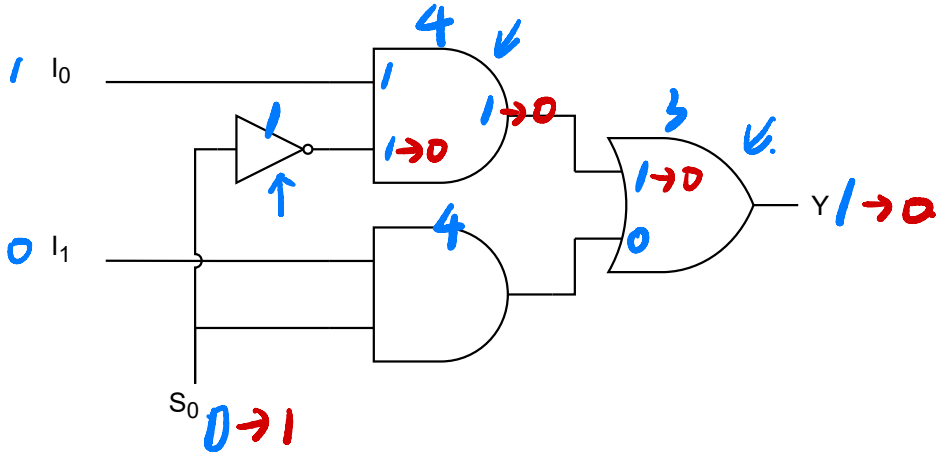


Figure 1: A 2-to-1 MUX diagram for questions 2a and 2b.

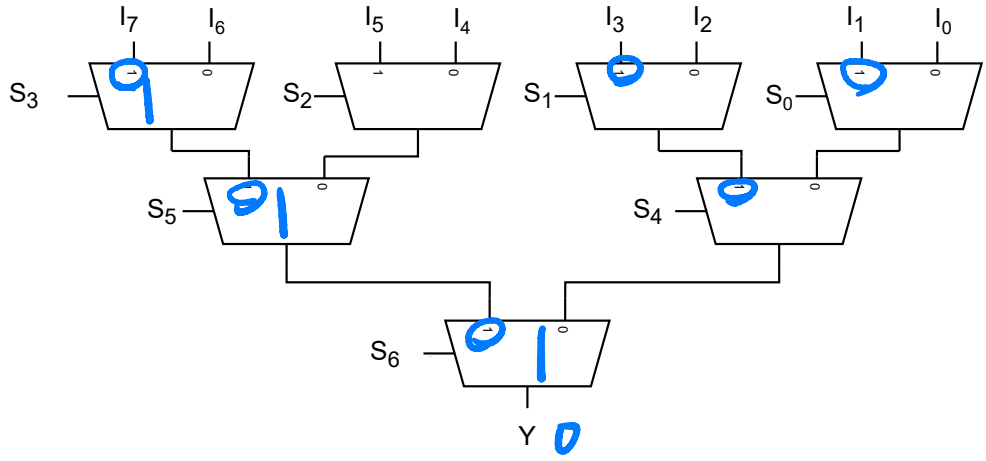


Figure 2: A 8-to-1 LUT diagram for questions 2c and 2d.

Questions continue on the next page.

3. **[30 points]** *Timing Diagrams*

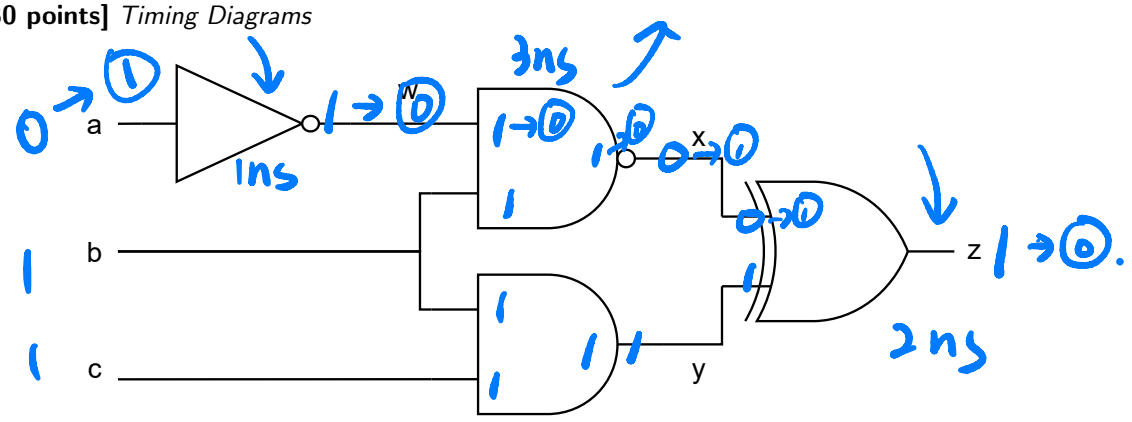
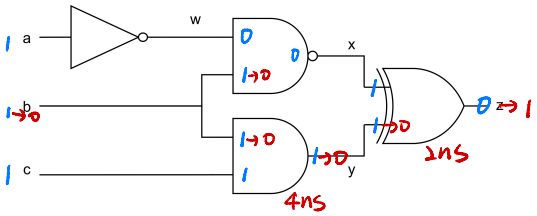


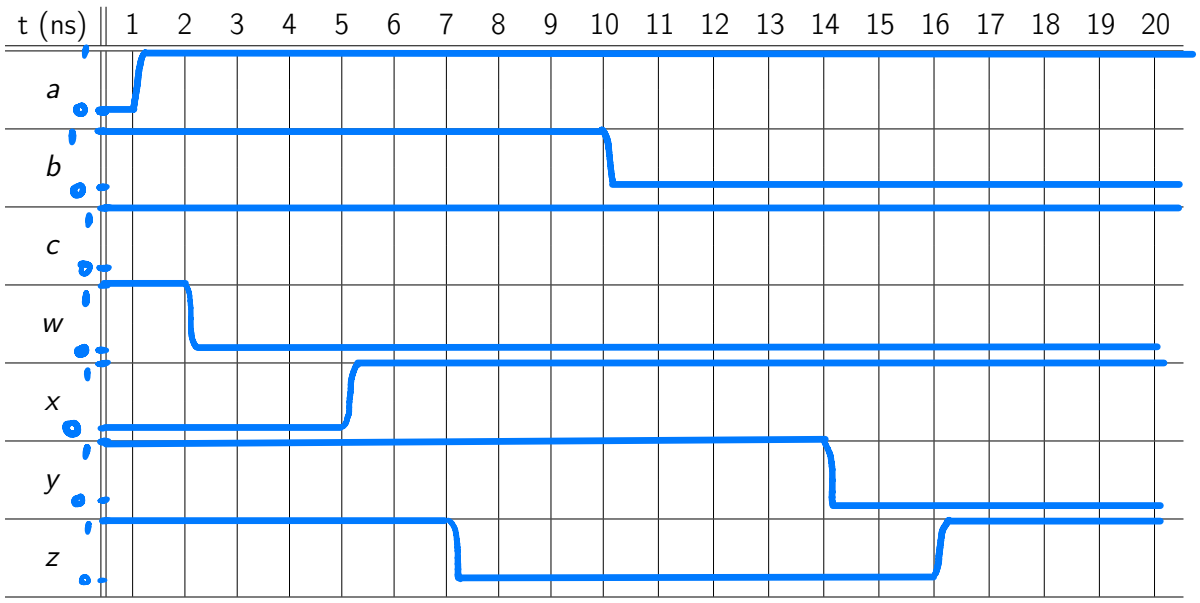
Figure 3: Circuit used for question 3a and 3b.



Gate	Delay (units)
NOT	1
XOR	2
NAND	3
AND	4

Table 2: Gate delay times for problem 3a and 3b. Assume the same delay for rising and falling edges.

a. (20 pts) Draw a timing diagram for *a*, *b*, *c*, *w*, *x*, *y* and *z* for circuit in Figure 3 and delays in Table 2. Please show the causality arrows. Assume *a* has been zero for a long time, while *b* and *c* have been 1 for a long time. At t=1, *a* transitions from $0 \rightarrow 1$. Then at t=10, *b* transitions from $1 \rightarrow 0$.



b. (10 pts) Perform a timing simulation for the circuit in Figure 3 with delays in Table 2 in modelsim using the test cases listed in Table 3. Do each test case in the listed order with a 10 ns delay between each case. Save an image of the simulation. Then draw causality arrows on the image (using any image editing program you wish to use).

a	b	c
0	1	1
1	1	1
1	0	1
0	1	1

Table 3: Test cases for problem 3b.