1. Identify the primary states associated with the cash register and list the cycles numbers associated with them.

	primary states	cycles numbers
A. LoadX	3'd1	2.5.8
B. AddX	3'd2	3.6.9
C. MoreX	3'd3	4.7.10
D. LoadT	3'd4	11.
E. DisplayTotal	3'd5	12. 13

2. Take a look at the simulation and notice that the registers are loaded after their respective load signals go low. Why is this? Hint: Consider the synchronous (clock driven) operation of the A register.

Since inputs must be synchronized with the system clock before being applied to a synchronous system and the registers are made of D flip flops. So the outputs of registers can only change when the system clock go from 0 to one which means the rising edge of the clock. So even if the load signals go low, the registers still need to wait the rising edge of the system signal.

3. Modify the testbench to provide the scenario 1+2+3+4 and submit the waveform with the correct sum.