

$$\Sigma_{a,b,c,d} (0, 2, 5, 6, 7, 8, 10, 14)$$

0000, 0010, 0101, 0110, 0111,
1000, 1010, 1110

EECS 270 Fall 2021

Homework 6

Due Friday, November 5 @ 5:00 PM on Gradescope

This is an individual assignment, all of the work should be your own.

Write neatly or type and show all your work for full credit.

Have your name and unique name on the front page of your submission.

$$f = cd' + d'b' + db'a'$$

$$= cd' + b'd' + \cancel{abd}$$

$$= cd' + b'd'$$

$$f = bd' + dc' + bd + dc'b$$

$$= ab + c'd + bd + bc'd'$$

Total Points: 115

$\Sigma_{a,b,c,d} (0, 3, 8, 10, 11, 14)$

0000, 0011, 1000, 1010, 1011, 1110

1. [20 points] *K-maps:* Using K-maps, find the minimal SOP and POS equations for the following functions.

- [10] $f(a, b, c, d) = \sum_{a,b,c,d}(0, 2, 5, 6, 7, 8, 10, 14)$
- [10] $f(a, b, c, d) = \prod_{a,b,c,d}(0, 3, 8, 10, 11, 14) + d(2, 5, 7, 15)$

$$f = bc' + dc' + bd'$$

$$= bc' + c'd + a'b$$

2. [30 points] *Sequential Circuit Analysis:* Analyze the sequential circuit shown in Figure 1. Note that equations do not need to be simplified, flip-flop outputs Q_0 and Q_1 are fed back as inputs to the circuit on the left, and A also appears to the right of the flip-flops.

$$f = (a+d)(b'tc+d)$$

$$(a+bt+d)$$

因为两个
2x2重叠。

$$f = b'd + ad + b'd'c'$$

$$= b'd + ad + bc'd'$$

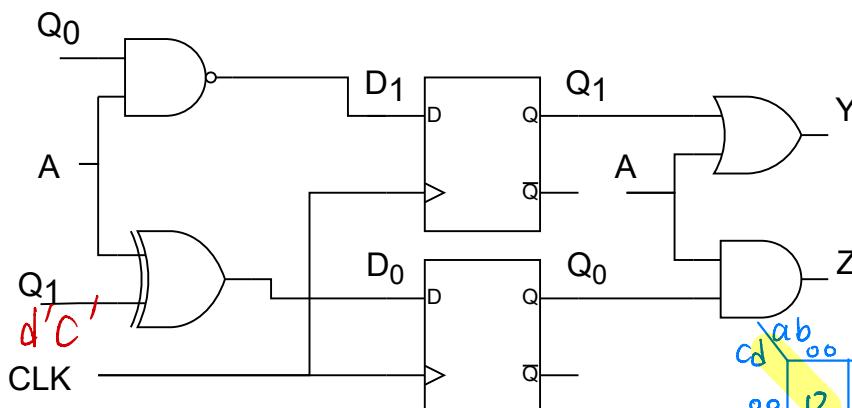
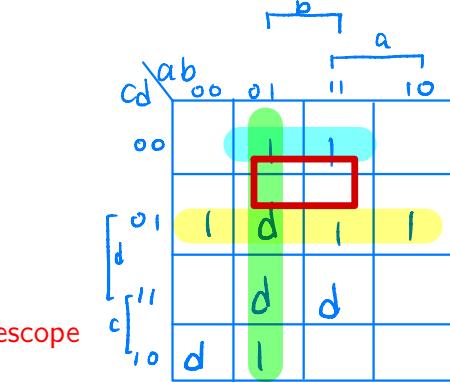


Figure 1: Sequential circuit using D flip-flops.



$$\Sigma_{a,b,c,d} (0, 3, 8, 10, 11, 14)$$

$$f = bd' + dc' + bd + dc'b$$

$$= ab + c'd + bd + bc'd'$$

$$f' = ad + bd'c'$$

$$+ bd'a'$$

$$= ad + bc'd'$$

$$+ a'b'd$$

$$f = (a+d)(b'tc+d)$$

$$(a+bt+d)$$

因为两个
2x2重叠。

$$f = b'd + ad + b'd'c'$$

$$= b'd + ad + bc'd'$$

$$f = (b+d')$$

- a. [5] Is this a Moore or a Mealy machine?

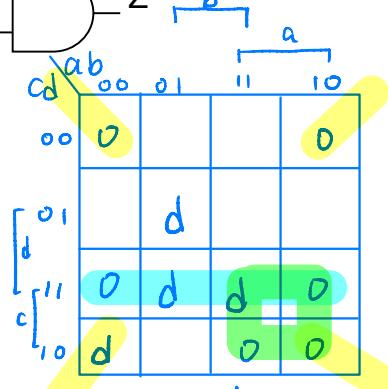
- b. [5] Find the excitation/transition equations of the two flip-flops

- c. [5] Find the output equations

- d. [5] Create the transition/output table

- e. [5] Draw the state diagram. Please label the states (00 = A, 01 = B, 10 = C, 11 = D).

- f. [5] Are there any states that are unreachable from all other states? Assume you are assured you will start on state A. Could you use this to simplify design?



$$f' = b'd' + cd + ac$$

$$f = (b+d)(c+d')$$

$$(c+d')$$

3. [25 points] *Sequential Comparator:* Design a sequential circuit to compare two unsigned n-bit numbers $X = x_{n-1}x_{n-2}\dots x_0$ and $Y = y_{n-1}y_{n-2}\dots y_0$ applied serially starting with their most significant bits. In other words, first x_{n-1} and y_{n-1} are input to the state machine, then x_{n-2} and y_{n-2} , etc, until x_0 and y_0 are used. The circuit should have two outputs z_1 and z_0 that indicate the result of the comparison. z_1 is 1 if $X < Y$. z_0 is 1 if $X > Y$. Otherwise z_1 and z_0 are 0. If the result is yet undetermined, z_1 and z_0 should also be 0.

- a. [10] Draw a state diagram using 3 states. Please include an arrow pointing to the starting state.

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2. [30 points] Sequential Circuit Analysis: Analyze the sequential circuit shown in Figure 1. Note that equations do not need to be simplified, flip-flop outputs Q_0 and Q_1 are fed back as inputs to the circuit on the left, and A also appears to the right of the flip-flops.

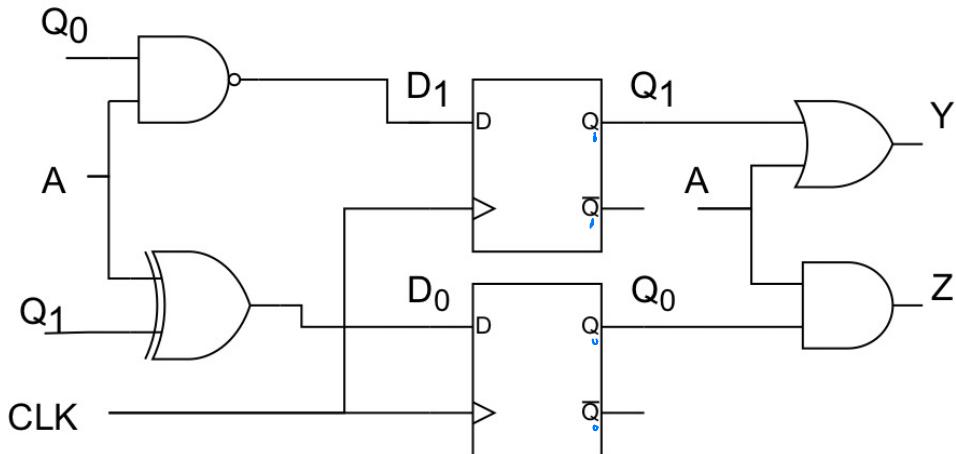


Figure 1: Sequential circuit using D flip-flops.

- a. [5] Is this a Moore or a Mealy machine? Mealy
 - b. [5] Find the excitation/transition equations of the two flip-flops
 - c. [5] Find the output equations
 - d. [5] Create the transition/output table
 - e. [5] Draw the state diagram. Please label the states ($00 = A$, $01 = B$, $10 = C$, $11 = D$).
 - f. [5] Are there any states that are unreachable from all other states? Assume you are assured you will start on state A. Could you use this to simplify design?

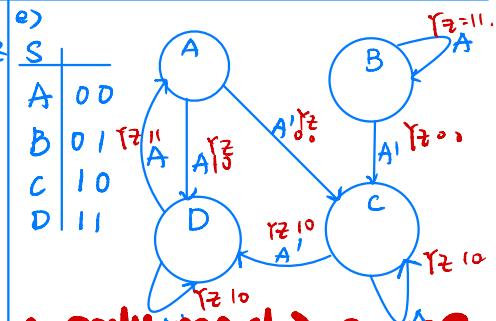
$$\Rightarrow Q_1^+ = (Q_0 A)' = Q_0' + A$$

$$Q_0^+ = A \oplus Q_1$$

$$c) Y = Q_1 + A$$

$$Z = Q_0 A$$

d) Q1 Q0		Input A		Output Y/Z/I	
Current state		0 / output	Y/Z/I	1 / output	
A	0 0	C 1 0 / 0 0	D 1 1 / 1 0		
B	0 1	C 1 0 / 0 0	D 0 1 / 1 1		
C	1 0	D 1 1 / 1 0	C 1 0 / 1 0		
D	1 1	D 1 1 / 1 0	A 0 0 / 1 1		



mealy machine use

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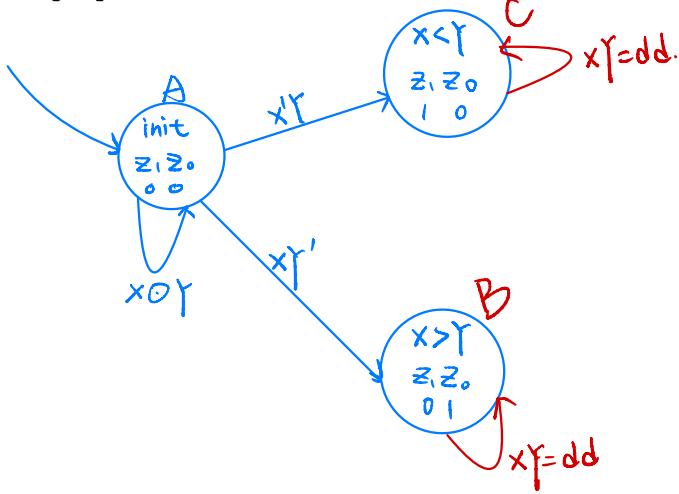
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3. [25 points] **Sequential Comparator:** Design a sequential circuit to compare two unsigned n-bit numbers $X = x_{n-1}x_{n-2}\dots x_0$ and $Y = y_{n-1}y_{n-2}\dots y_0$ applied serially starting with their most significant bits. In other words, first x_{n-1} and y_{n-1} are input to the state machine, then x_{n-2} and y_{n-2} , etc, until x_0 and y_0 are used. The circuit should have two outputs z_1 and z_0 that indicate the result of the comparison. z_1 is 1 if $X < Y$. z_0 is 1 if $X > Y$. Otherwise z_1 and z_0 is 0. If the result is yet undetermined, z_1 and z_0 should also be 0.

- a. [10] Draw a state diagram using 3 states. Please include an arrow pointing to the starting state.



- b. [10] Derive a state table.

- c. [5] Using a state assignment where the *state* = z_1z_0 , determine the next state equations.

b) current state	Input(X'Y)				output
	00	01	10	11	
A	A	C	B	A	00
B	B	B	B	B	01
C	C	C	C	C	10

state	Input(X'Y)				output
	00	01	10	11	
0 0	00	10	01	00	00
0 1	01	01	01	01	01
1 0	10	10	10	10	10

$Q_1 Q_0$ $Q_1^+ Q_0^+$

$$\left. \begin{array}{l} Q_1^+ = Q_1 + \cancel{Q_0}' X' Y' \\ Q_0^+ = Q_0 + \cancel{Q_1}' X' Y \end{array} \right\} Q_1$$

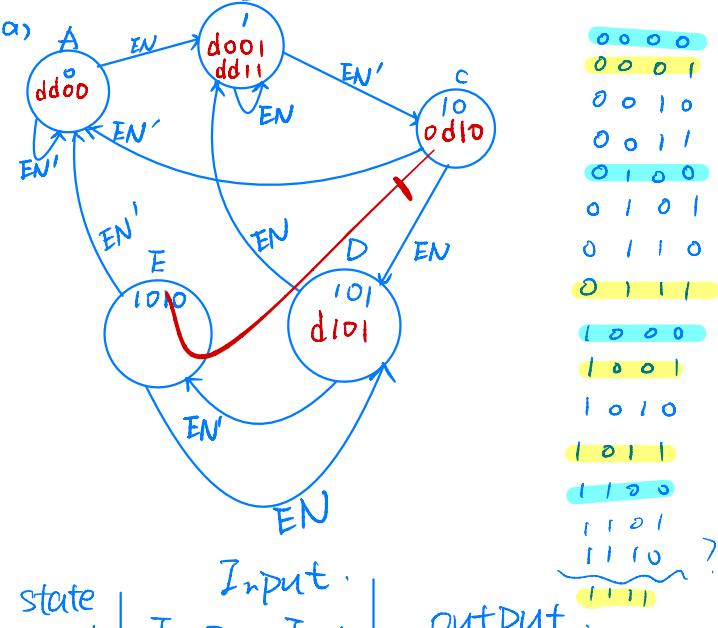
- b. [10] Derive a state table.
 c. [5] Using a state assignment where the state = $z_1 z_0$, determine the next state equations.
4. [40 points] Sequence Recognizer: Design a single-input single-output sequential circuit that recognizes the 4-bit input sequence 1010 including overlaps. For example,

	$t_0 \rightarrow t_{15}$
I	0010 1001 0101 0111
O	0000 0100 0010 1000

Table 1: Example sequence

- a. [10] What is the minimal number of states needed in this sequence recognizer? Hint: start at sequences that go from dd00 \rightarrow 1010 and dd11 \rightarrow 1010, then try to see if some states can be combined. States can be combined if they have the same transitions and output.
 b. [10] Draw a state diagram.
 c. [10] Derive the state table. Hint: use this to double check your answer for minimal states in part a. If two states have the same transitions and output they are the same.
 d. [5] Using a state assignment where the state containing with the lowest possible numerical sequence (i.e., 0000) receives 000, the state with the next lowest assignment receives a 001, etc., derive the next state equations for each state bit. You do not need to simplify.

- e. [5] Determine the output equations. You do not need to simplify.



0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111

e) output = $Q_2 Q_1 Q_0'$

no \rightarrow output = Q_2

$Q_0^+ = I$

state	input	state	input
current	$I=0$	$I=0$	$I=1$

	Input	Output
A	$I=0$	0
B	$I=1$	0
C	$I=0$	0
D	$I=1$	0
E	$I=0$	0
A	$I=1$	1

state	input	output
000	$I=0$	0
001	$I=1$	0
010	$I=0$	0
011	$I=1$	0
100	$I=0$	0
101	$I=1$?
$Q_2 Q_1 Q_0$	$Q_2^+ Q_1^+ Q_0^+$	$+ Q_2 Q_1 Q_0' I'$
2		$+ Q_2' Q_1 Q_0 I'$
		$Q_2^+ = Q_2' Q_1 Q_2 I' \quad Q_1^+ = Q_2' Q_1' Q_0 I'$