UM EECS 270 F22 Introduction to Logic Design

10. Analysis of Sequential Circuits

Sequential Circuits

- Modeled as **Finite** State Machines
- Timing behavior:
  - Synchronous (clocked)
  - Asynchronous

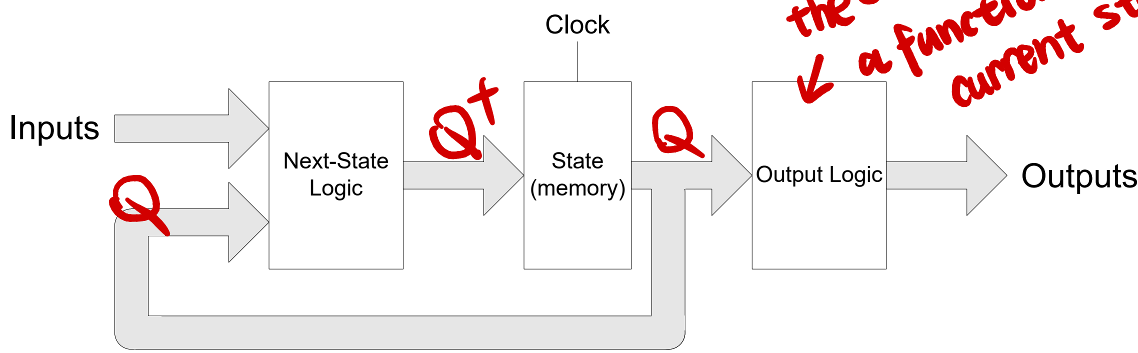
Our Focus: **Synchronous** Sequential Circuits

不考虑时间，使 functionality correct

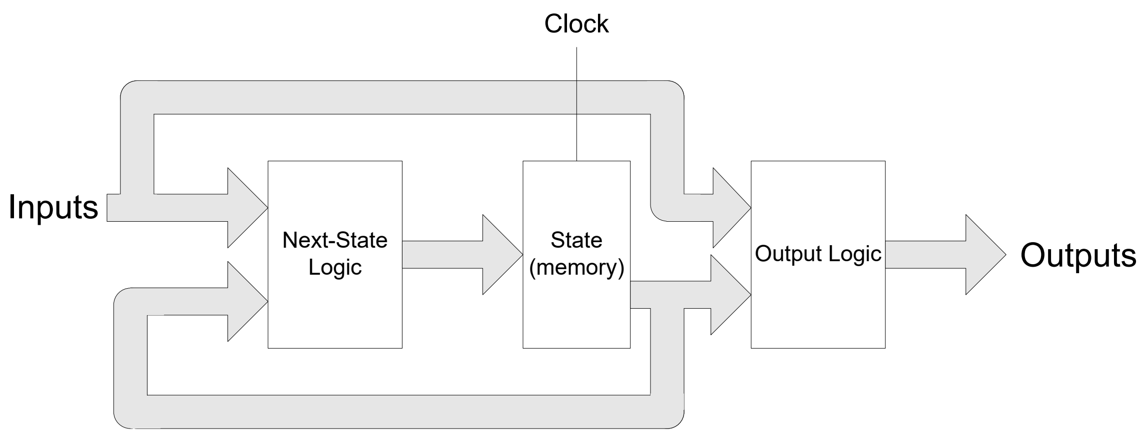
Timing: How fast is this thing

- Sequential Circuit Components:
  - **Next state logic** *(combinational)*: next state = f(current state, inputs)
  - **Memory** *(sequential)*: stores state in terms of state variables
  - **Output logic** *(combinational)*:
    - **Moore Output**: output = g(current state)

the output is only a function of the current state



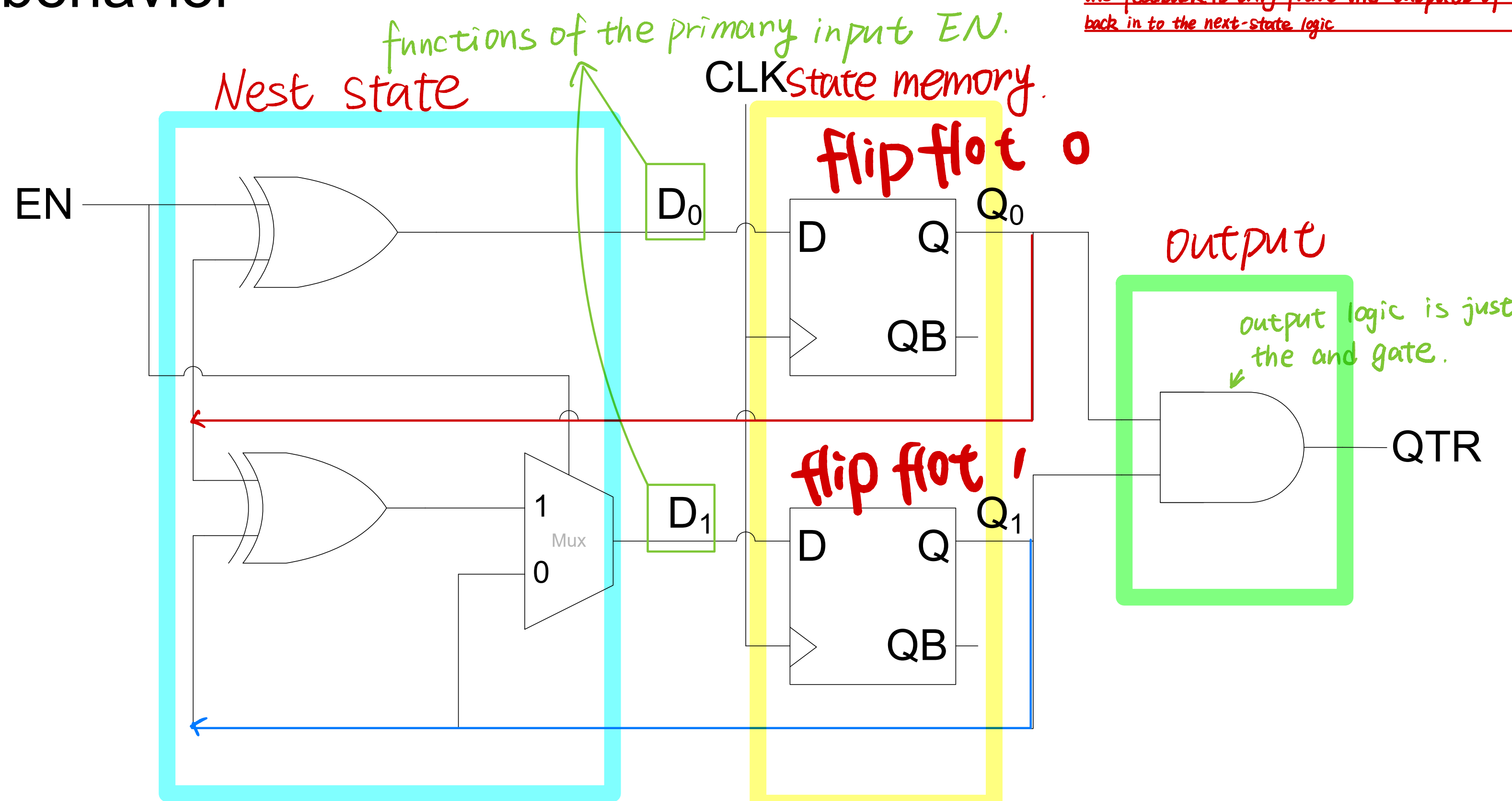
    - **Mealy Output**: output= g(current state, inputs)



Sequential Circuit Analysis

- Goal: Given a sequential circuit, describe the circuit's behavior

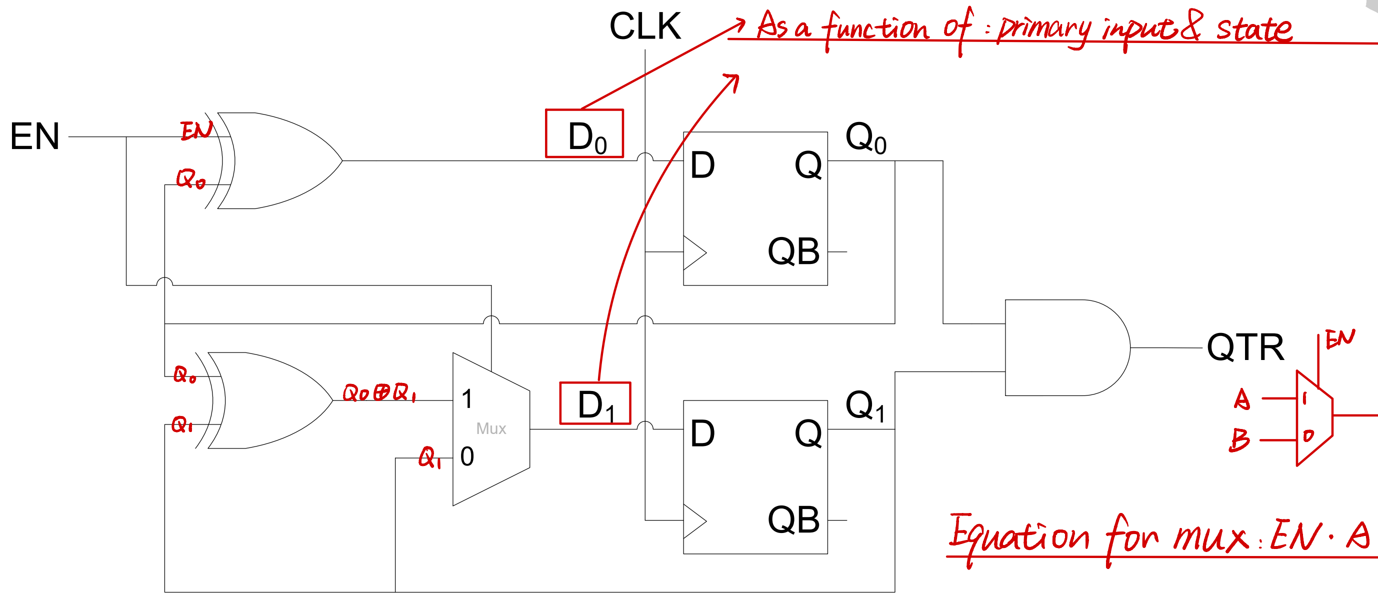
the feedback is only from the outputs of the flip flops back in to the next-state logic



- **Excitation equations** describe memory (FF or latch) input signals as a function of inputs and current state (i.e., state variables)

excitation logic equations : excite the flip flops.

As a function of : primary input & state



Equation for mux : $EN \cdot A + \overline{EN} \cdot B$

Excitation Equations: they excite the flip flop.

$$D_0 = EN \oplus Q_0$$

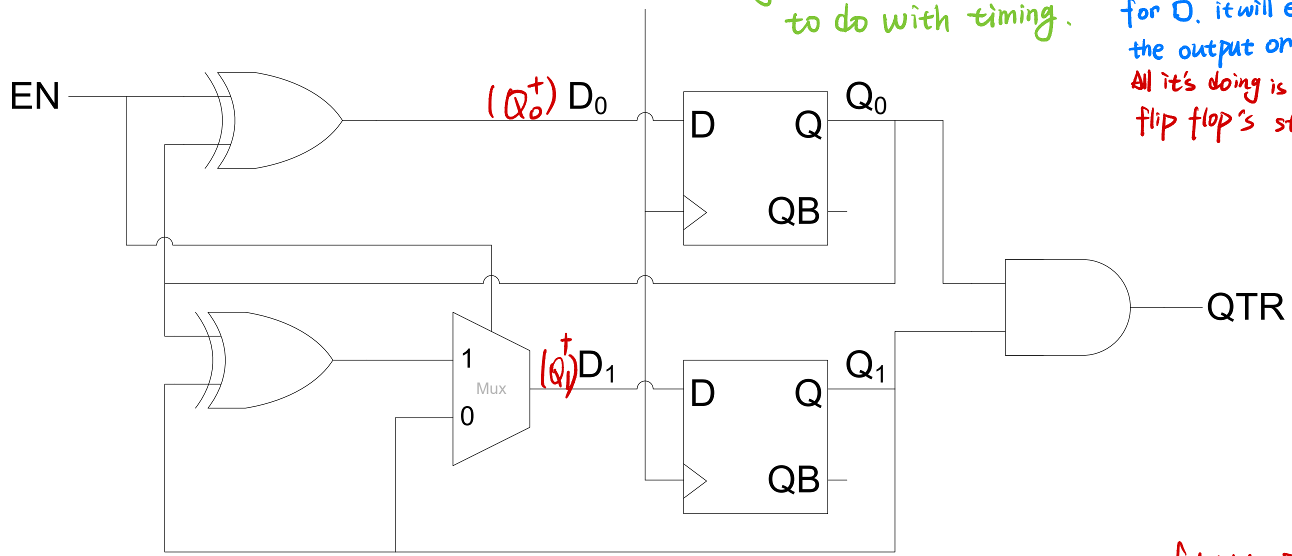
$$D_1 = EN \cdot (Q_0 \oplus Q_1) + \overline{EN} \cdot Q_1$$

- **Transition equations** describe the next state as a function of inputs and current state
  - Generated by substituting the excitation equations into the characteristic equation for the sequential gates

nothig to do with function. to do with timing.

No functional role, it just a gatekeeper for D. it will either make the D affect the output or not.

All it's doing is controlling when the flip flop's state changes.



D FF Characteristic Eqn:

特征方程.

$$Q^+ = D$$

Next state $f(IN, PS)$

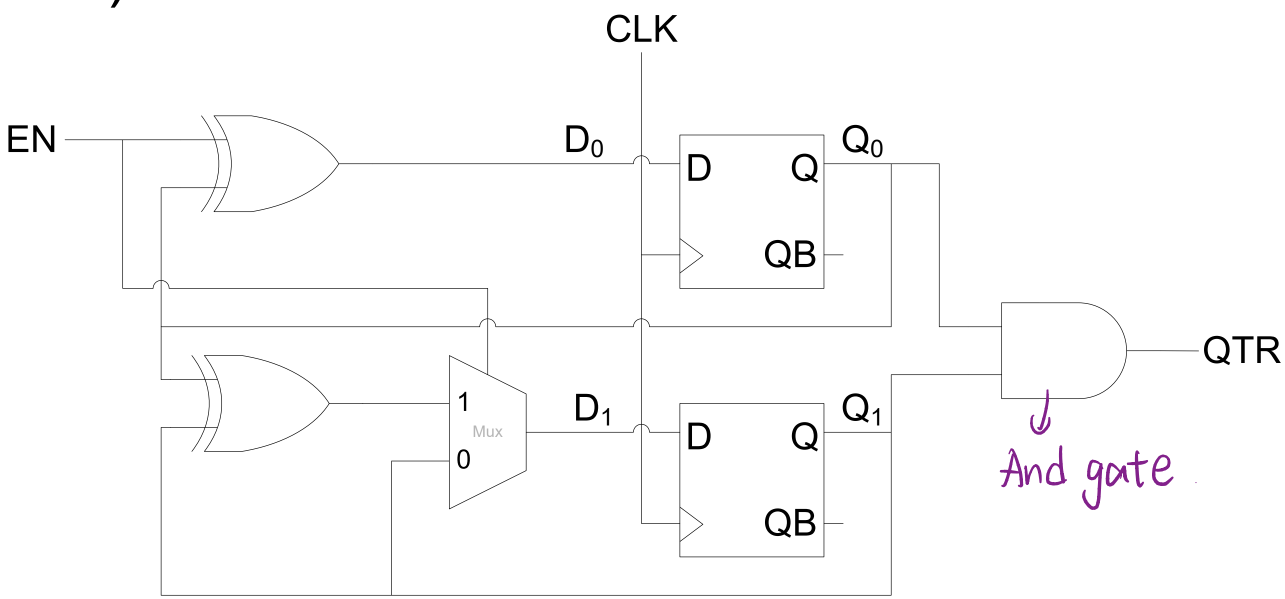
Transition Equations:

$$Q_0^+ = D_0 = EN \oplus Q_0$$

$$Q_1^+ = D_1 = EN \cdot (Q_0 \oplus Q_1) + \overline{EN} \cdot Q_1$$

This step is trivial when using D FFs!

- **Output equations** describe the output signals as a function of the current state (for a Moore machine) or as a function of the current state and inputs (for a Mealy machine)

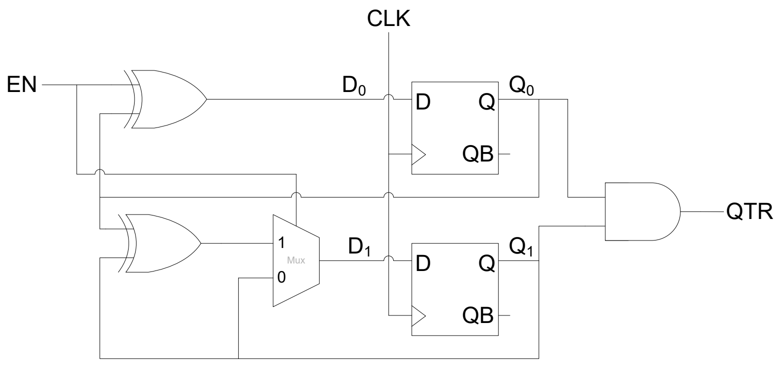


Output Equation:

$$QTR = Q_0 \cdot Q_1$$

- The **transition/output table** shows the next state and output for every current state/input combination
  - Entries of the table are obtained from the transition equations and the output equations

Transition 就是从 Q → Q⁺ 的过程，所以左侧是 current state Q.
Q^+ 取决于 input 和 Q. 由 transation equation 来描述具体的 logic combination 的逻辑. 而 output 只取决于 current state.



Transition Equations:

we have three input: EN, Q_0, Q_1

$$Q_0^+ = D_0 = EN \oplus Q_0$$

$$Q_1^+ = D_1 = EN \cdot (Q_0 \oplus Q_1) + \overline{EN} \cdot Q_1$$

Output Equation:

$$QTR = Q_0 \cdot Q_1$$

针对于一整个 sequencial circuit.
对应一个 input 和目前有的 current states. Q.
(因为 flip flop 不只一个, 所以 Q_i 也不只一个).
Q_i 会 transit 成 Q_i^+, 也就是一个组合, bits 的多少
取决于 Q 的多少, 也就是 flip flops 的多少).
↓
于是我们就通过 Q^+ 的 bits 的多少推导出有 n 种可能的 Q^+.

Transition/Output Table:

名字的由来是因为中间是 transition 的结果, 右侧是 output 的结果.

A possible current state		input EN		output
Q_1	Q_0	0	1	QTR
0	0	00	01	0
0	1	01	10	0
1	0	10	11	0
1	1	11	00	1
		$Q_1^+ Q_0^+$		
		next state		

transition function 如何运作.

- **State labels** are a one-to-one mapping from state encodings to state names

Q_1	Q_0	State name
0	0	A
0	1	B
1	0	C
1	1	D

• 给每个 state 编号 (Binary number)

• State 一共就这4个,
一会是 current state, 一会儿是 next state.

• 并且左侧的 current state Qi 也可以被集中起来表示

• 所以图表中间显现的不再是每个 flip flop 的 output 怎么变, 而是简化成 state 怎么变,

- The **state/output table** has the same format as the transition table, but state names are substituted in for state encodings

Transition/Output Table:

Q_1	Q_0	EN 0	EN 1	QTR
0	0	00	01	0
0	1	01	10	0
1	0	10	11	0
1	1	11	00	1
		$Q_1^+ Q_0^+$		

we just change from bits to labels.

State Assignments

Q_1	Q_0	State name
0	0	A
0	1	B
1	0	C
1	1	D

State value (4)

State/Output Table:

EN remain the same

S	EN 0	EN 1	QTR
A	A	B	0
B	B	C	0
C	C	D	0
D	D	A	1
	S^+		

所以 Transition/output table 和 state/output table 相比就是去掉所有单独出现的 Q_0, Q_1, Q_0^+ Q_1^+, 而是依照 current 和 Next 当Q组合成 state.

- A **state diagram** is a graphical representation of the information in the state/output table
- **Nodes** (or vertices) represent states
  - Moore machines: output values are written in state node
- **Arcs** (or edges) represent state transitions
  - Labeled with a **transition expression**
    - when an arc's transition expression evaluates to 1 for a given input combination, that arc is followed to the next state
  - Mealy machines: output values (or expressions) are written on arcs

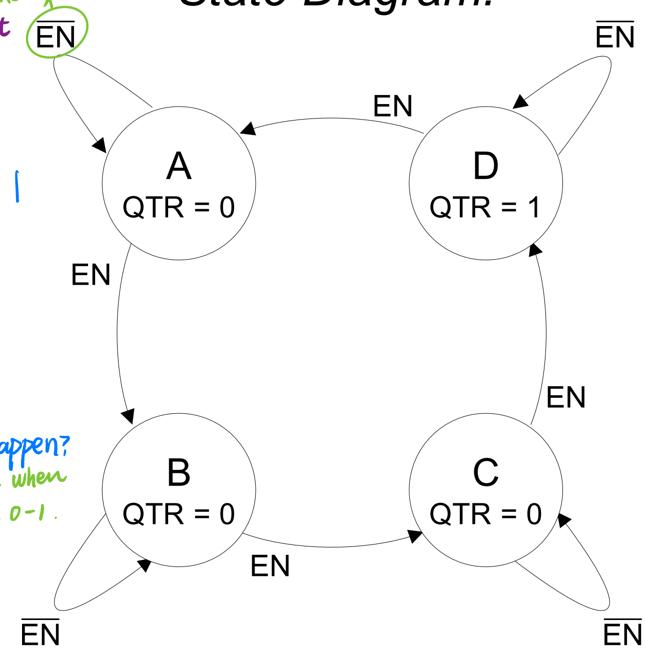
不同于 transition equation
transition expression中只包含 input，而不包含 current state Q.

State/Output Table:

	EN		
S	0	1	QTR
A	A	B	0
B	B	C	0
C	C	D	0
D	D	A	1
	S^+		

State Diagram:

means $\overline{EN}=0$



When EN = 1
A → B
B → C
C → D
D → A

· When does it happen?
· It's a timing issue, when clock transite from 0-1.

Sequential Circuit Analysis Recap

1) Find the circuit's ① **excitation equations** D = (input & current state)
2) Using the excitation and ② characteristic equations, write the circuit's ③ **transition equations** Q^+与D之间的关系.
3) Write the circuit's ④ **output equations**
4) From the transition and output equations, create the circuit's **transition/output table** ⑤
5) Create **state labels** ⑥
6) Using the transition table and state labels, create the **state table** ⑦ state/output table.
7) (optional) Draw the circuit's **state diagram**