

# EECS 373 - Homework #4

Name: \_\_\_\_\_ unique name: \_\_\_\_\_

For this assignment make a copy of this Google Doc and use the boxes provided to fill in the answers to the questions. Then submit a PDF of your completed assignment to Gradescope. Students are encouraged to fill out the assignment digitally but handwritten answers will be accepted. While minor reformatting is acceptable please do not change the layout of the questions in order to facilitate error-free grading.

## Question 1

Short answer questions: [20points, 4 each]

A) What is an interrupt vector table?

a table which the address of the interrupt routine implementation code.

B) Why should the time to execute an ISR be as short as possible? How many clock cycles does it typically take to enter an ISR?

Since when we do the ISR, the core have to switch from main mode to interrupt mode. the main program is frozen.  
ISR usually takes 12 cycles. since before implement ISR, we need to first do saving.

C) What are the hexadecimal addresses of (1) Reset\_Handler and (2) USART1\_Handler?

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## Question 1

Short answer questions: [20points, 4 each]

A) What is an interrupt vector table?

The **interrupt vector table** is a **table** of memory addresses of interrupt/exception handler routines. In other words, it defines where the code of a particular **interrupt/exception routine** is located in the microcontroller's memory.

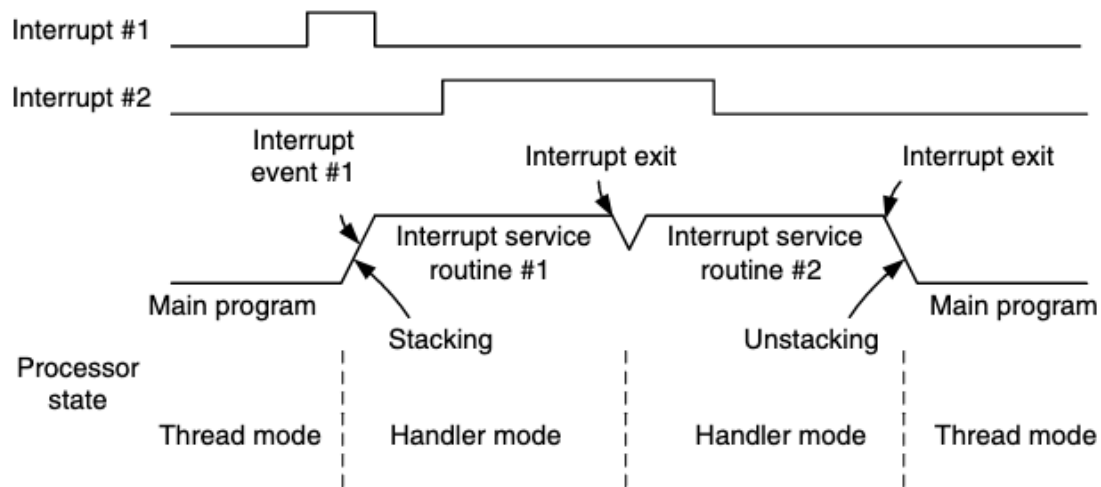
B) Why should the time to execute an ISR be as short as possible? How many clock cycles does it typically take to enter an ISR?

Interrupts allow the MCU core to react asynchronously to external events. If the time to enter the ISR is too long the MCU may not be able to respond before the next interrupt occurs. It typically takes 12 clock cycles to enter an ISR.

C) What are the hexadecimal addresses of (1) Reset\_Handler and (2) USART1\_Handler?

Reset\_Handler = 0x0000 0004  
USART1\_Handler = 0x0000 00D4

D) For the diagram below, which interrupt has the higher priority and which method is being used to improve interrupt latency. Must answer both parts to get full credit.



interrupt #1 has the higher priority ✓

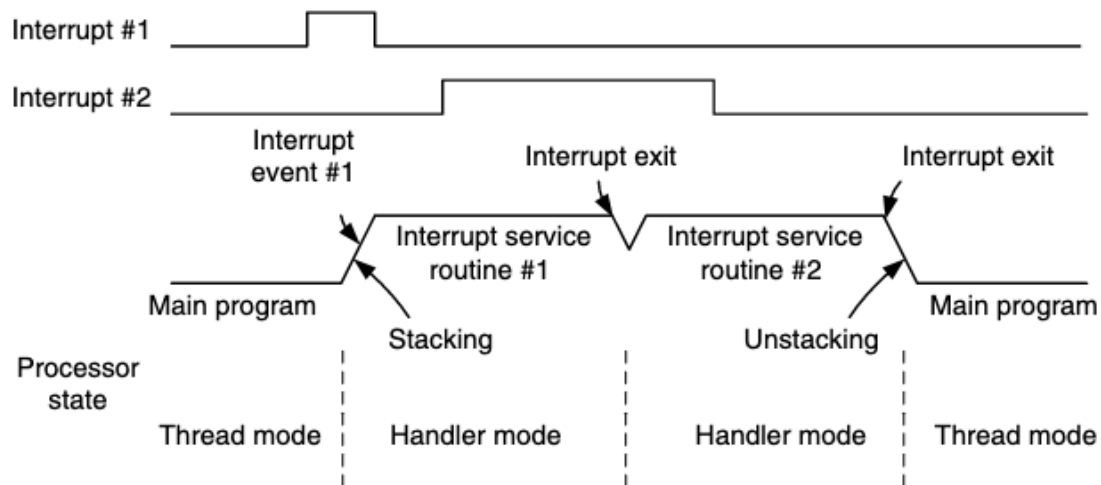
method: chain method.

Tail chaining

E) When an interrupt signal is generated, what will be done by the processor automatically before the processor starts to execute the corresponding interrupt service routine?

Stacking

D) For the diagram below, which interrupt has the higher priority and which method is being used to improve interrupt latency. Must answer both parts to get full credit.



ISR #1 has higher or equal priority to ISR #2 (meaning that ISR #1's Interrupt Priority Number is lower then or equal to the Interrupt Priority Number of ISR #2).

The method used to improve interrupt latency is called "Tail Chaining". Where pending interrupts are entered without unstacking from the previous interrupt and stacking the same information again for the pending interrupt

E) When an interrupt signal is generated, what will be done by the processor automatically before the processor starts to execute the corresponding interrupt service routine?

Push 8 registers on the stack (xPSP,PC,LR,R12,R3,R2,R1,R0)

Set LR to 0xFFFFFFFF

Set IPSR to the interrupt number

Set PC to the vector

*caller save*

## Question 2 [15 points]

You are working on a design for our STM32L4R5 which has 4 interrupt sources: A, B, C, D, and E. Recall that the STM32L4R5 only implements the 4 highest priority bits, the other 4 are ignored. You want the following to be true:

- A should be able to preempt any interrupt other than B and C.
- B should be able to preempt any interrupt.
- C should be able to preempt any interrupt other than A and B. C should have a priority higher than A.
- D should be able to preempt only E.
- E should not be able to preempt anything.

$B C > A$   
 $B > A C D$   
C should have a priority higher than A.

B ①  
 C ② ①

Table 51. Priority grouping

PRIGROUP [2:0]	Interrupt priority level value, PRI_N[7:4]			Number of	
	Binary point <sup>(1)</sup>	Group priority bits	Subpriority bits	Group priorities	Sub priorities
0b0xx	0bxxxx	[7:4]	None	16	None
0b100	0bxxx.y	[7:5]	[4]	8	2
0b101	0bxx.yy	[7:6]	[5:4]	4	4
0b110	0bx.yyy	[7]	[6:4]	2	8
0b111	0b.yyyy	None	[7:4]	None	16

1. PRI\_N[7:4] field showing the binary point. x denotes a group priority field bit, and y denotes a subpriority field bit.

A ② ②  
 D ③ ①  
 E ④ ①



### Part A

List all PRIGROUP setting or settings you could use in this case. Assume no two interrupts can be assigned the same priority. Provide your answer in 3-digit binary and explain. [5 points]

highest 2 bits are preempt priority bit.  
 second 2 highest bits are subpriority bit.

$B > [C, A] > D > E$ .

B: 0000  
 C: 0100  
 A: 0101  
 D: 1000  
 E: 1100

4 priority groups  
 2 subpriority groups

还要画图.

## Question 2 [15 points]

You are working on a design for our STM32L4R5 which has 4 interrupt sources: A, B, C, D, and E. Recall that the STM32L4R5 only implements the 4 highest priority bits, the other 4 are ignored. You want the following to be true:

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1. PRI\_n[7:4] field showing the binary point. x denotes a group priority field bit, and y denotes a subpriority field bit.

### Part A

List **all** PRIGROUP setting or settings you could use in this case. Assume no two interrupts can be assigned the same priority. **Provide your answer in 3-digit binary and explain. [5 points]**

The ranking is  $B > [C, A] > D > E$ .

Where B has the highest priority and E has the lowest priority. C and A are in the same priority group where C has a higher subpriority than A. Thus, we need 4 priority groups and 2 subpriority groups.

Given table 51 there are two options that meet the criteria: 0b100 and 0b0101

I use 0b101 prigroup [7:6] [5:4]

group priority subgroup priority

## Part B

Indicate, **in 8-bit binary**, what priorities you will assign to each interrupt. Let us know which PRIGROUP setting you are using (mainly if you have more than one PRIGROUP listed above).

Again, no two interrupts may be assigned the same priority. [5 points]

PRIGROUP= 0b101 (3-digit binary)  
A priority= 0b0101 0000 (8-digit binary)  
B priority= 0b0000 0000 (8-digit binary)  
C priority= 0b0100 0000 (8-digit binary)  
D priority= 0b1000 0000 (8-digit binary)  
E priority= 0b1100 0000 (8-digit binary)

## Part B

Indicate, ***in 8-bit binary***, what priorities you will assign to each interrupt. Let us know which PRIGROUP setting you are using (mainly if you have more than one PRIGROUP listed above). Again, no two interrupts may be assigned the same priority. **[5 points]**

PRIGROUP=\_\_\_\_\_ (3-digit binary)

A priority=\_\_\_\_\_ (8-digit binary)

B priority=\_\_\_\_\_ (8-digit binary)

C priority=\_\_\_\_\_ (8-digit binary)

D priority=\_\_\_\_\_ (8-digit binary)

E priority=\_\_\_\_\_ (8-digit binary)

*There are multiple possible answers for each PRIGROUP.*

*Xs represent don't cares to make this key as versatile as possible*

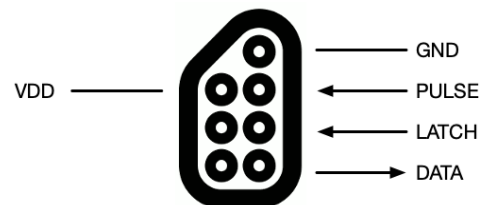
The ranking is B > [C,A] > D > E. with lowest binary priority number having the highest priority

<p>PRIGROUP = 101</p> <p>A priority = 0101, XXXX</p> <p>B priority = 0000, XXXX</p> <p>C priority = 0100, XXXX</p> <p>D priority = 1000, XXXX</p> <p>E priority = 1100, XXXX</p>	<p>PRIGROUP = 100</p> <p>A priority = 0011, XXXX</p> <p>B priority = 0000, XXXX</p> <p>C priority = 0010, XXXX</p> <p>D priority = 0100, XXXX</p> <p>E priority = 0110, XXXX</p>
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## Question 4: NES Controller Design

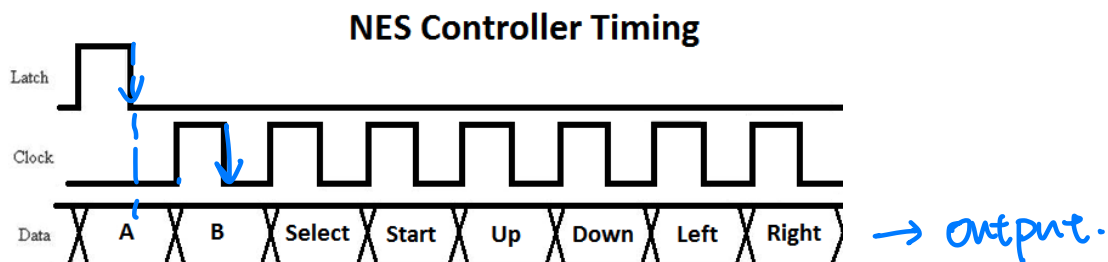
The NES (Nintendo Entertainment System) game controller is essentially a shift register that loads the state of the 8 buttons on the rising edge of the “LATCH” signal and shifts the value out serially on the “DATA” line with subsequent rising edges of “PULSE” as shown in the timing diagram below. The data is easily read by the game processor with another shift register. The data is persistent at each transition, so each button value can be latched and shifted into a shift register on each falling edge of pulse. However, the first value must be latched in using the *Latch* signal instead of the Pulse signal. For example, the **A** button can be read on the falling edge of *Latch*, the **B** button can be read on the first falling edge of Pulse, the **Select** button read on the second falling edge of pulse and so on.



### Pin Description

Pin #	Pin Name	Pin Type	Function
1	GND	Power	Ground
2	PULSE	Input	Pulse (aka Clock)
3	LATCH	Input	Rising edge causes state of the buttons to be latched into the NES game controller
4	DATA	Output	
5	NC	-	No Connect (pin not used)
6	NC	-	No Connect (pin not used)
7	+5V	Power	Power

### Timing Diagram



Your task is to design a system that will read the NES game controller using interrupts. You should read the entire problem thoroughly before starting.

Your task is to design a memory-mapped IO interface to the N8 that will capture the button values and generate a hardware interrupt signal "NES-INT" after each read is done.

- Writing to location 0x40050000 is to cause the start of a read of the NES controller. Once the read has been done an interrupt should be generated letting the core know that the value is ready to be read. The data sent with the write to this address does not matter. You may assume no read to this location will occur while in the process of doing another read.
- Reading from location 0x40050000 should return the value of the last complete transaction of the controller. This should be a 32-bit binary value where the lower 8 bits indicate the value of the buttons (A being the msb and Right being the lsb of that 8-bit value). You may assume no write will occur to this location while a read to that location is in progress.

Once that hardware has been designed, you are to write two C functions.

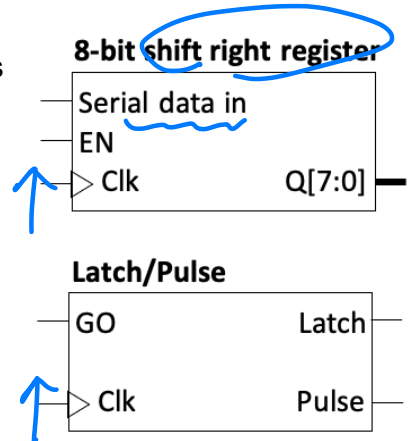
- An ISR that gets called when "NES-INT" is asserted and puts the 8-bit value read from the NES controller into a global variable called "NES\_value" and sets the global variable "NES\_ready" to 1.
- A C function that when called checks the value of NES\_ready. If that value is a 0, it is to just return a -1. If instead NES\_ready is a 1 it is to:
  - Set NES\_ready to be a 0
  - Start a new read of the NES controller.

## Part 1: NES Module [25]

Note: The logic which generates the Latch and Pulse signals is given to you (**you don't have to design it!**).

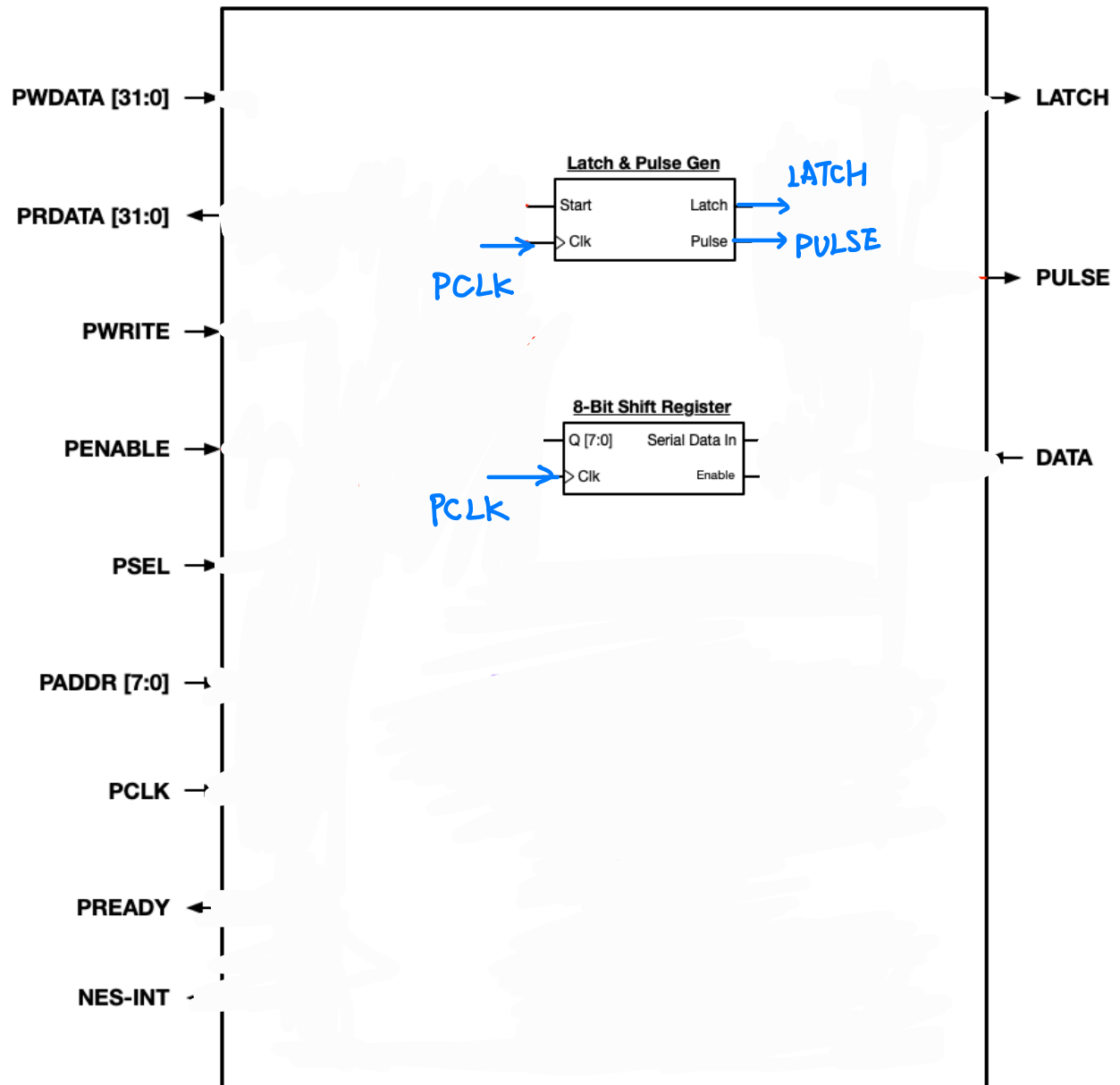
You are to design this module in schematic form. The following components are available. You may use as many of each device as you need unless otherwise indicated.

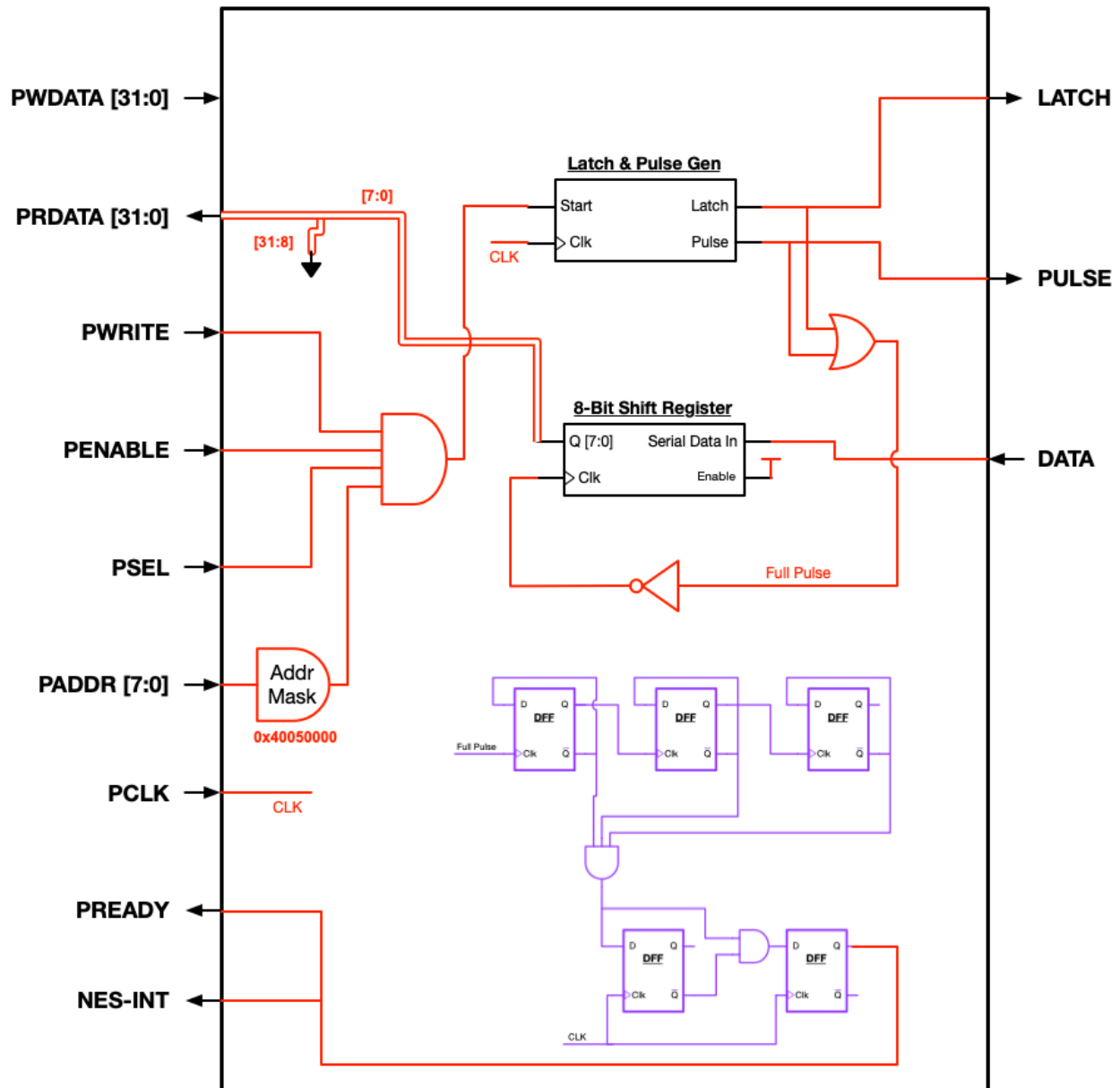
1. One serial shift register with a serial data input, an enable, and a clock input. It has an 8-bit parallel output that reflects the values in the shift register. The register shifts data to the right on every rising clock edge in which EN is 1.
2. One Latch/Pulse device. It generates Latch and Pulse as described whenever the signal GO is found to be asserted ("1") on the rising edge of its clock. It will start immediately. PCLK must be given as its clock input. This device will not function correctly if GO is asserted while the device is in the process of generating latch and pulse.
3. AND, OR, XOR and NOT gates.
4. Tri-State drivers.
5. DFFs with Enable (clock enable) and DFF connected as a registers
6. You may also use a "AND Mask" to for the PAddress to simply drawing complicated AND gates.



You may represent buses as a single wire, but indicate which signals it carries. For example, PADDR[3:0]. Further, you may show signal connections with a signal label instead of a line. For example, you can write PCLK wherever a PCLK is needed rather than drawing lines connecting all the places PCLK is needed.

Use the space on the following page to draw your schematic. All inputs are shown on the left and all outputs on the right.





The red part is the main focus of this problem. Note, we *are* using pulse as a clock, but that's okay because A) it is synced to PCLK and B) it is glitch free.

Generating NES-INT can be quite hard. You need some way to have it go high for just a clock cycle once the pulse is done. In this case I used a 3-bit counter and a "One Shot" consisting of two DFFs and an AND gate to keep NES-INT high for a one PCLK cycle, The vast majority of the points will be from the red part.

## Part 2: Interrupt Handler [10]

Write an ISR that gets called when FABINT is asserted and puts the 8-bit value read from the NES controller into a global unsigned char called “NES\_value” and sets the global int “NES\_ready” to 1.

```
__attribute__ ((interrupt)) void Fabric_IRQHandler( void ) {
```

```
__attribute__ ((interrupt)) void Fabric_IRQHandler( void ) {  
    uint8_t * NES_addr = (uint8_t *) 0x40050000;  
    NES_value = *(NES_addr);  
    NES_ready = 1;  
}
```

```
int NES_read(){  
    if (NES_ready == 0) {  
        return -1;  
    }  
    else {  
        uint8_t * NES_addr = (uint8_t *) 0x40050000;  
        NES_ready = 0;  
        *(NES_addr) = 1;  
        return NES_value;  
    }  
}
```

### Part 3: Read function [10]

Write a C function called “NES\_read” that when called checks the value of NES\_ready. If that value is a 0, it is to just return a -1. If instead NES\_ready is a 1 it is to do the following tasks:

- Set NES\_ready to be a 0
- Start a new read of the NES controller.
- Return the value last read from the NES controller.

```
int NES_read()
{
    If (NES_ready == 0) return -1;
    NES_ready = 0;
    int* addr = (int*) 0x40050000;
    *addr = 0;
    Return (int) NES_value;
}
```