EECS 270 Fall 2021

Homework 7

Due Friday, November 12 @ **5:00 PM** on Gradescope

This is an individual assignment, all of the work should be your own.
Write neatly or type and show all your work for full credit.
Have your name and unique name on the front page of your submission.

Total Points: 100

1. **[15 points]** *Setup and Hold timings:* The following tables in Table 1 show the minimum and maximum combinational delays, as well as the timing parameters of the flip-flops, in a sequential circuit with three positive edge-triggered D flip-flops clocked at 200*MHz*. All delays and timing parameters are in nanoseconds. Note that $\delta_{i,j}$ and $\Delta_{i,j}$ denotes the minimum and maximum combinational delays from the output of flip-flop i to the input of flip-flop j, respectively.

Minimum Delays

$\delta_{i,j}$	D_0	D_1	D_2
Q_0	3	∞	3
Q_1	1	6	4
Q_2	∞	4	2

Maximum Delays

$\Delta_{i,j}$	D_0	D_1	D_2
Q_0	5	$-\infty$	5
Q_1	2	9	6
Q_2	$-\infty$	5	3

Clock to Q delay	$t_P^{C\longrightarrow Q} = 3$
Setup time	$S = 1$
Hold time	$H = 5$

Table 1: Timing specifications for sequential circuit.

	Min	Max
D_0	1+3=4	5+3=8
D_1	4+3=7	9+3=12
D_2	2+3=5	6+3=9

#12 P=10ns.

a. **[6]** Compute the early and late arrival times for each of the three flip-flops.

b. **[6]** Determine if there are any setup or hold violations with respect to the clock (200 MHz).
Hold Violation at FF_0: True/False
Hold Violation at FF_1: True/False
Hold Violation at FF_2: True/False
Setup Violation at FF_0: True/False
Setup Violation at FF_1: True/False
Setup Violation at FF_2: True/False

$a_0 = 4$ $A_0 = 8$
$a_1 = 7$ $A_1 = 12$
$a_2 = 5$ $A_2 = 9$

hold time = 5 $P = \frac{1}{f} = \frac{1}{200\times10^6 Hz} = 0.5\times10^{-6}s = 5ns$,

c. **[3]** If there are setup or hold violations that prevent the circuit from operating at 200 MHz, what is the maximum frequency (in MHz) that allows the circuit to function without timing errors? If simply changing the frequency does not fix all timing errors, what other actions must be taken?

12+1=13ns.

$f = \frac{1}{13ns} = \frac{1}{13\times10^{-9}} = 0.077\times10^9 Hz = 77MHz.$

However we can't use this frequency to solve the FF0 Hold violation. We can lower the hold time by 1ns or add an additional delay during the path.

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1. **[15 points]** *Setup and Hold timings:* The following tables in Table 1 show the minimum and maximum combinational delays, as well as the timing parameters of the flip-flops, in a sequential circuit with three positive edge-triggered D flip-flops clocked at $200MHz$. All delays and timing parameters are in nanoseconds. Note that $\delta_{i,j}$ and $\Delta_{i,j}$ denotes the minimum and maximum combinational delays from the output of flip-flop i to the input of flip-flop j, respectively.

Minimum Delays

$\delta_{i,j}$	D_0	D_1	D_2
Q_0	3	∞	3
Q_1	1	6	4
Q_2	∞	4	2

Maximum Delays

$\Delta_{i,j}$	D_0	D_1	D_2
Q_0	5	$-\infty$	5
Q_1	2	9	6
Q_2	$-\infty$	5	3

Clock to Q delay	$t_P^{C\longrightarrow Q} = 3$
Setup time	$S = 1$
Hold time	$H = 5$

Table 1: Timing specifications for sequential circuit.

   a. **[6]** Compute the early and late arrival times for each of the three flip-flops.

   b. **[6]** Determine if there are any setup or hold violations with respect to the clock (200 MHz).
   Hold Violation at FF_0: True/False
   Hold Violation at FF_1: True/False
   Hold Violation at FF_2: True/False
   Setup Violation at FF_0: True/False
   Setup Violation at FF_1: True/False
   Setup Violation at FF_2: True/False

   c. **[3]** If there are setup or hold violations that prevent the circuit from operating at 200 MHz, what is the maximum frequency (in MHz) that allows the circuit to function without timing errors? If simply changing the frequency does not fix all timing errors, what other actions must be taken?

2. **[35 points]** *Sequential Circuit Timing Analysis 1:* Assume the timing parameters in Table 2 for timing analysis of the circuit in Figure 1.

Gate Timings
t_p^{NOT}=1 ns
t_p^{NAND}=2 ns
t_p^{OR}=4 ns

Flip-flop timings
$t_p^{C\longrightarrow Q} = 5$ ns (Clock-to-Q delay)
$S_{0,1} = 4$ ns (Setup time for $DFF_{0,1}$)
$S_2 = 5$ ns (Setup time for DFF_2)
$H = 2$ ns (Hold time for all three DFFs)

Table 2: Timings for problem 2

   a. **[6]** Determine the early (d_0, d_1, d_2) and late (D_0, D_1, D_2) signal departure times from the three flip-flops.

2. **[35 points]** *Sequential Circuit Timing Analysis 1:* Assume the timing parameters in Table 2 for timing analysis of the circuit in Figure 1.

Gate Timings	Flip-flop timings
t_p^{NOT}=1 ns	$t_c^{C\to Q}$ = 5 ns (Clock-to-Q delay)
t_p^{NAND}=2 ns	$S_{0,1}$ = 4 ns (Setup time for $DFF_{0,1}$)
t_p^{OR}=4 ns	S_2 = 5 ns (Setup time for DFF_2)
	H = 2 ns (Hold time for all three DFFs)

Table 2: Timings for problem 2

a. **[6]** Determine the early (d_0, d_1, d_2) and late (D_0, D_1, D_2) signal departure times from the three flip-flops.

min	D_0	D_1	D_2
Q_0	4	3	4
Q_1	4	2	4
Q_2	8	∞	5

max	D_0	D_1	D_2
Q_0	8	3	4
Q_1	4	2	4
Q_2	8	$-\infty$	5

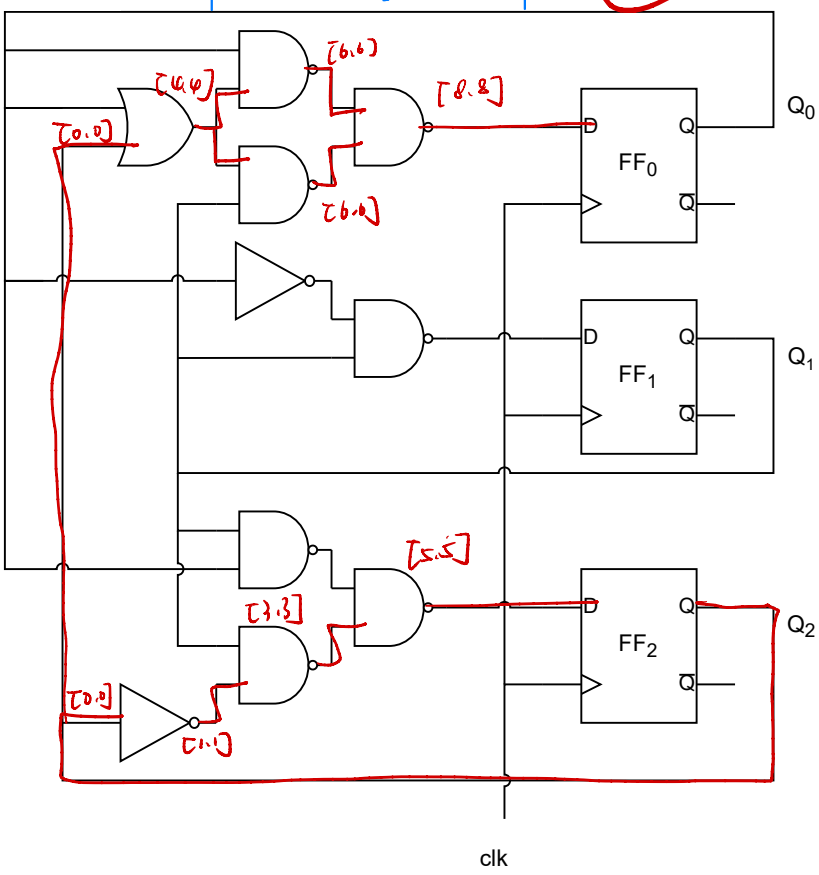

Figure 1: Circuit for problem 2

b. **[18]** Determine the matrix of minimum and maximum combinational propagation delays from the flip-flop outputs to flip-flop inputs. Use $\delta_{i,j}$ and $\Delta_{i,j}$ to denote the minimum and maximum combinational delays from the output of flip-flop i to the input of flip-flop j, respectively. Remember to use the appropriate values for when a signal is not connected to the other: ∞ for minimum delays and $-\infty$ for maximum delays.

$a_0 = 4+5 = 9$ | $A_0 = 8+5 = 13$
$a_1 = 2+5 = 7$ | $A_1 = 3+5 = 8$
$a_2 = 4+5 = 9$ | $A_2 = 5+5 = 10$

Minimum Delays

$\delta_{i,j}$	D_0	D_1	D_2
Q_0			
Q_1			
Q_2			

Maximum Delays

$\Delta_{i,j}$	D_0	D_1	D_2
Q_0			
Q_1			
Q_2			

c. **[6]** early and late signal arrival times to each of the flip-flops.

d. **[5]** The minimum clock period P_{min} that allows the circuit to operate without violating the setup and hold requirements. In addition, use P_{min} to derive the maximum clock frequency f_{CLK} for this circuit.

$P_{0\,min} = 13+4 = 17$ max 17

$P_{1\,min} = 8+4 = 12$

$P_{2\,min} = 10+5 = 15$

$1/17\,ns = \frac{1}{17 \times 10^{-9}}\,s$

$= 58.8\,MHz$

3. **[25 points]** *Sequential Circuit Timing Analysis 2:* The schematic diagram shown in Figure 2 displays the timing data for a sequential circuit with three edge-triggered D flip-flops. Table 3 has additional information. Each flip flop has black-box transition logic, each as a function of Q_2, Q_1, Q_0. On each block are the minimum and maximum path delays for each input in nanoseconds listed as [$delay_{min}$, $delay_{max}$]. For example the min and max path delays from from Q_1 to D_2 are 3 and 5 ns, respectively.

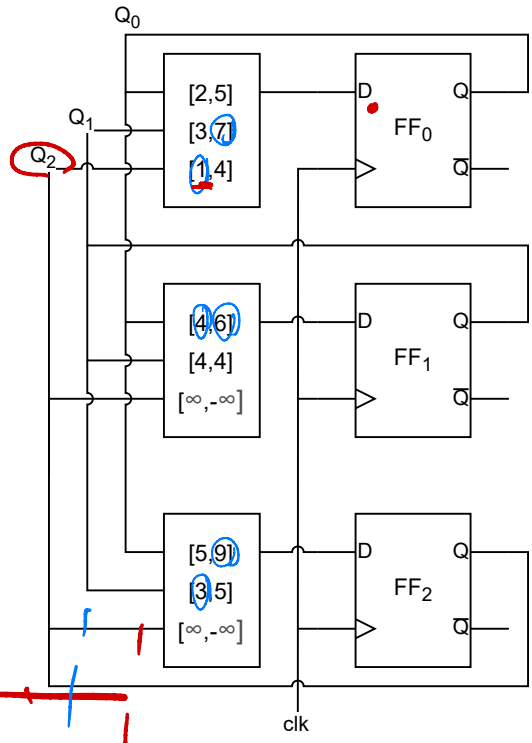

Figure 2: Circuit for problem 3

FF timing parameters:
$t_p^{C\rightarrow Q}$ = [1,3] ns (Clock-to-Q delay)
S = 4 ns (Setup Time)
H = 4 ns (Hold Time)

Table 3: Flip-flop timing parameters for problem 3.

a. **[6]** Compute the early (a_i) and late (A_i) arrival times for the three flip-flops: a_0, a_1, a_2, A_0, A_1, A_2.

b. **[4]** What should the minimum clock period P be to avoid setup violations?

c. **[5]** Is there a hold violation at FF_0? If Yes, which path delay(s) should be increased, and by how much, in order to eliminate the violation without increasing P?

d. **[5]** Is there a hold violation at FF_1? If Yes, which path delay(s) should be increased, and by how much, in order to eliminate the violation without increasing P?

e. **[5]** Suppose that CLK_0 and CLK_1 have [-1, +1] ns uncertainty in their periods. In this case, what should the minimum clock period P be to avoid setup violations?

4. **[25 points]** *Johnson Counter Decoder:* The modulus of a 4-bit binary counter is 16. When used in a polling application it requires a 4-to-16 decoder consisting of 16 4-bit AND gates. A 4-bit shift register ring counter eliminates the need for the decoder but its modulus is only 4. A 4-bit Johnson counter represents a compromise between these two "extremes". Its modulus is 8 and its decoder can be implemented using 8 2-input AND gates.

   Figure 3 shows the schematic of a 4-bit Johnson Counter followed by a "box" representing its decoder logic. The inputs of the decoder are the 4 bits of the Johnson counter Y_3, Y_2, Y_1, Y_0 and its outputs are the decoded signals labeled Z_i where i corresponds to the 4-bit combination of the Y signals. For example, Z_7 corresponds the the count $Y_3Y_2Y_1Y_0 = 0111$.

   Find the logic expression of each of the 8 Z signals as a function of the Y signals.

   Hint: Consider don't-cares on 4-variable K-Maps!

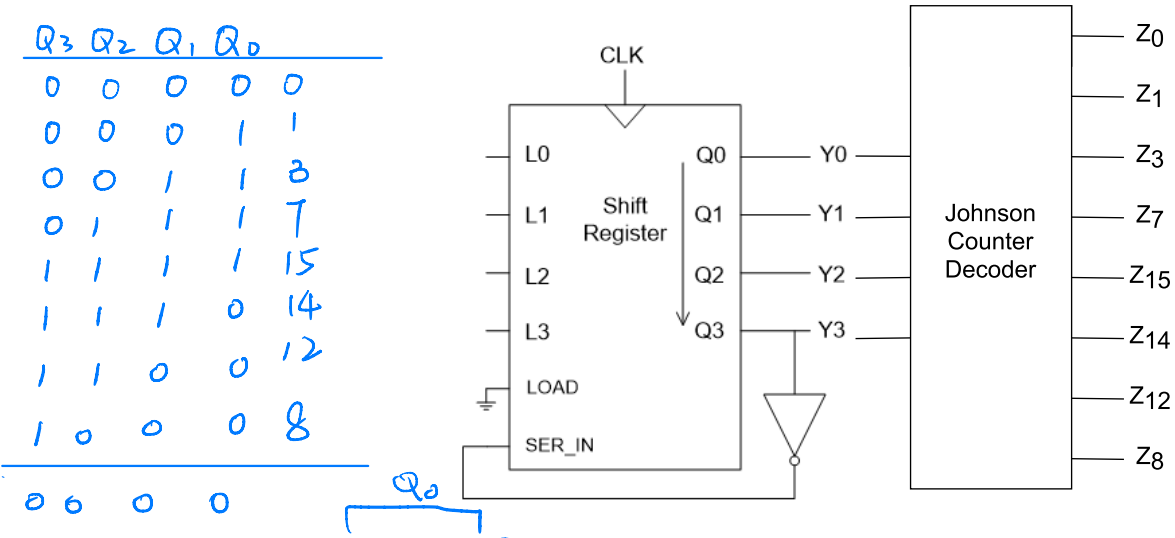

Figure 3: Decoding 4-bit Johnson Counter

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	✓ 0	✓ 1	✓ 3	d 2
01	d 4	d 5	✓ 7	d 6
11	✓ 12	d 13	✓ 15	✓ 14
10	✓ 8	d 9	d 11	d 10

$f_{Z0} = Q_3' Q_0'$

$f_{Z1} = Q_0 Q_1'$

$f_{Z3} = Q_2' Q_1$

$f_{Z7} = Q_2 Q_3'$

$f_{Z15} = Q_3 Q_0$

$f_{Z14} = Q_1 Q_0'$

$f_{Z12} = Q_1' Q_2$

$f_{Z8} = Q_3 Q_2'$