

EECS 373 Midterm 2

Fall 2017

6 November 2017

Calculators without network connection are allowed. No external reference material is allowed.

Pledge: I have neither given nor received aid on this exam nor observed anyone else doing so.

Signature:

Name:

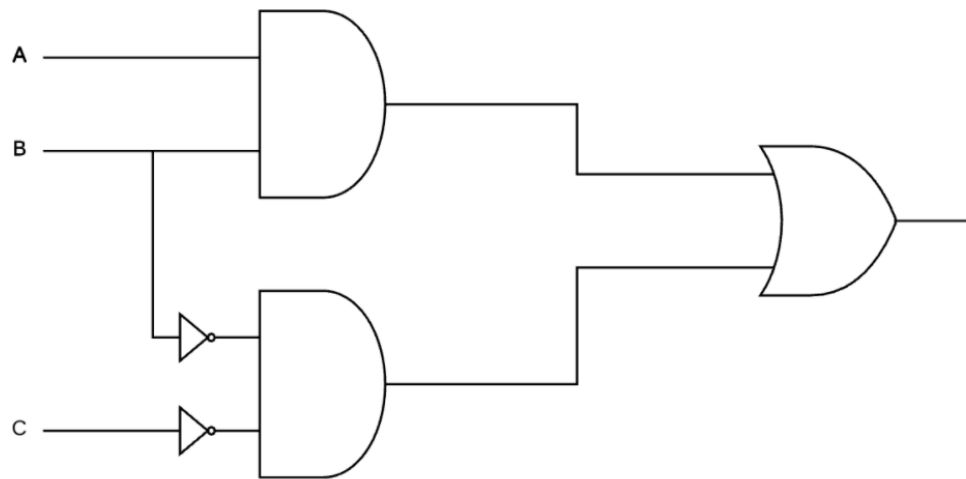
Unique name:

1. (8 pts.) Digital Design

Consider the two-level logic circuit below. Determine if the circuit contains a hazard and if so, update the circuit diagram to remove the hazard without changing the function. You are allowed to use and/or/not gates to do so but the circuit must remain two-level (inverters do not count as a level). If there is no hazard, briefly explain why.

Hazard? **Yes** **No**

If not, why?



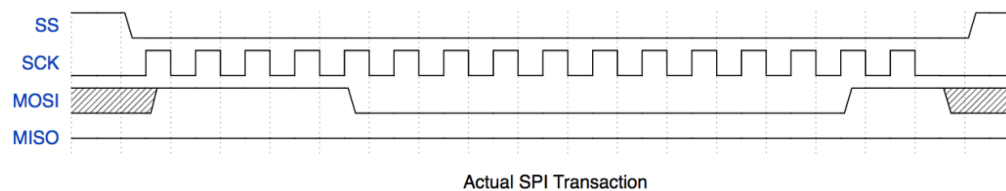
2. (10 pts.) Serial Buses

- (a) (5 pts.) You are interfacing with a LIDAR module using SPI. You attempt to put the module into sleep mode, but the module does not respond as expected. You have gathered the following information.

From the datasheet:

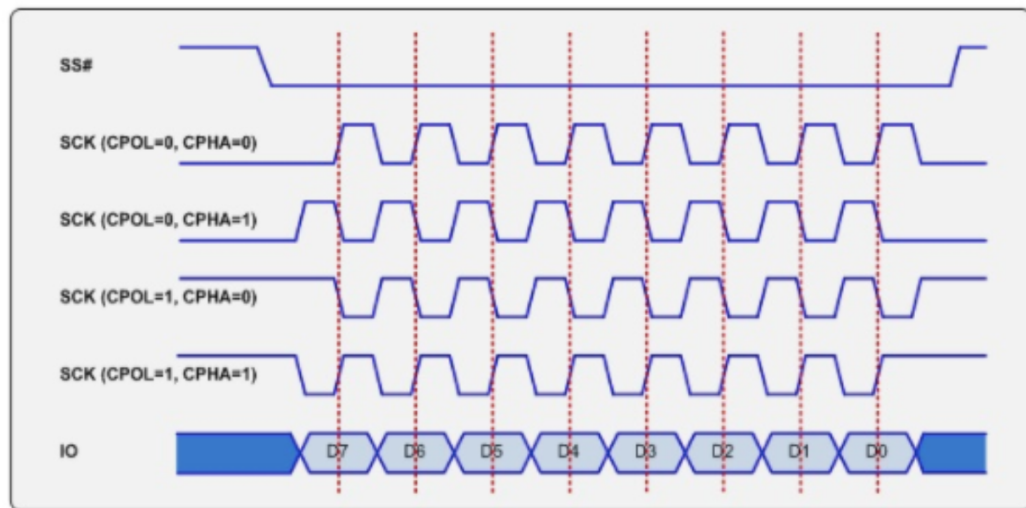
- The module uses SPI mode 0 (CPOL = 0, CPHA = 0)
- The module can be put into sleep mode by writing instruction byte 0xF0 followed by the data byte 0x03
- The module uses a SPI frame size of 1 instruction byte and 1 data byte

From a logic analyzer:



Using this information, what is the cause of this problem? A timing diagram is provided below.

SPI Timing Diagram:



- (b) **(5 pts.)** You are interfacing with two identical 12-bit DACs using SPI on a SmartFusion. Each DAC accepts levels between 0x000 and 0xFFF and output the corresponding voltage on one of 8 channels. The DAC uses SPI mode 0 (CPOL = 0, CPHA = 0). The 16-bit SPI frame is shown below. OutEnable is active high, Chan2-0 form a three bit number denoting channels 0-7.

Byte 1 (MSB on left)

OutEnable	Chan2	Chan1	Chan0	Data11	Data10	Data9	Data8
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Byte 2

Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0
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- i. **(3 pts.)** Fill in the blanks to make each DAC output the maximum value on channel 0. Assume that all GPIO pins are configured. See excerpts from the MSS SPI header file on the following page.

```
#include <stdio.h>
#include <inttypes.h>
#include "drivers/mss_spi/mss_spi.h"

int main(void) {
    const uint8_t frame_size = ____; // TODO: SPI FRAME SIZE IN BITS
    const uint8_t DAC0_frame[] = _____; // TODO: DAC 0 FRAME
    const uint8_t DAC1_frame[] = _____; // TODO: DAC 1 FRAME

    MSS_SPI_init( &g_mss_spi1 );

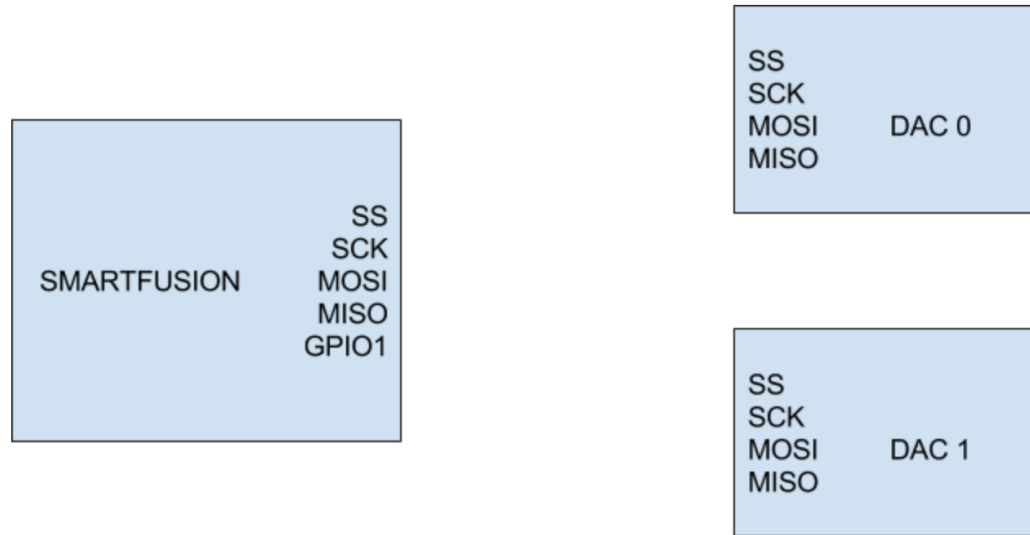
    MSS_SPI_configure_master_mode
    (
        &g_mss_spi1,
        MSS_SPI_SLAVE_0,
        _____, //TODO: SPI MODE (ex. MSS_SPI_MODE3)
        MSS_SPI_PCLK_DIV_256,
        frame_size
    );

    // WRITE TO DAC 0
    MSS_SPI_set_slave_select( &g_mss_spi1, MSS_SPI_SLAVE_0 );
    MSS_SPI_transfer_frame( &g_mss_spi1, DAC0_frame );
    MSS_SPI_clear_slave_select( &g_mss_spi1, MSS_SPI_SLAVE_0 );

    // WRITE TO DAC 1
    _____; // TODO: Slave Select
    MSS_SPI_transfer_frame( &g_mss_spi1, DAC1_frame );
    _____; // TODO: Slave Select

    return(0);
}
```

- ii. (2 pts.) Fill in the schematic below by connecting all inputs and outputs.



MSS SPI Header – Function Declarations:

```

/*
The MSS_GPIO_set_output() function sets the state of a single GPIO Port
Example Usage:
MSS_GPIO_set_output(MSS_GPIO_0, 1);
*/
void MSS_GPIO_set_output
(
    mss_gpio_id_t      port_id,
    uint8_t            value
);
/*
The MSS_SPI_configure_master_mode() function configures the SPI bus master

Example Usage:
MSS_SPI_configure_master_mode
(
    &g_mss_spi0,
    MSS_SPI_SLAVE_0,
    MSS_SPI_MODE3,
    MSS_SPI_PCLK_DIV_256,
    MSS_SPI_BLOCK_TRANSFER_FRAME_SIZE
);
*/
void MSS_SPI_configure_master_mode
(
    mss_spi_instance_t * this_spi,
    mss_spi_slave_t      slave,
    mss_spi_protocol_mode_t protocol_mode,
    mss_spi_pclk_div_t    clk_rate,
    uint8_t               frame_bit_length
);

```

3. **(12 pts.)** Timers

Consider the following tasks that a development board must handle:

- An accelerometer that must be read from every 4 seconds,
- a motor driven by a PWM with 50% duty cycle running at 100 Hz,
- SPI data lines that must be sampled at 50 kHz, and
- an LED that must be toggled at 1 MHz.

There are two 32-bit hardware timers, both clocked at 80 MHz.

Describe how to set the overflow and/or compare values of the hardware and virtual timers to accomplish these tasks. Describe what event(s) must happen when a timer overflows or hits its compare register. You do not need to elaborate on how to accomplish the tasks, just when they should be accomplished.

(3 pts.) Hardware Timer #1:

(3 pts.) Hardware Timer #2:

(6 pts.) Virtual Timer(s): You may not need to use all the timers. If you do not use one or more, please write n.a. in the space provided.

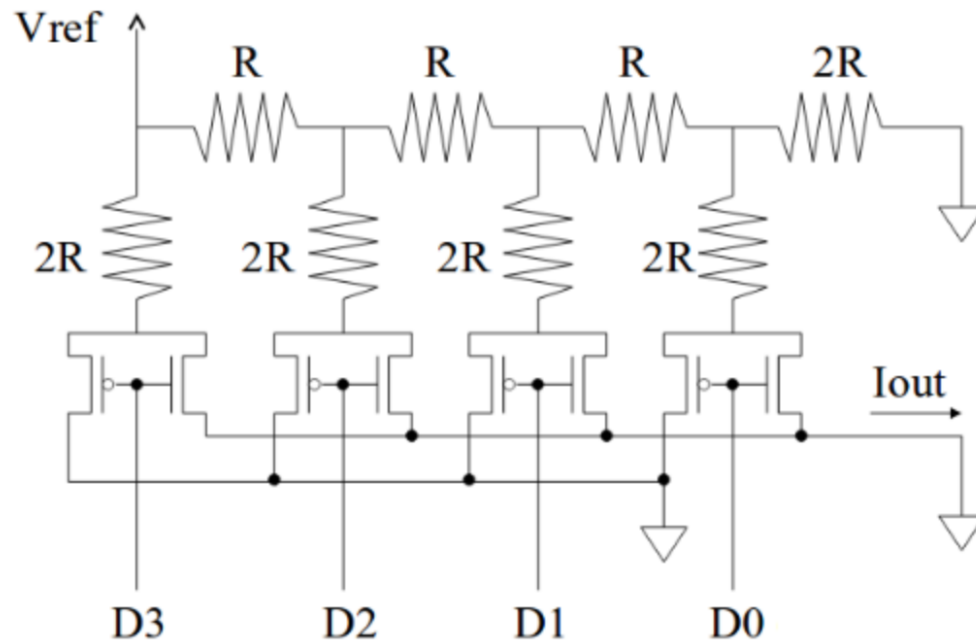
Virtual Timer #1:

Virtual Timer #2:

Virtual Timer #3:

4. (8 pts.) ADCs and DACs

Consider the schematic below. For this problem assume $V_{ref} = 8\text{ V}$ and $R = 500\ \Omega$. D3 is the MSB of the DAC and D0 is the LSB.



(a) (5 pts.) What is I_{out} if you input 0b0101 into the above DAC? Show all work.

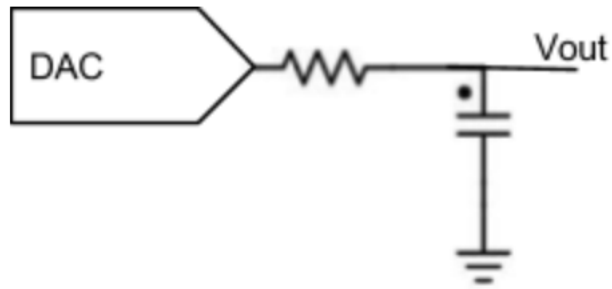
(b) (3 pts.) In fewer than 3 sentences, explain the advantages and disadvantages of using an R/2R Ladder as shown above versus a voltage divider?

5. (12 pts.) Analog Circuits

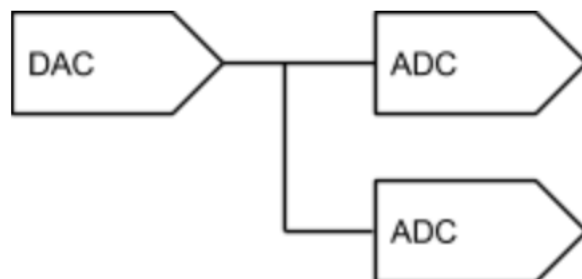
- (a) (4 pts.) You add a low pass filter to a DAC output and discover that its 3 dB down point is reduced from 500 Hz to 100 Hz. You reason that the source resistance for the DAC is affecting your filter. What is the DAC's source resistance if the filter component values are $R = 1\text{ k}\Omega$ and $C = 1/\pi\text{ }\mu\text{F}$? Show your work.

$$1\text{ }\mu\text{F} = 10^{-6}\text{ F.}$$

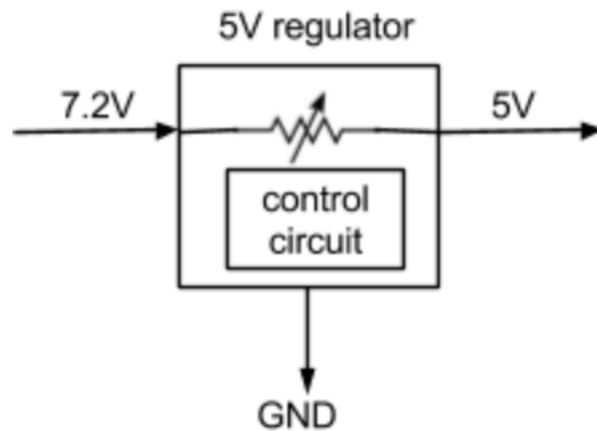
The 3 dB down point for a low pass filter is given by $2\pi f = 1/RC$.



- (b) (4 pts.) You want to test two ADCs with a DAC. When you connect them, you notice at full scale your DAC output is only 1/2 of full scale. If the source resistance of the DAC is $10\text{ k}\Omega$, what are the input resistances of the ADCs assuming they are the same value? Show your work.



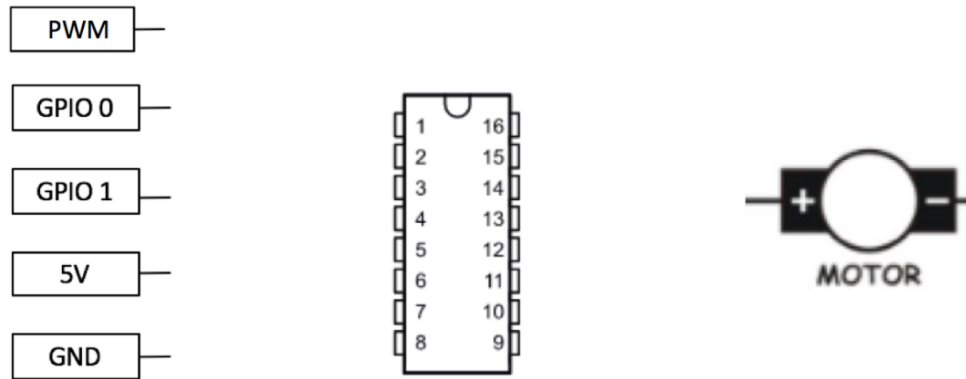
- (c) (4 pts.) You need 5 V for your project, but the battery you are using is 7.2 V. The lab instructor gives you a linear 5 V regulator. A linear regulator can be approximately modeled as a variable resistor that varies to adjust the output voltage. Assuming that your circuit draws about 200 mA, how much power does the regulator have to dissipate? Show your work.



6. (8 pts.) Motors and H-bridges

You are tasked with hooking up a motor to your embedded system. Below we have abstracted your system to be 5 SmartFusion pins, the SN754410 H-Bridge (see documentation below), and a motor.

Draw wires to connect your system so that the GPIO pins can drive the motor forward or backward, depending on GPIO outputs (you don't need to specify GPIO outputs). Note that this H-bridge is capable of driving two motors, but you are only instructed to drive one. Ground any inputs you are not using to drive the motor shown. The PWM pin is for controlling the speed of the motor. The documentation below should provide all of the necessary information you need to solve this problem. State your assumptions on pin-channel association.



PIN		TYPE	DESCRIPTION
NAME	NO.		
1,2EN	1	I	Enable driver channels 1 and 2 (active high input)
<1:4>A	2, 7, 10, 15	I	Driver inputs, non-inverting
<1:4>Y	3, 6, 11, 14	O	Driver outputs
GROUND	4, 5, 12, 13	—	Device ground and heat sink pin. Connect to circuit board ground plane with multiple solid vias
V _{CC2}	8	—	Power VCC for drivers 4.5V to 36V
3,4EN	9	I	Enable driver channels 3 and 4 (active high input)
V _{CC1}	16	—	5V supply for internal logic translation

The pinout above is for an SN754410 H-Bridge. Descriptions for the pins are given in the table. Setting GPIO 0 high, and GPIO 1 low should turn the motor forward. Setting GPIO 0 low, and GPIO 1 high should turn the motor in reverse.

7. **(12 pts.)** Wireless sensor network battery lifespan.

Consider a wireless sensor network containing 20 battery-powered nodes distributed over several acres of land. They sense ground vibration events.

These nodes spend most of their time in low-power sleep modes, in which the processor has 1 mW power consumption and the radio has 0 mW power consumption. When a ground vibration event occurs, a node leaves sleep mode, with the processor transitioning to an active state in which it has 100 mW power consumption. The processor (with built-in ADC and accelerometer) measures vibration until the vibration event ends and all of the data have been transmitted to a base station, then re-enters sleep mode. The 16-bit built-in ADC samples at 100 kHz. The wireless interface has 200 mW power consumption when transmitting and transmits data at a rate of 10,000 b/s. The system can sample vibration data in parallel with transmitting it.

Each sensor experiences a vibration event once per hour. All vibration events for a particular node last the same amount of time. The shortest vibration event lasts 1 s and the longest lasts 10 s.

- (a) **(3 pts.)** What is the long-term average power consumption of the node with the shortest vibration events?

- (b) **(3 pts.)** What is the long-term average power consumption of the node with the longest vibration events?

(c) **(3 pts.)** The system is considered operational if and only if all nodes are operational. Each node has a separate battery. Given that all nodes use the same type of 3.2 V ideal battery, what mA-h rating is required for the system to last for 30 days? $1 \text{ J} = 1 \text{ W-s}$.

(d) **(3 pts.)** If all nodes have the same battery type, what is the battery lifespan of the longest-lived node?

8. (1 pts.) What does this cat represent?



- (a) Fowler-Nordheim tunneling.
- (b) Matthew Smith.
- (c) A tinning sponge.
- (d) Me, in my customer's eyes.
- (e) Society.

Done.

Overflow space. We won't look at this space unless you tell us to after the relevant question.