Youngwoo **Jeong**

System Architect · System Solution Group @ MangoBoost

jini221220@gmail.com | yw-ray.github.io/ | youngwoo-jeong-508b28264

Summary

Hello! I'm Youngwoo (Ray) Jeong, and I received my master degree in Electronic Engineering at Seoul University of Science and Technology in February 2024. My research focused on computer architecture, high-level synthesis (HLS), domain-specific accelerator, FPGA prototyping, HW/SW co-design. Currently, I am working at MangoBoost, a DPU startup company, where I joined the architecture team in March 2024.

Education

Seoul National University of Science and Technology — *Seoul, Republic of Korea*

M.S in Electronic Engineering — *Mar 2022 - Feb 2024*

- Advisor: Prof. Seung Eun Lee
- Lab: Computer Architecture Laboratory
- Thesis: Approximate Arithmetic Circuits for Embedded Fuzzy Logic Controller

Seoul National University of Science and Technology — *Seoul, Republic of Korea*

B.S in Electronic and IT Media Engineering — *Mar 2015 - Feb 2022*

- Advisor: Prof. Seung Eun Lee

Work Experience

MangoBoost — *Seoul, South Korea*

Hardware Engineer — *Mar 2024 - present*

- Architected an NVMe/TCP initiator (NTI) with dynamic ARM–FPGA acceleration, allowing protocol processing to be flexibly offloaded depending on performance requirements and hardware availability. This ensured both efficiency and reliability in large-scale deployments (e.g., Ceph).
- Extended scalability from the original 2 subsystems to 18 FPGA-accelerated functions via SR-IOV, while achieving full 200G line-rate throughput in aggregated performance tests. On the ARM side, designed a flexible execution path supporting up to 130 concurrent functions to enable diverse application workloads.
- Verified functionality and throughput using FIO benchmarks across multiple configurations (single disk, RAID, XFS).
- Measured real-world database performance with PostgreSQL (pgbench) workloads.

Selected Publications [Full list on Google Scholar]

- **SANA: Fast, Scalable, and Production-ready Storage Architecture with NVMe/TCP Acceleration (Under review)**
  International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2026
  MangoBoost
- **SEAM: A synergetic energy-efficient approximate multiplier for application demanding substantial computational resources** [URL]
  Integration. vol.101, 2025
  Youngwoo Jeong, Joungmin Park, Raehyeong Kim, Seung Eun Lee
- **Robot-Specific Processor for Autonomous Driving**
  1st Workshop on Robotics Acceleration with Computing Hardware (RoboARCH) (Co-located with MICRO), Chicago, USA, Oct., 2022
  Youngwoo Jeong, Kwang Hyun Go, Soohee Kim, Seung Eun Lee
- **An Architecture for Resilient Federated Learning through Parallel Recognition (Poster Session)** [URL]
  The 31st International Conference on Parallel Architectures and Compilation Techniques (PACT), Chicago, USA, Oct., 2022
  Jeongeun Kim, **Youngwoo Jeong**, Suyeon Jang, Seung Eun Lee
- **Photoplethysmography-Based Distance Estimation for True Wireless Stereo** [URL]
  Micromachines. vol.14, no.2, 2023
  Youngwoo Jeong, Joungmin Park, Sun Beom Kwon, Seung Eun Lee
- **An Edge AI Device Based Intelligent Transportation System** [URL]
  Journal of Information and Communication Convergence Engineering (JICCE). vol.20, no.3, 2022
  Youngwoo Jeong, Hyun Woo Oh, Soohee Kim, Seung Eun Lee

Patents

Federated Learning Method and System Using Shared Learning Data — *United States*

Seung Eun Lee, Jeongeun Kim, **Youngwoo Jeong** — *December 2023*

patent application

Method and System for Determining Final Result Using Federated Learning — *United States*

Seung Eun Lee, Jeongeun Kim, **Youngwoo Jeong** — *December 2023*

patent application

Research Project

Development for Processing Software on AI Semiconductor Devices — *South Korea*

Ministry of Science and ICT — *2024 - 2022*

- Analyzed various AI models to standardize the input for AI systems.
- Proposed an architecture for a hardware scheduler optimized for multi-AI core architecture.

Development of Proximity/Healthcare Convergence Sensor SoC for TWS — *South Korea*

Ministry of Trade, Industry and Energy — *2023 - 2021*

- Designed a test environment for photoplethysmography sensors to evaluate their performance.
- Proposed a waveform adjustment filter and AI-based distance estimation algorithm to enhance signal processing accuracy.

Embedded AI Module Based on Neuromorphic Computing — *South Korea*

Ministry of Trade, Industry and Energy — *2021 - 2020*

- Designed various applications utilizing multiple embedded AI modules.
- Developed a testbed for evaluating multi-AI core controllers.
- Proposed methodologies to enhance accuracy in federated learning with multi-AI core systems.

Honors & Awards

Excellent Thesis Award — *Seoul, South Korea*

Seoul National University of Science and Technology — *February 2024*

- **Topic: Approximate Arithmetic Circuits for Embedded Fuzzy Logic Controller**

Corporate (LX Semicon) Special Award — *Seoul, South Korea*

Korea Semiconductor Industry Association — *October 2022*

- **Topic: AI Processor employing Stochastic Computing for Embedded Systems**

Department Chair Award — *Seoul, South Korea*

Seoul National University of Science and Technology — *February 2022*

- **Topic: Design of an Autonomous Indoor Robot for Robot-on-Chip**

Teaching Experience

Advanced AI Processor, Computer Architecture — *Seoul, South Korea*

Seoul National University of Science and Technology — *Fall 2022*

Teaching Assistant

Digital System Design, Resilient Processor Design — *Seoul, South Korea*

Seoul National University of Science and Technology — *Spring 2022*

Teaching Assistant

Skills

Hardware Description Languages	Verilog
High-Level Computer Languages	SystemC, C, C++, Python, Matlab
Design and Implementation Tools	Catapult HLS, Design Compiler, IC Compiler II, Quartus II, Vivado
Verification and Analysis Tools	Verdi, VCS, ModelSim, PSpice, PrimeTime, Formality, StarRC
Benchmark Tools	Flexible I/O (FIO), PGbench

Chip Design

Design of Robot-Specific Processor for Autonomous Driving

- Technology: Samsung 28nm RFCMOS
- Designer: **Youngwoo Jeong**, Yue Ri Jeong, Hyun Woo Oh, Kwang Hyun Go
- Gate Counts: 1062K @ 50MHz
- Memory: Code region (16KB), Data region (128KB)
- Date: 2022. 07. 18