Mixed Signal Simulation

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March 3, 2015

Contents

1 Introduction

In the Cadence Virtuoso environment, it is easy to do the analog simulation in Spectre. The purpose of this manual is to illustrate the process to run the mixed signal simulation in the Virtuoso. I begin with the creating of the new verilog file, how to make symbol for the verilog netlist and then how to make the simulation file. The target is to run the mixed signal successfully.

2 Use the latest version of Virtuoso

Make sure you have the latest version of Virtuoso in your account.

Check your *cshrc* file, for example, you can use the command:

nedit ~ /*.cshrc*

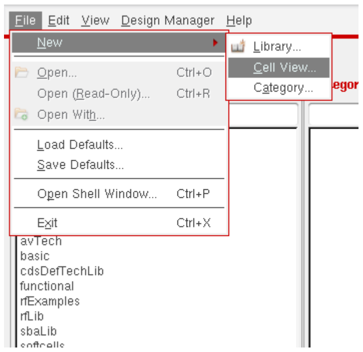
And make sure the version you are using is cadence615b:

```
source /users/iit/synopsys/source_synopsys01lnx
#source /users/iit/cadence/source_cadence615lnx
source /users/iit/cadence/source_cadence615b
#source /users/iit/cadence/source_cadence12lnx
```

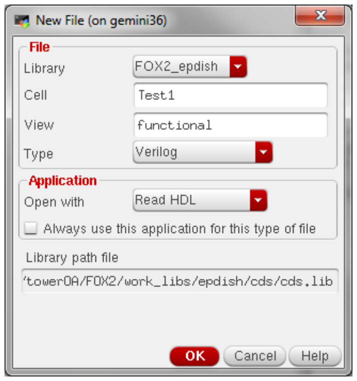
For the convenience of the simulation, I start with a very simple verilog netlist.

3 Create verilog file in Virtuoso

Just the same as we did for making new schematic file:



In the cell view, type functional with Type verilog


New File (on gemini36)

File

Library: FOX2_epdish
Cell: Test1
View: functional
Type: Verilog

Application

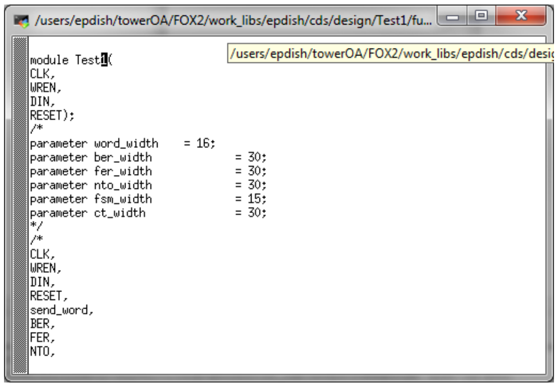
Open with: Read HDL
Always use this application for this type of file

Library path file: 'towerOA/FOX2/work_libs/epdish/cds/cds.lib

Note that the cell name of the cell should be the same as the module name in the verilog file.

4 Add the verilog code

The default editor for the verilog file is *vi*, then just add your verilog code in the file.

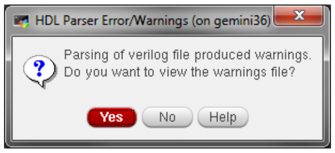


/users/epdish/towerOA/FOX2/work_libs/epdish/cds/design/Test1/fu...

/users/epdish/towerOA/FOX2/work_libs/epdish/cds/desig

```
module Test1(
CLK,
WREN,
DIN,
RESET);
/*
parameter word_width    = 16;
parameter ber_width             = 30;
parameter fer_width             = 30;
parameter nto_width             = 30;
parameter fsm_width             = 15;
parameter ct_width              = 30;
*/
/*
CLK,
WREN,
DIN,
RESET,
send_word,
BER,
FER,
NTO,
```

Then type ": *wq*" to escape *vi* and if there are errors/warnings in the verilog file, it will report.

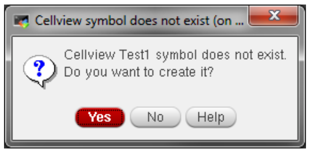


HDL Parser Error/Warnings (on gemini36)

Parsing of verilog file produced warnings.
Do you want to view the warnings file?

5 Create symbol for the cell

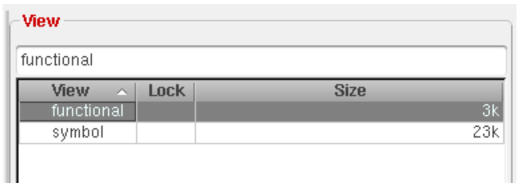
After we escape *vi* without error, we will get this window automatically, of course, we need to have the symbol for this cell, so click Yes.



Cellview symbol does not exist (on ...

Cellview Test1 symbol does not exist.
Do you want to create it?

Now we have 2 views in our cell:



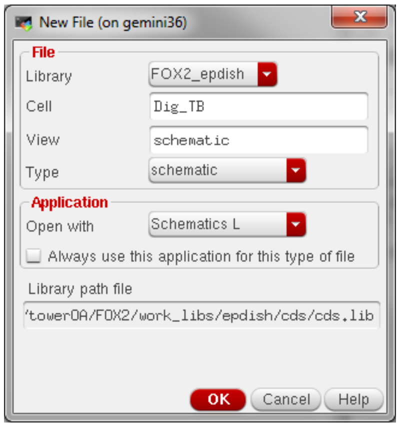
View

functional

View	Lock	Size
functional		3k
symbol		23k

6 Establish the test bench

For the test bench, the name is not important since we don't have verilog block here.


New File (on gemini36)

File

Library	FOX2_epdish
Cell	Dig_TB
View	schematic
Type	schematic

Application

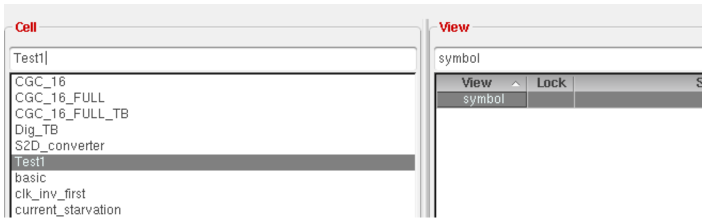
Open with	Schematics L

☐ Always use this application for this type of file

Library path file

'towerOA/FOX2/work_libs/epdish/cds/cds.lib

Then add the digital symbol and analog symbol into this test bench.


Cell

Test1

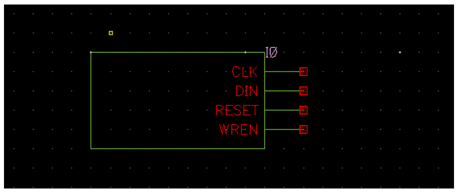
CGC_16
CGC_16_FULL
CGC_16_FULL_TB
Dig_TB
S2D_converter
Test1
basic
clk_inv_first
current_starvation

View

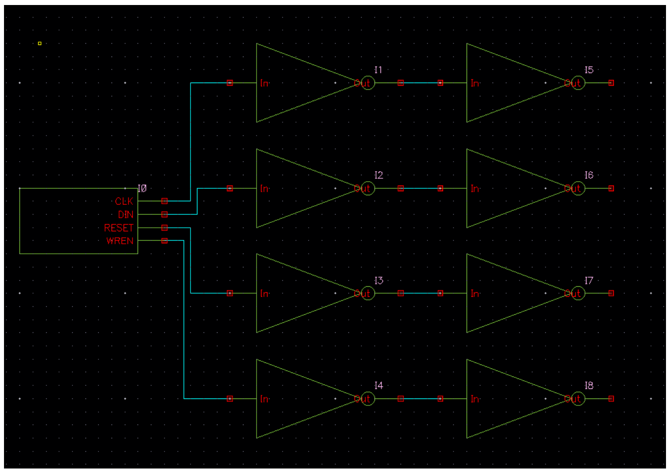
symbol

View	Lock
symbol	

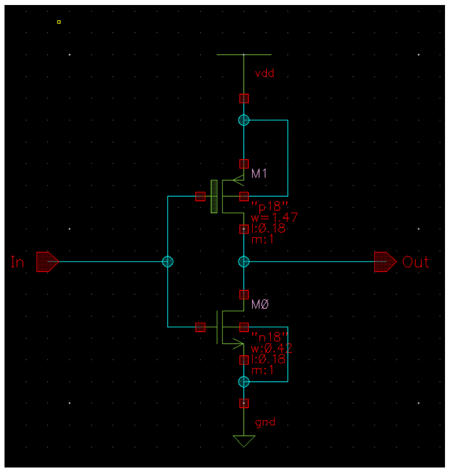
Select the symbol



Add the analog block, for convenience, I use 4 inverters to connect with the output ports of the digital controller.



The schematic for the inverter is still simple.

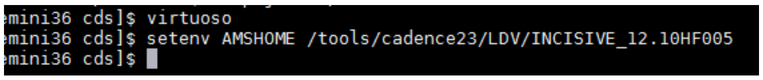


It's a basic inverter, but compared with the verilog file, we call it analog block.

7 Setting virtuoso

We need to run this command in the cmd:

setenv AMSHOME /tools/cadence23/LDV/INCISIVE_12.10HF005

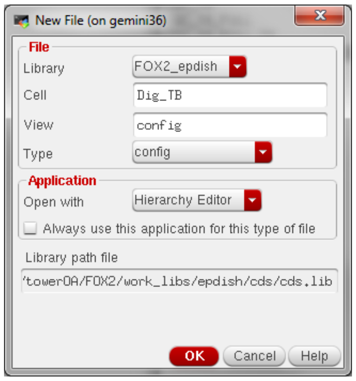


```
mini36 cds]$ virtuoso
mini36 cds]$ setenv AMSHOME /tools/cadence23/LDV/INCISIVE_12.10HF005
mini36 cds]$ █
```

Only need to run this command one time, once you have set, no need to run it again.

8 Make config file for test bench

In order to run the file we want to simulate, we need to make a config file for the test bench cell.

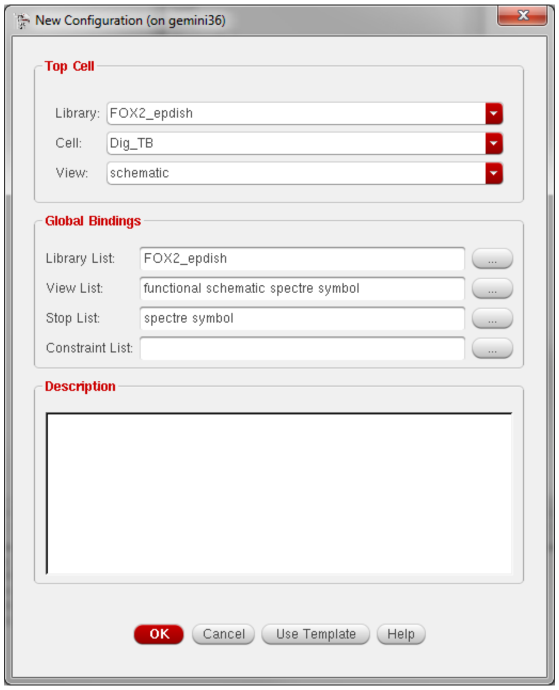


File
Library: FOX2_epdish
Cell: Dig_TB
View: config
Type: config

Application
Open with: Hierarchy Editor
Always use this application for this type of file

Library path file: 'towerOA/FOX2/work_libs/epdish/cds/cds.lib

Choose the view as schematic, and library list is your working library. Set the view list with the order “functional schematic spectre symbol”and the stop list as “spectre symbol”. Then click OK.

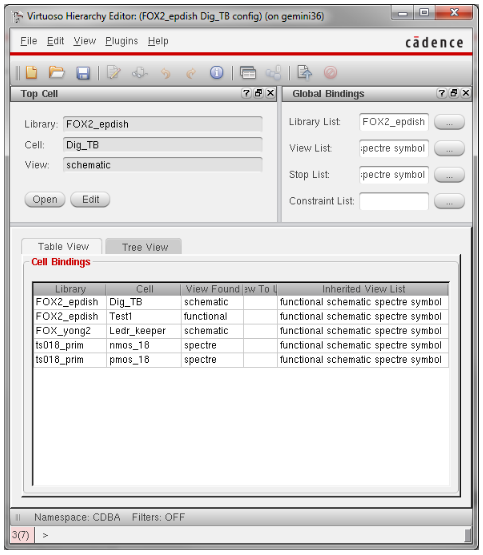


Top Cell
Library: FOX2_epdish
Cell: Dig_TB
View: schematic

Global Bindings
Library List: FOX2_epdish
View List: functional schematic spectre symbol
Stop List: spectre symbol
Constraint List:

Description

We will get the following window.


Virtuoso Hierarchy Editor: (FOX2_epdish Dig_TB config) (on gemini36)

File Edit View Plugins Help

Top Cell

Library: FOX2_epdish
Cell: Dig_TB
View: schematic

Global Bindings

Library List: FOX2_epdish
View List: ;pectre symbol
Stop List: ;pectre symbol
Constraint List:

Table View | Tree View

Cell Bindings

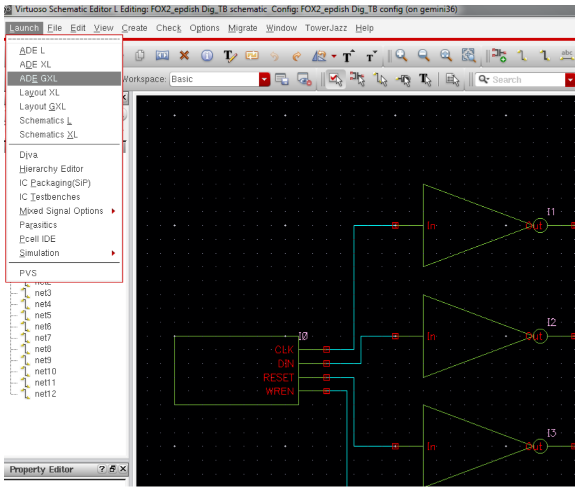
Library	Cell	View Found	ew To U	Inherited View List
FOX2_epdish	Dig_TB	schematic		functional schematic spectre symbol
FOX2_epdish	Test1	functional		functional schematic spectre symbol
FOX_yong2	Ledr_keeper	schematic		functional schematic spectre symbol
ts018_prim	nmos_18	spectre		functional schematic spectre symbol
ts018_prim	pmos_18	spectre		functional schematic spectre symbol

Namespace: CDBA Filters: OFF

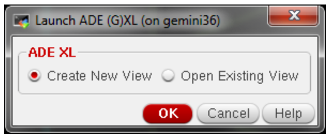
9 Establish the simulation environment

9.1 Lauch the simulation file

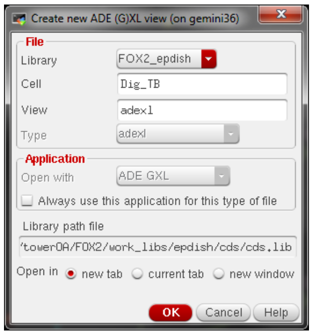
Click open from the config file we had above, and then add the simulation file.



Then choose create new view


Launch ADE (G)XL (on gemini36)
ADE XL
[✓ Create New View] Open Existing View
OK
Cancel
Help

And click OK and give it a name


Create new ADE (G)XL view (on gemini36)

File

Library	FOX2_epdish
Cell	Dig_TB
View	adexl
Type	adexl

Application

Open with	ADE GXL

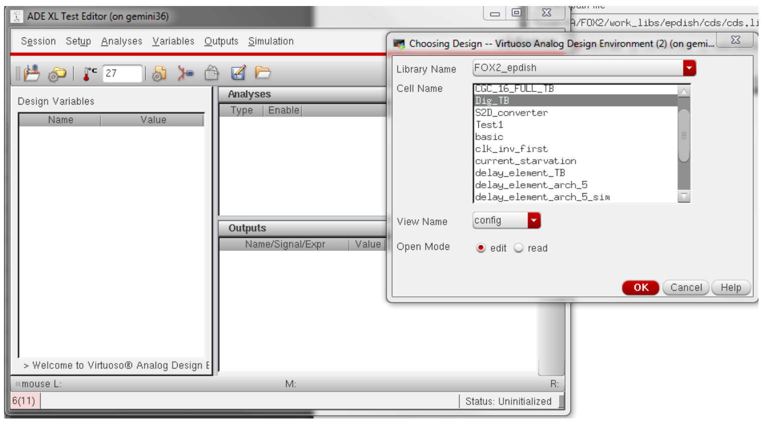
☐ Always use this application for this type of file

Library path file

'towerOA/FOX2/work_libs/epdish/cds/cds.lib

Open in [✓ new tab] current tab new window

Click OK again.


ADE XL Test Editor (on gemini36)
Session Setup Analyses Variables Outputs Simulation
27
Design Variables
Name
Value
Analyses
Type
Enable
Outputs
Name/Signal/Expr
Value

> Welcome to Virtuoso® Analog Design E

mouse L: M: R:

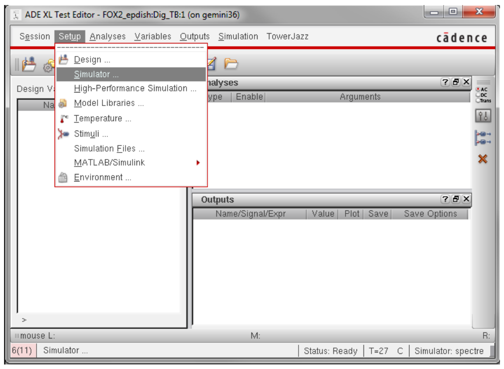
6(11) Status: Uninitialized

Choosing Design -- Virtuoso Analog Design Environment (2) (on gemi...

Library Name	FOX2_epdish
Cell Name	CGC_16_FULL_TB
	Dig_TB
	S2D_converter
	Test1
	basic
	clk_inv_first
	current_starvation
	delay_element_TB
	delay_element_arch_5
	delay_element_arch_5_sim
View Name	config
Open Mode	[✓ edit] read

9.2 Make new test

Establish the new test and choose the view name as in config in the sub window above (Just click OK, the default is correct).

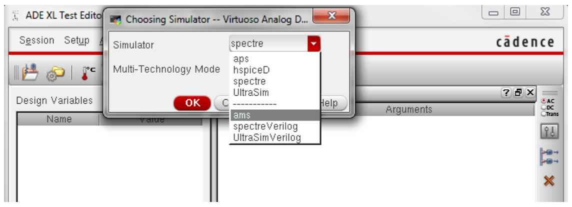


mouse L: M: R:

6(11) Simulator ... Status: Ready T=27 C Simulator: spectre

9.3 Set up simulator

Then in the ADE XL editor, setup and then simulator.



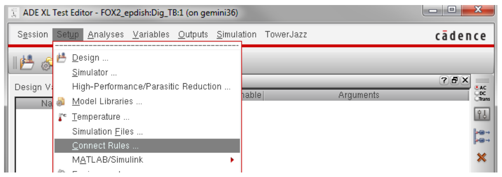
Select "ams" instead of "spctre" in simulator and click OK

9.4 Set up connect rules

In order to set the connect rule, add the connect rule in the cds.lib frist.

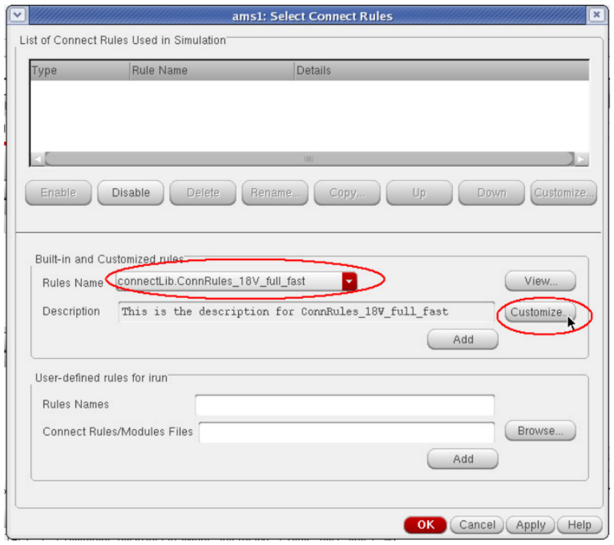
DEFINE connectLib /tools/cadence23/LDV/INCISIVE_12.10HF005/tools.lnx86/affirma_ams/etc/connect_lib /connectLib

Then from the connect rules, we can see the required connect ruels


ADE XL Test Editor - FOX2_epdish:Dig_TB:1 (on gemini36)
Session Setup Analyses Variables Outputs Simulation TowerJazz
cādence
Design ...
Simulator ...
High-Performance/Parasitic Reduction ...
Model Libraries ...
Temperature ...
Simulation Files ...
Connect Rules ...
MATLAB/Simulink
Design V
Arguments

Open ADE→ Setup → Connect Rule

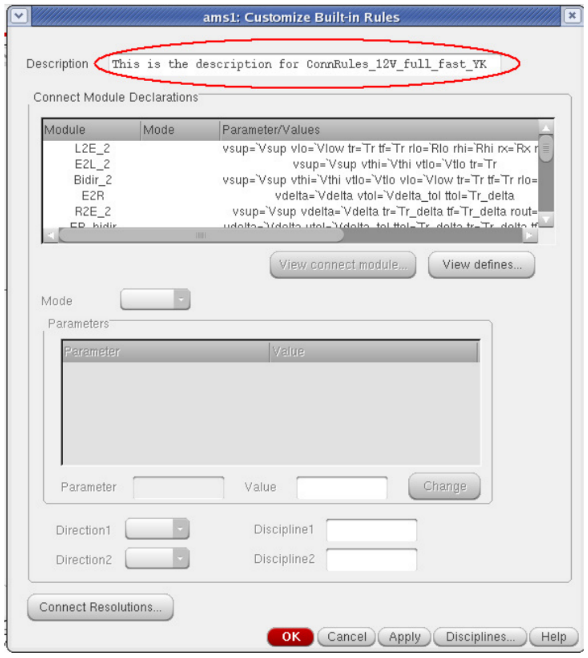
Select connect module from the "*Built-in and Customized rules"* and click *customize*:


ams1: Select Connect Rules
List of Connect Rules Used in Simulation
Type
Rule Name
Details
Enable
Disable
Delete
Rename...
Copy...
Up
Down
Customize...
Built-in and Customized rules
View...
Customize...
Add
User-defined rules for irun
Rules Names
Connect Rules/Modules Files
Browse...
Add
OK
Cancel
Apply
Help

Rules Name: connectLib.ConnRules_18V_full_fast

Description: `This is the description for ConnRules_18V_full_fast`

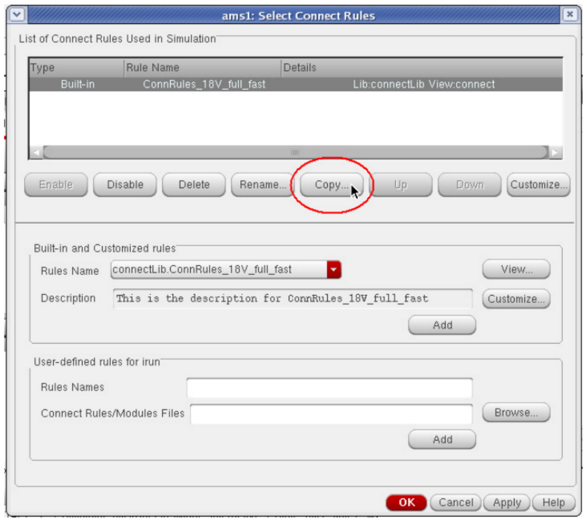
Change the Description and click o.k.



Description: `This is the description for ConnRules_12V_full_fast_YK`

Module	Mode	Parameter/Values
L2E_2		vsup=`Vsup vlo=`Vlow tr=`Tr tf=`Tr rlo=`Rlo rhi=`Rhi rx=`Rx r
E2L_2		vsup=`Vsup vthi=`Vthi vtlo=`Vtlo tr=`Tr
Bidir_2		vsup=`Vsup vthi=`Vthi vtlo=`Vtlo vlo=`Vlow tr=`Tr tf=`Tr rlo=
E2R		vdelta=`Vdelta vtol=`Vdelta_tol ttol=`Tr_delta
R2E_2		vsup=`Vsup vdelta=`Vdelta tr=`Tr_delta tf=`Tr_delta rout=
ER_bidir		vdelta=`Vdelta vtol=`Vdelta_tol ttol=`Tr_delta tr=`Tr_delta tf

Click add, then select the added new connect rule and click copy:


ams1: Select Connect Rules

List of Connect Rules Used in Simulation

Type	Rule Name	Details
Built-in	ConnRules_18V_full_fast	Lib:connectLib View:connect

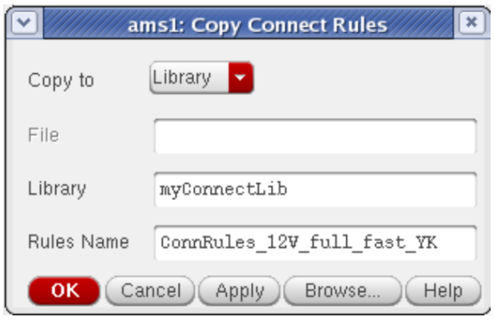
Built-in and Customized rules

Rules Name	connectLib.ConnRules_18V_full_fast
Description	This is the description for ConnRules_18V_full_fast

User-defined rules for irun

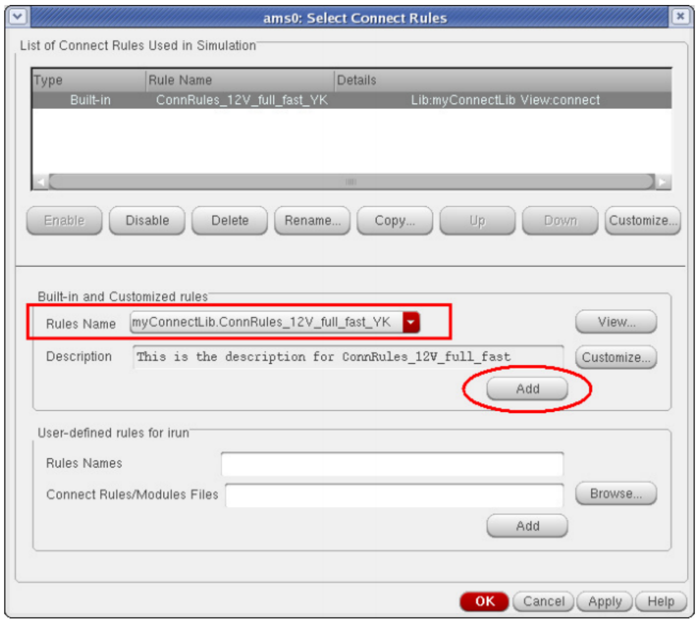
Rules Names	
Connect Rules/Modules Files	

Copy to destination library and make sure to update the Rule name field


ams1: Copy Connect Rules

Copy to	Library
File	
Library	myConnectLib
Rules Name	ConnRules_12V_full_fast_YK

As long as myConnectLib is defined in the cds.lib, you will be able to add the new connect rule.



List of Connect Rules Used in Simulation

Type	Rule Name	Details
Built-in	ConnRules_12V_full_fast_YK	Lib:myConnectLib View:connect

Built-in and Customized rules

Rules Name: myConnectLib.ConnRules_12V_full_fast_YK

Description: This is the description for ConnRules_12V_full_fast

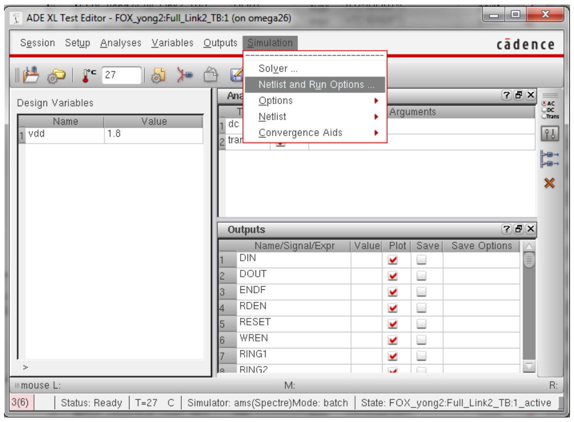
User-defined rules for irun

Rules Names:

Connect Rules/Modules Files:

9.5 Set the simulation Option

Finally you can set the simulation option, as illustrated below.



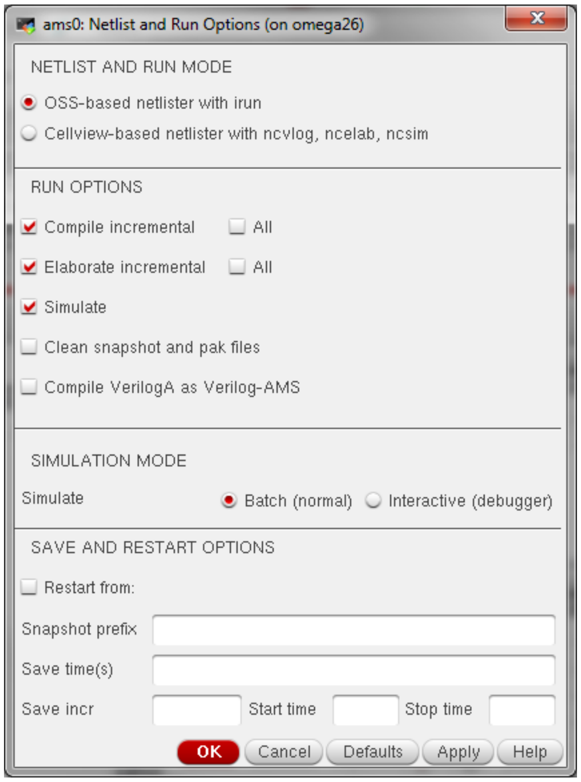
Design Variables

	Name	Value
1	vdd	1.8

	Name/Signal/Expr	Value	Plot	Save	Save Options
1	DIN		✓	☐	
2	DOUT		✓	☐	
3	ENDF		✓	☐	
4	RDEN		✓	☐	
5	RESET		✓	☐	
6	WREN		✓	☐	
7	RING1		✓	☐	
8	RING2		✓	☐	

mouse L: M: R:

3(6) | Status: Ready | T=27 C | Simulator: ams(Spectre)Mode: batch | State: FOX_yong2:Full_Link2_TB:1_active


ams0: Netlist and Run Options (on omega26)

NETLIST AND RUN MODE

- [✓ OSS-based netlister with irun]
- Cellview-based netlister with ncvlog, ncelab, ncsim

RUN OPTIONS

- [✓] Compile incremental — [ ] All
- [✓] Elaborate incremental — [ ] All
- [✓] Simulate
- [ ] Clean snapshot and pak files
- [ ] Compile VerilogA as Verilog-AMS

SIMULATION MODE

Simulate: [✓ Batch (normal)] Interactive (debugger)

SAVE AND RESTART OPTIONS

- [ ] Restart from:

Snapshot prefix:

Save time(s):

Save incr: Start time: Stop time:

Done! Now you can run the mixed signal simulation!!!