DRCLVS for digital block

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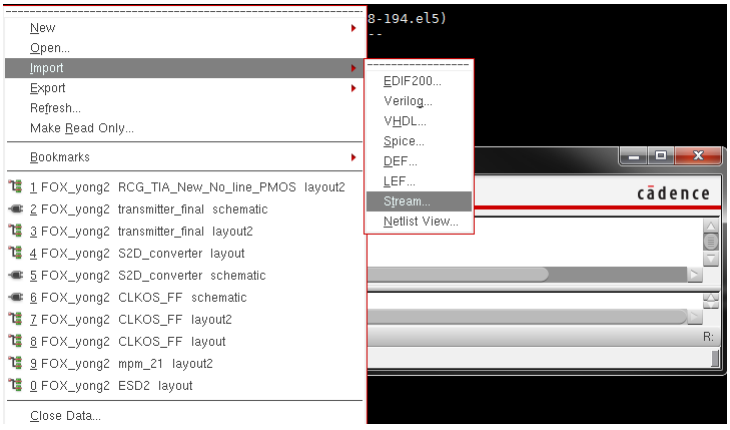
Contents

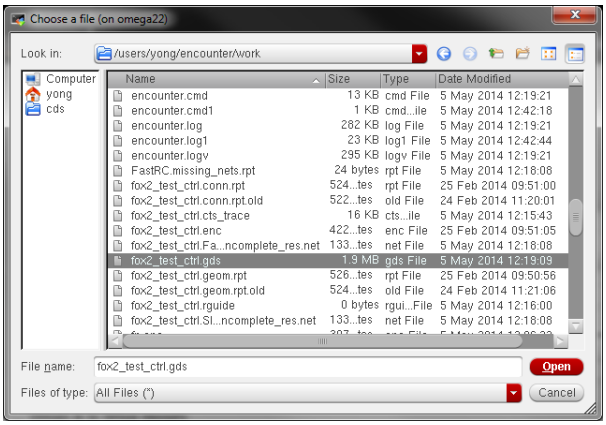
1 Stream Out the gds file

After the route in the encounter, we run this command:

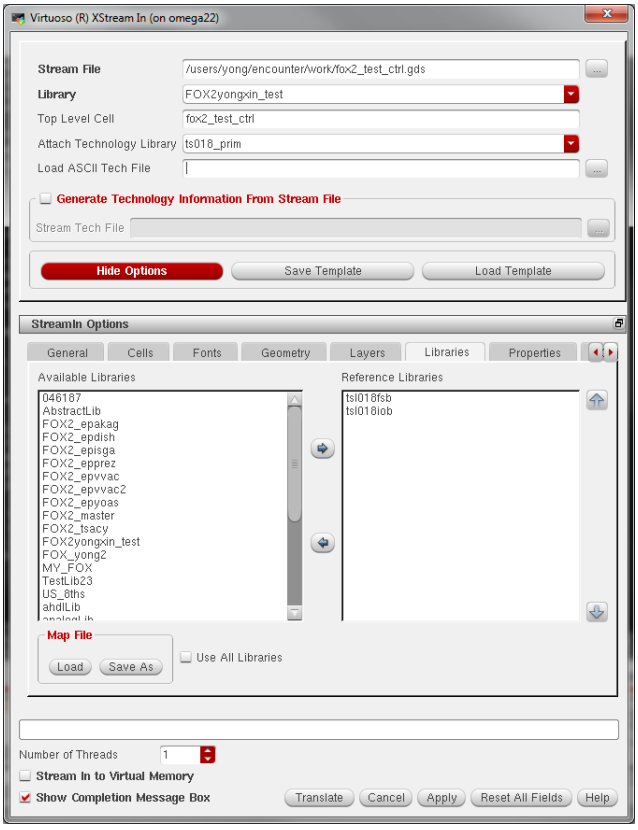
```
streamOut fox2_test_ctrl.gds -mapFile /users/iit/cadence/tsl018b/gds2_6lm.map
-libName DesignLib -units 1000 -mode ALL
```



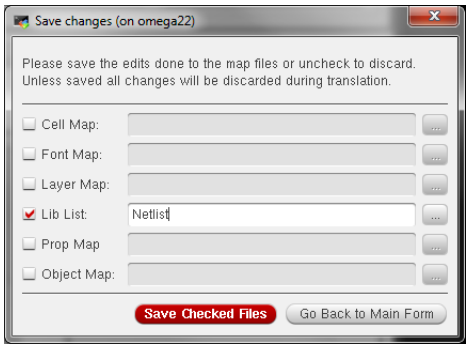
Then, open virtuoso and import stream:



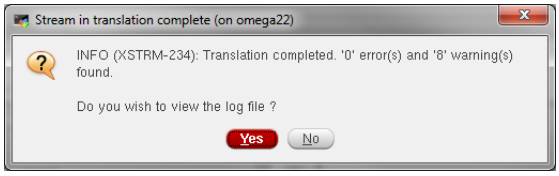
Click open, and then click the show Option. Then go to libraries and add the 2 libraries as shown here.



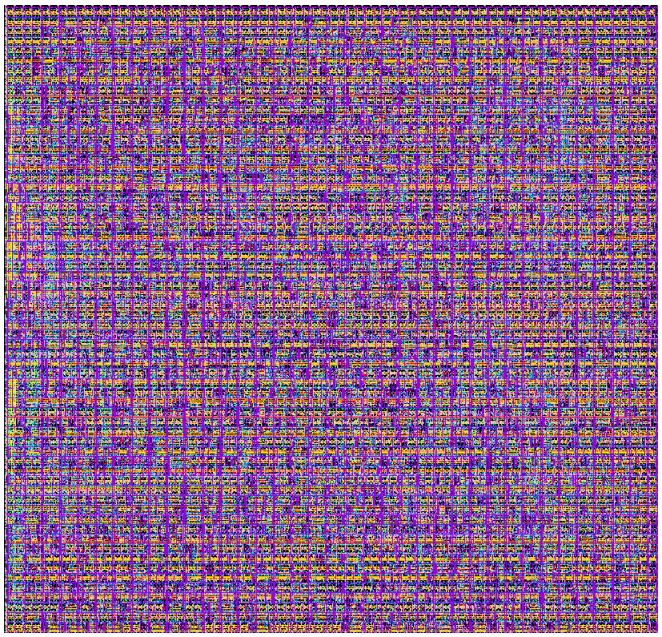
Finally, click translate



Add, “Netlist”in the text window and chick “Saved checked files”

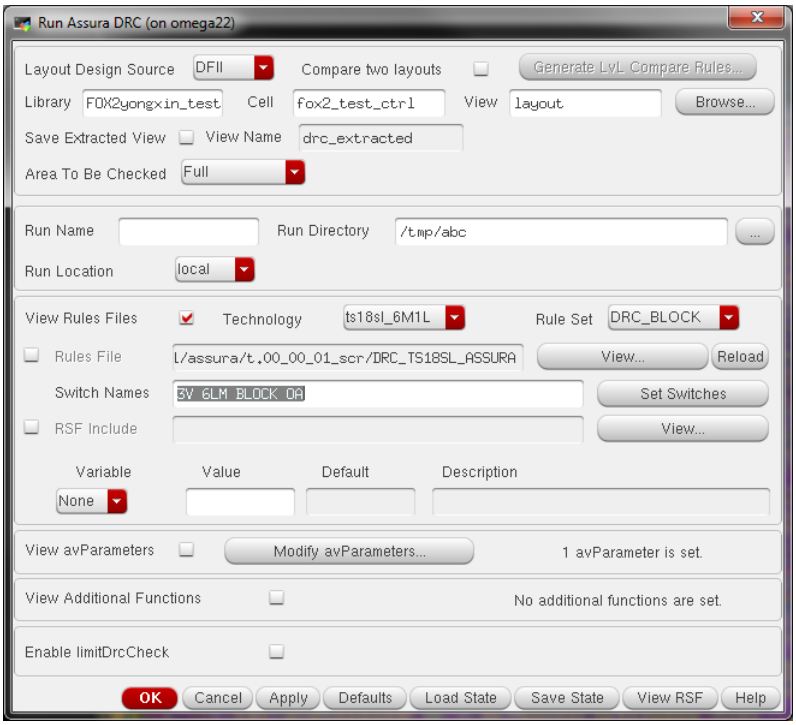


Then, open the imported file in Virtuoso

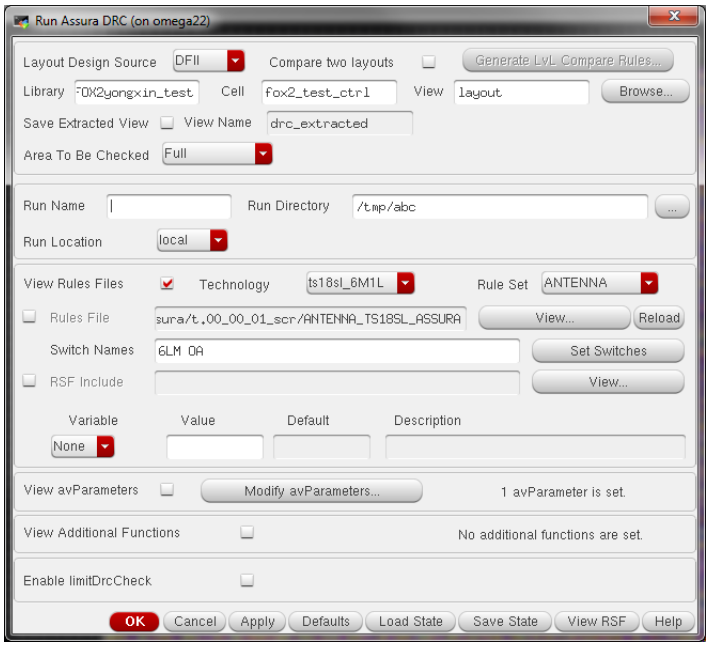


2 DRC check

`Run the DRC, frist Run DRC_BLOCK or DRC_CHIP (depends it is the final chip or just one block)`



If it passed the DRC check, we will Run the DRC fro antenna



I passed this check also

3 LVS Check

In order to Run the LVS, we need to make a new folder that contains the gate level verilog file and then execute the following command to get the cdl file:

```
/tools/mentor90/Calibre/ixl_cal_2009.4_16.13/bin/v2lvs -v top.v -o top.cdl
```

```
Info: Creating Design Database ...
Info: Converting Design ...
Warning: Duplicate port/net name "n1784" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n642" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n673" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n704" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n735" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n766" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n797" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n828" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n859" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n890" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n921" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n952" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: Duplicate port/net name "n983" found in module "fox2_test_ctrl" while doing case-insensitive lookup
Warning: No module declaration for module invhdk first encountered in module fox2_test_ctrl
```

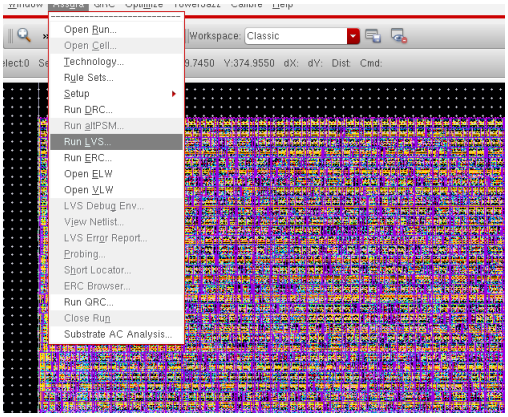
Change the name in the .cdl file to get rid of errors for the LVS (we need to change the small letter and capital letter of the wire name inside of the cdl file)

Then add the following lines at the beginning of the cdl file:

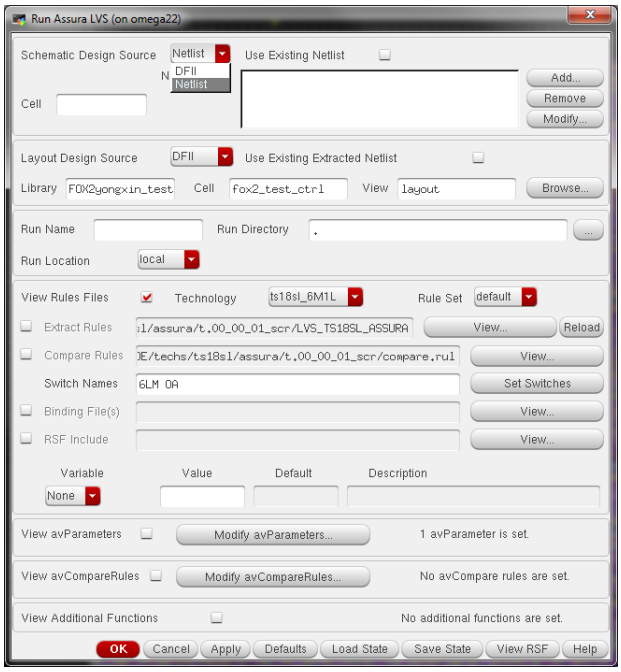
.GLOBAL VSS
.GLOBAL VDD
.include /users/iit/cadence/tsl018b/cdl/tsl18fs120.cdl
.include /users/iit/cadence/tsl018b/cdl/tsl18cio150.cdl

After that, change the word "$PINS" in the cdl file to be "$PINS VDD=VDD VSS=VSS" and save the final cdl file

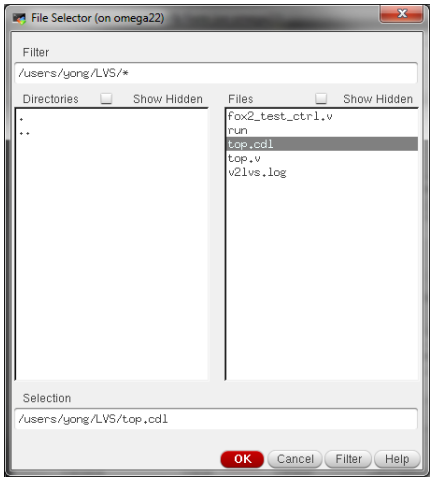
Then open the final layout of the digital block in Virtuoso first



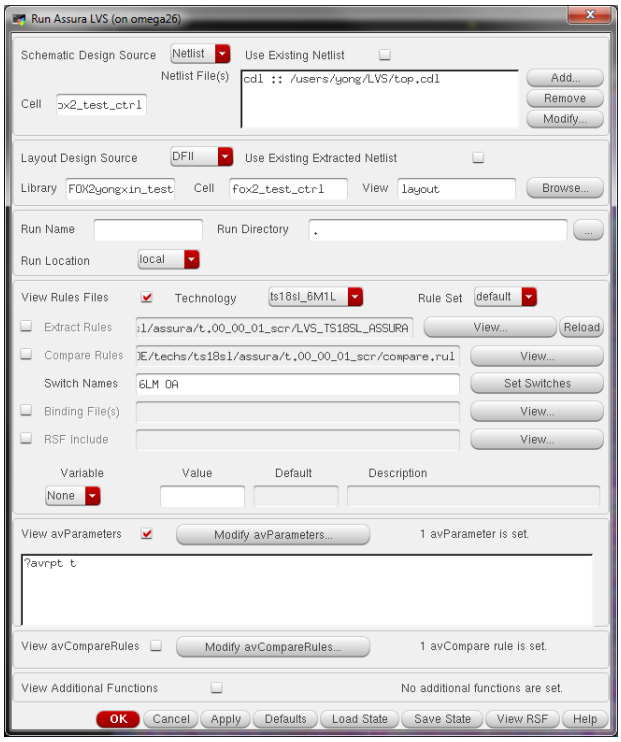
Then add the schematic source by choosing the netlist as follows



After that, Click Add button and add the cdl file that you got above



Choose the top.cdl file that we have had.



Before run the LVS, make sure you have chosen the correct cell name for the cdl file and you are supposed to get the final layout report: