Yixiao Du

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Education

- **Cornell University** *Aug. 2020 - present*
  MS/Ph.D. in Electrical and Computer Engineering, Advisor: Zhiru Zhang Ithaca, United States
- **Cornell University** *Aug. 2019 - Aug. 2020*
  Master of Engineering in Electrical and Computer Engineering Ithaca, United States
  - GPA: 4.04/4.25
  - Transferred to MS/Ph.D. program in Aug. 2020
- **University of Electronics Science and Technology of China** *Sep. 2015 - Jun. 2019*
  Bachelor of Engineering in Microelectionics Science and Engineering Chengdu, China
  - GPA: 3.91/4.00

Work Experience

- **RapidStream Design Automation, Inc.** *May 2025 - Aug. 2025*
  Research Intern, Mentor: Licheng Guo Remote
  - Studied automated floorplanning and parallel implementation for dataflow architectures on FPGAs.
- **MangoBoost, Inc. [https://www.mangoboost.io]** *May 2023 - Dec. 2023*
  Research Intern, Mentor: Eriko Nurvitadhi Bellevue, WA
  - Built hardware in Verilog to characterize the high-bandwidth memory (HBM) system on AMD Alveo U55C FPGA.
  - Explored functional simulation of HLS designs interfacing with NVMe.

Publications

[1] Hanchen Jin, Zichao Yue, Zhongyuan Zhao, **Yixiao Du**, Chenhui Deng, Nitis Srivastava, Zhiru Zhang. **Vesper: A Versatile Sparse Linear Algebra Accelerator With Configurable Compute Patterns** . *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Nov. 2024.

[2] Jiajie Li, Jan-Niklas Schmelzle, **Yixiao Du**, Simon Heumos, Andrea Guarracino, Giulia Guidi, Pjotr Prins, Erik Garrison, Zhiru Zhang. **Rapid GPU-Based Pangenome Graph Layout** . *International Conference for High Performance Computing, Networking, Storage, and Analysis (SC)*, Nov. 2024.

[3] Hongzheng Chen, Jiahao Zhang, **Yixiao Du**, Shaojie Xiang, Zichao Yue, Niansong Zhang, Yaohui Cai, Zhiru Zhang. **Understanding the Potential of FPGA-Based Spatial Acceleration for Large Language Model Inference** . *ACM Transactions on Reconfigurable Technology and Systems (TRETS)*, Mar. 2024.

[4] **Yixiao Du**, Yuwei Hu, Zhongchun Zhou, Zhiru Zhang. **High-Performance Sparse Linear Algebra on HBM-Equipped FPGAs Using HLS: A Case Study on SpMV** . *International Symposium on Field-Programmanle Gate Arrays (FPGA)*, Feb. 2022.

[5] Yuwei Hu, **Yixiao Du**, Ecenur Ustun, Zhiru Zhang. **GraphLily: Accelerating Graph Linear Algebra on HBM-Equipped FPGAs** . *International Conference on Computer-Aided Design (ICCAD)*, Nov. 2021.

Honors and Awards

- **ECE Outstanding Ph.D. Teaching Assistant Award** *Apr. 2023*
  School of Electrical and Computer Engineering, Cornell University
  - Only one winner per year with 3000$ cash award.

Services

- **Reviewer:** ACM Transactions of Reconfigurable Technology and Systems (TRETS)
- **Artifact Evaluator:** International Symposium of Field-Programmable Gate Arrays (FPGA) 2023

SKILLS

- Familiar with architectural and micro-architectural design, memory access optimization, AXI on-chip system design, and optimization for timing closure. Understand AI/LLM inference principles and common methods for graph/sparse processing.
- **Hardware Description Languages:** Verilog, System Verilog
- **Programming Languages:** C/C++, Python
- **CAD Tools:** Vivado, Vitis HLS, Catapult HLS, Cadence Virtuoso