Application Note AN_A7130_HW

General Information

Document Title

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Revision History

Rev.	History	Issue Date	Remark
0.0	Initial Issue	August, 2011	Preliminary
0.1	Modify the Frequency Tolerance	September, 2011	Preliminary
0.2	Modify the Equivalent Series Resistor	November, 2011	Preliminary
0.3	Add RSSI Calculation with AGC off	January, 2012	Preliminary
0.4	Modify the default setting of Tx Power	April, 2015	Preliminary

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1. Crystal Selection Guide

To select an appropriate crystal for A7130 is important for good RF performance. If users are not familiar with how to choose the X'tal, we suggest them to use the one in BOM of MD7130-A01 module spec. The X'tal spec. shown in table 1 is a suitable example. Users can also get more information in "*FQA_0001_Xtal Selection*". Users can adjust frequency by tuning the external capacitor at A7130 XI and XO pins or use setting CSXTAL in register [2A]DASP0. Please read A7130 datasheet or contact our FAE for detail.

Quartz Crystal Specification	**SMD 3225 (TST)**
Center Frequency	16 MHz
Frequency tolerance at room temperature	±30 ppm
Frequency stability over operation temperature	±20 ppm
Load Capacitance	18 pF
Equivalent Series Resistor (ESR)	≦80Ω
Shunt Capacitance	2 pF
External Capacitor at A7130 XI pin	NC
External Capacitor at A7130 XO pin	NC

Table 1 Quartz Crystal Specification

Annotation:

A7130 can works well with a X'tal with ESR < 100 Ω. However, the X'tal settling time will get longer with higher ESR. The X'tal shown in BOM of MD7130-A01 module spec. is fully tested. If users have problems with X'tal selection, please contact your X'tal supplier or Amiccom's FAE.

2. Application Circuit and Layout Guide

2.1 Application Circuit

MD7130-A01-03 is AMICCOM's reference design for 2.4GHz high data rate transmission application (please see module spec. for the last update). The schematic is as Fig. 2.1a and the layout is as Fig. 2.1b. This document mainly notifies some key points which should be paid attention while doing PCB layout.

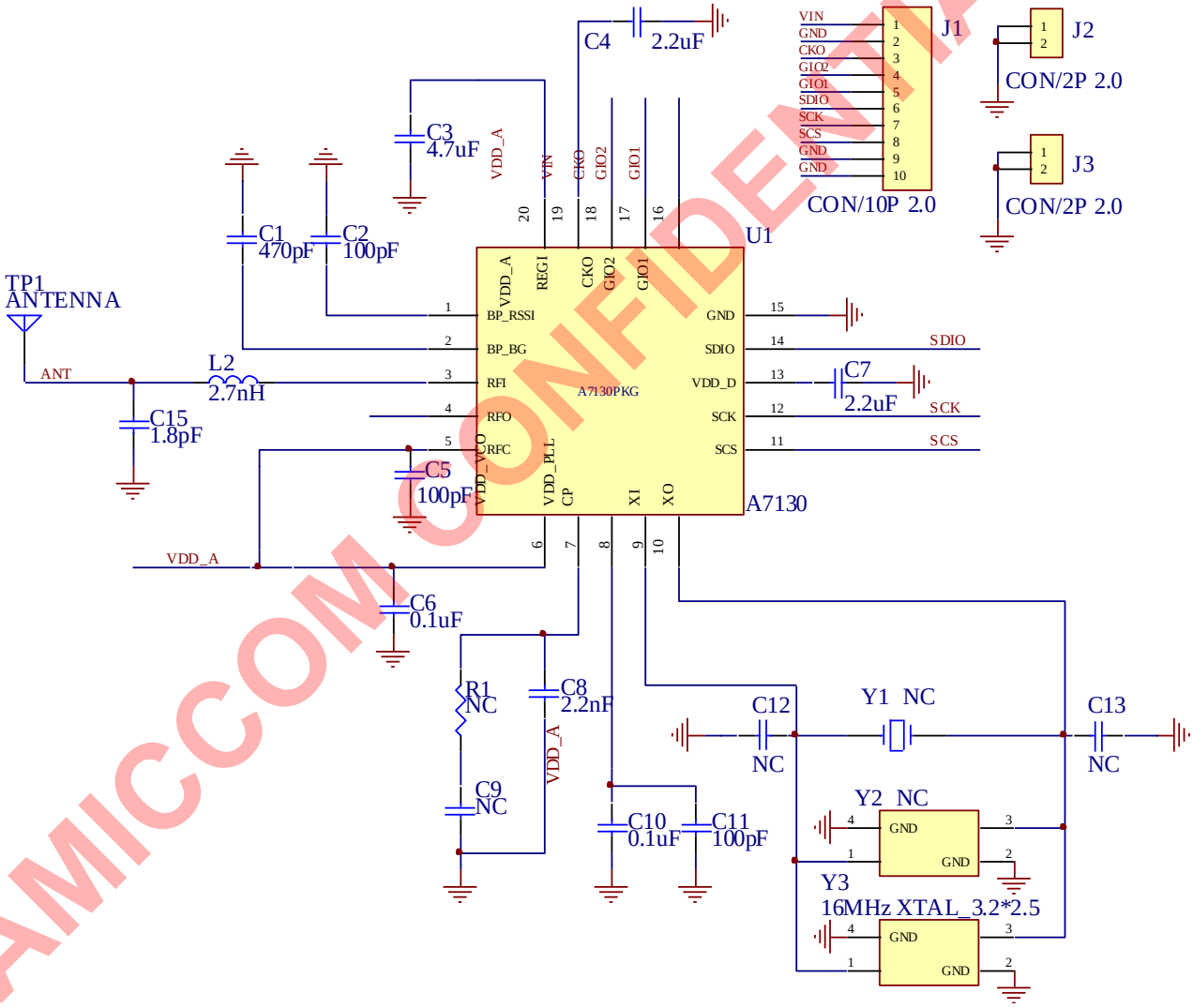

Fig. 2.1a Schematic of MD7130-A01-03

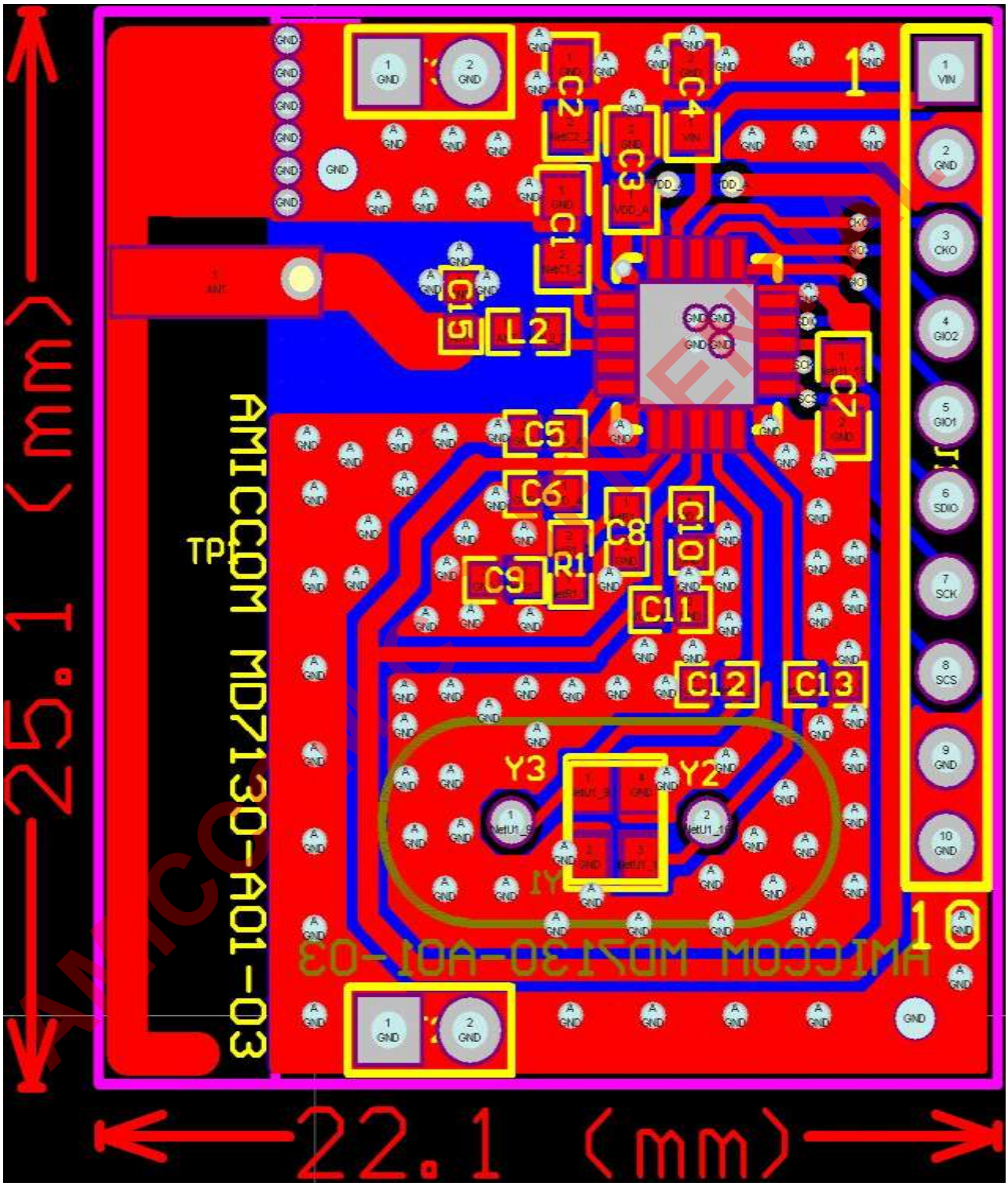

Fig. 2.1b Layout of MD7130-A01-03

2.2 Layout Guide

1. Bad ground plane always induce poor RF performance. Hence, a solid ground where it under the IC should be intact and not fragmentary can make the best RF performance of A7130. Please refer to Fig. 2.1b.

2. The impedance of RF path should be as close to 50 ohm as possible, and the RF trace should also be as short as possible. The ground plane below all RF traces must be intact and not fragmentary. The matching network (L2 and C15) should be placed close to A7130 IC because the matching network affects RF performance (power, and current) heavily. Therefore, we strongly recommend user to follow components placement and layout where shown by white traces in Fig. 2.2a. without any change.

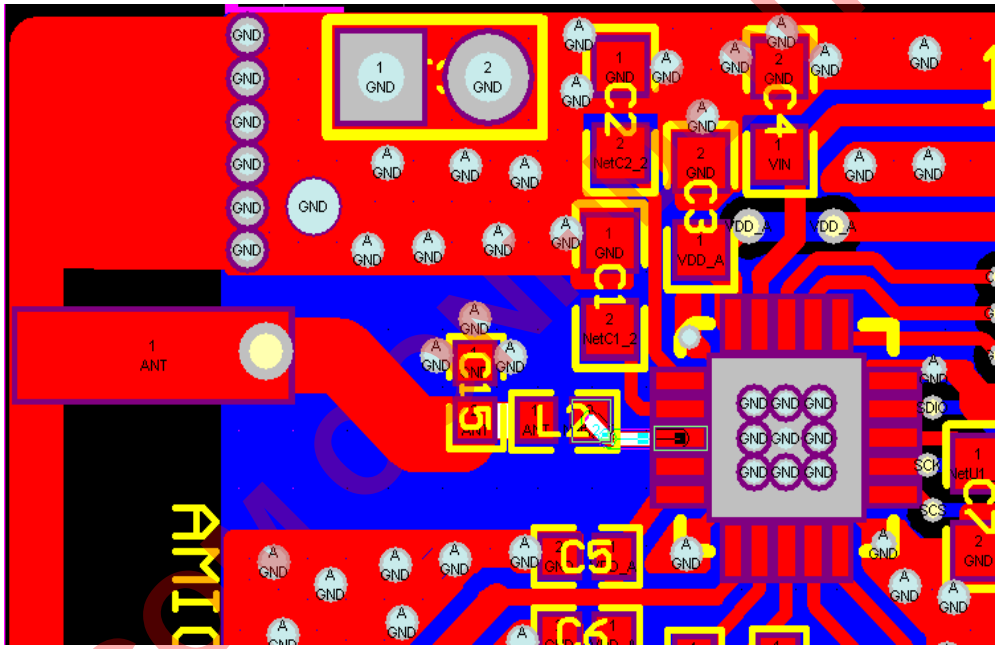

Fig. 2.2a RF matching trace (white)

4. In addition to ground plane, the clean and stable VDD source is also a key factor to impact RF performance. The bypass capacitors (C1, C2, C3, C4, C5, C6, C8, C10, C11) on this reference design is used for this purpose. To have the clean VDD source to A7130, those capacitors should be placed as close to the IC pins as possible and its ground via should be just nearby the components ground pad. Please refer to Fig. 2.1b.

5. C8 is PLL loop filter capacity. This capacitor (C8) should be correct and be close to IC pin 7 to for good PLL performance. Please refer to Fig. 2.1b.

6. The X'tal traces should be as short as possible and are better to be isolated by ground via. In addition, to minimize cross talk issue, components placement shall be as far away to X'tal trace as possible. Please refer to the white traces in Fig. 2.2c.

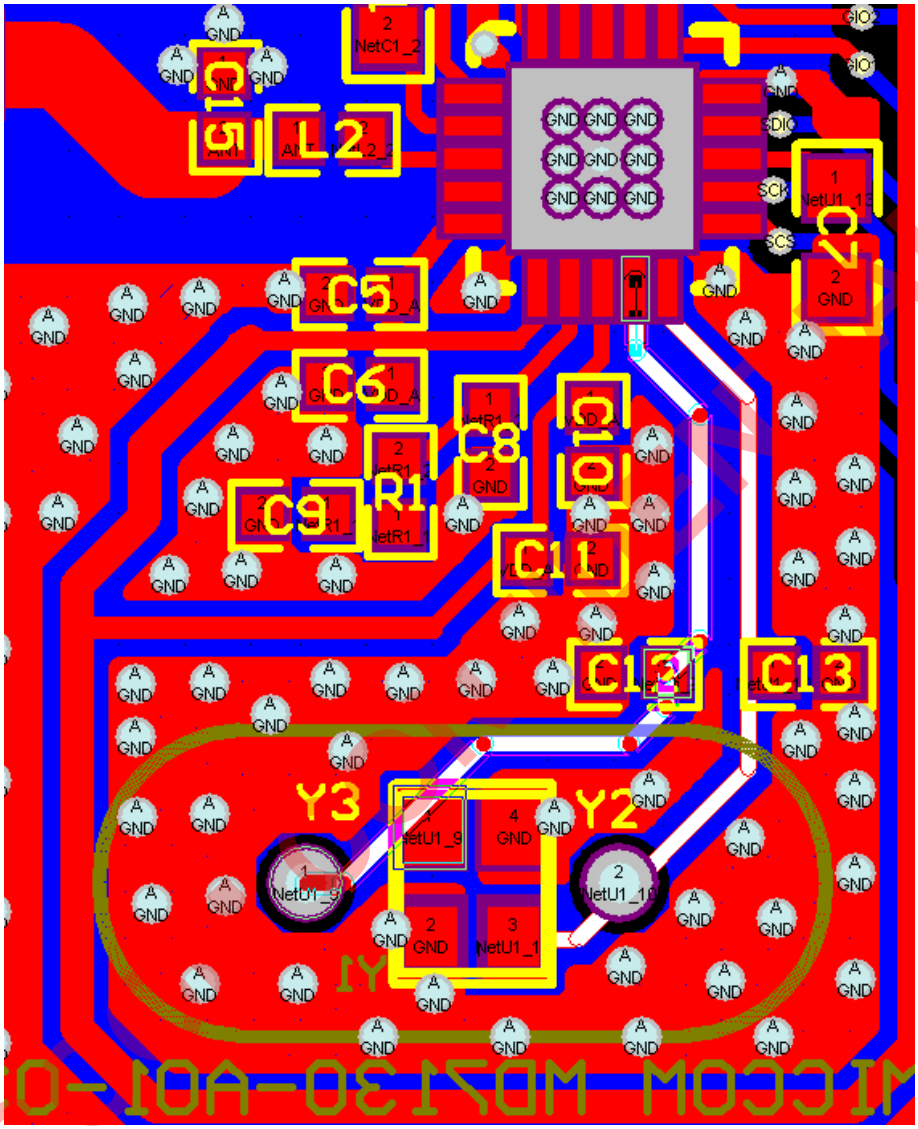

Fig. 2.2c X'tal trace (white)

3. Tx Power Control Setting

Users can get different TX power by setting TBG (Tx Buffer Gain), PAC (PA Current Select), and TXCS (TX Current Select) in register [2Dh] and PWORS (Tx high power setting) in register [24h] as the tables below. The default setting of register [2Dh] is 0x37 (TBG is set 7, PAC is set 2, TXCS is set 1) and register [24h] is 0xFF (PWORS is set 1). The power maybe change between different modules because the variation of components.

3.1 Power control setting

Tx Output Power and Current [PWORS=1]		PAC							
		0		1		2		3	
		power(dBm)	current(mA)	power(dBm)	current(mA)	power(dBm)	current(mA)	power(dBm)	current(mA)
TBG	0	0.43	18.74	1.37	19.83	2.41	21.67	3.24	24.87
	1	0.70	18.94	1.62	20.02	2.66	21.84	3.50	24.97
	2	1.05	19.19	1.96	20.29	2.98	22.10	3.83	25.12
	3	1.59	19.61	2.45	20.71	3.44	22.47	4.28	25.43
	4	2.27	20.19	3.09	21.27	4.02	23.03	4.77	25.77
	5	3.16	21.01	3.86	22.05	4.65	23.73	5.24	26.27
	6	4.01	22.01	4.60	23.02	5.18	24.55	5.56	26.73
	7	4.64	23.08	5.08	23.97	5.48	25.33	5.73	27.33

Tx Output Power and Current PWORS=0		PAC							
		0		1		2		3	
		power(dBm)	current(mA)	power(dBm)	current(mA)	power(dBm)	current(mA)	power(dBm)	current(mA)
TBG	0	-17.51	14.83	-15.52	15.95	-14.33	18.10	-13.84	21.57
	1	-14.77	14.93	-12.76	16.04	-11.53	18.16	-11.06	21.64
	2	-12.03	15.10	-10.03	16.18	-8.76	18.25	-8.24	21.67
	3	-8.73	15.50	-6.88	16.49	-5.55	18.46	-5.00	21.79
	4	-5.47	16.16	-3.88	17.10	-2.54	18.85	-1.90	22.01
	5	-2.14	17.25	-0.96	18.17	0.20	19.76	0.98	22.50
	6	0.77	18.93	0.52	19.88	2.63	21.38	3.51	23.71
	7	3.07	20.93	3.75	21.85	4.50	23.23	5.05	25.23

Annotation:

The input voltage is 3.3V(REGI) and P.A. voltage(1.8V) is from A7130 regulator.

4. Sensitivity Flatness

Users can set different channel by setting CHN (channel number) in register [0Fh]. The default setting of register [0Eh] is 0x50 by 4M bps data rate. When Tx frequency is in the N*16MHz (X'tal frequcncy) ± 2MHz, the sensitivity will degrade a little because of the interference from the X'tal. We suggest customers avoid using these channels.

5. RSSI

A7130 has built-in digital RSSI (Received Signal Strength Indicator) which measure the strength of the incoming RF signal. The digital RSSI can be read form ADC value and its range is form 0 to 255 (8bits). In the linear range, users can use the formula below to get the rough input power of the module.

Pin (dBm) = 12 * [(ADC-RL) / (RH-RL)] – 58 (AGC ON)

Pin (dBm) = 12 * [(ADC-RL) / (RH-RL)] – 80 (AGC OFF)

ADC, RL and RH value can be read from the registers.

The ADC values of each IC may have slight difference. If customers want to get more accurate RSSI value, they should use the ICs with RSSI tuning. Please contact Amiccom's FAE for detail about the RSSI tuning.

Typical RSSI characteristic is shown in Fig. 5.1.

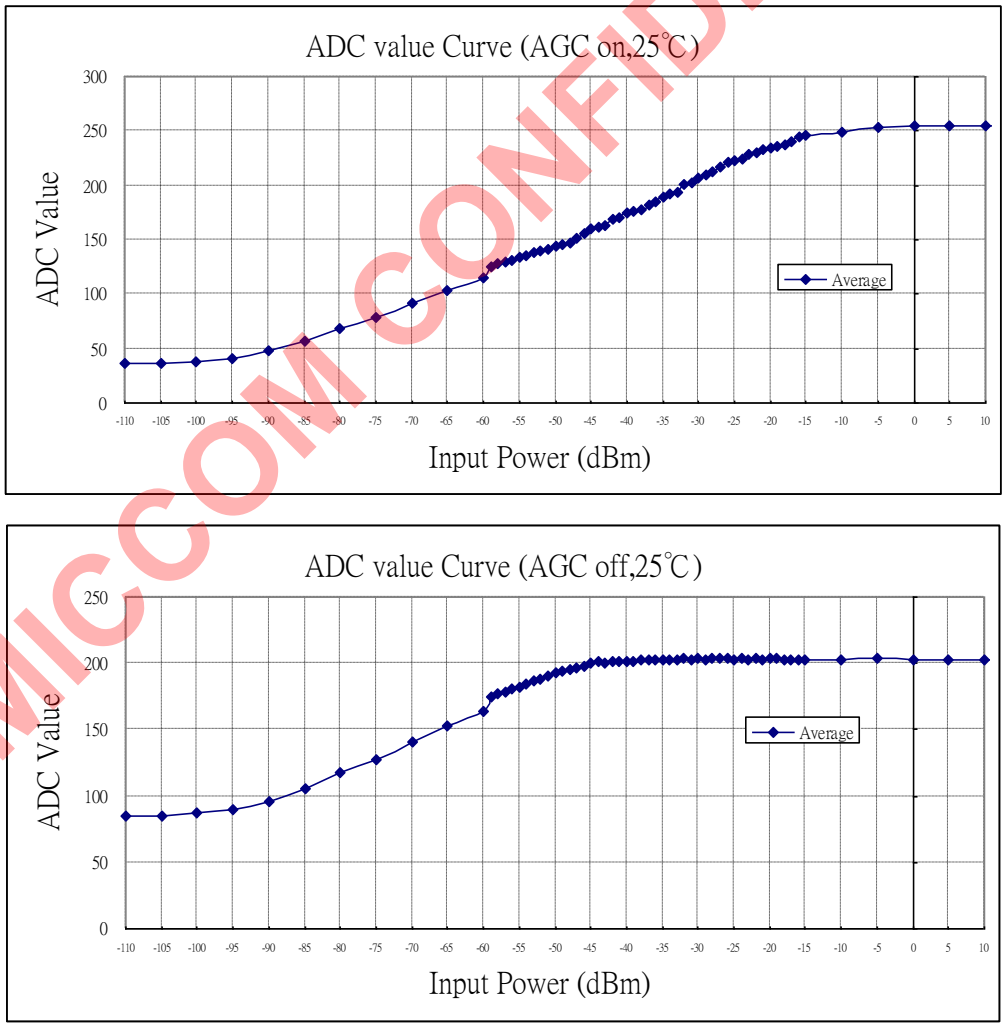

Fig. 5.1 RSSI curve

6. Temperature Curve

A7130 has a thermal sensor inside and users can know the rough temperature of the IC form reading the value of ADC.

Users can get different Temperature ADC scale by setting STMP (Temp voltage ADC reading select) in register [38h] ROMP4. Please read A7130 datasheet.

Customers can calculate T from the formula below roughly.

If STMP =0, Temp = (ADC-148)*2 + room Temp(calibration temp).
If STMP =1, Temp = (ADC-128) + room Temp(calibration temp).

The ADC values of each IC may have slight difference. If customers want to get more accurate Temp ADC value, they should use the ICs with Temp tuning. Please contact Amiccom's FAE for detail about the Temp tuning.

Some measurement data is shown in Fig. 6.1 & Fig. 6.2 below.

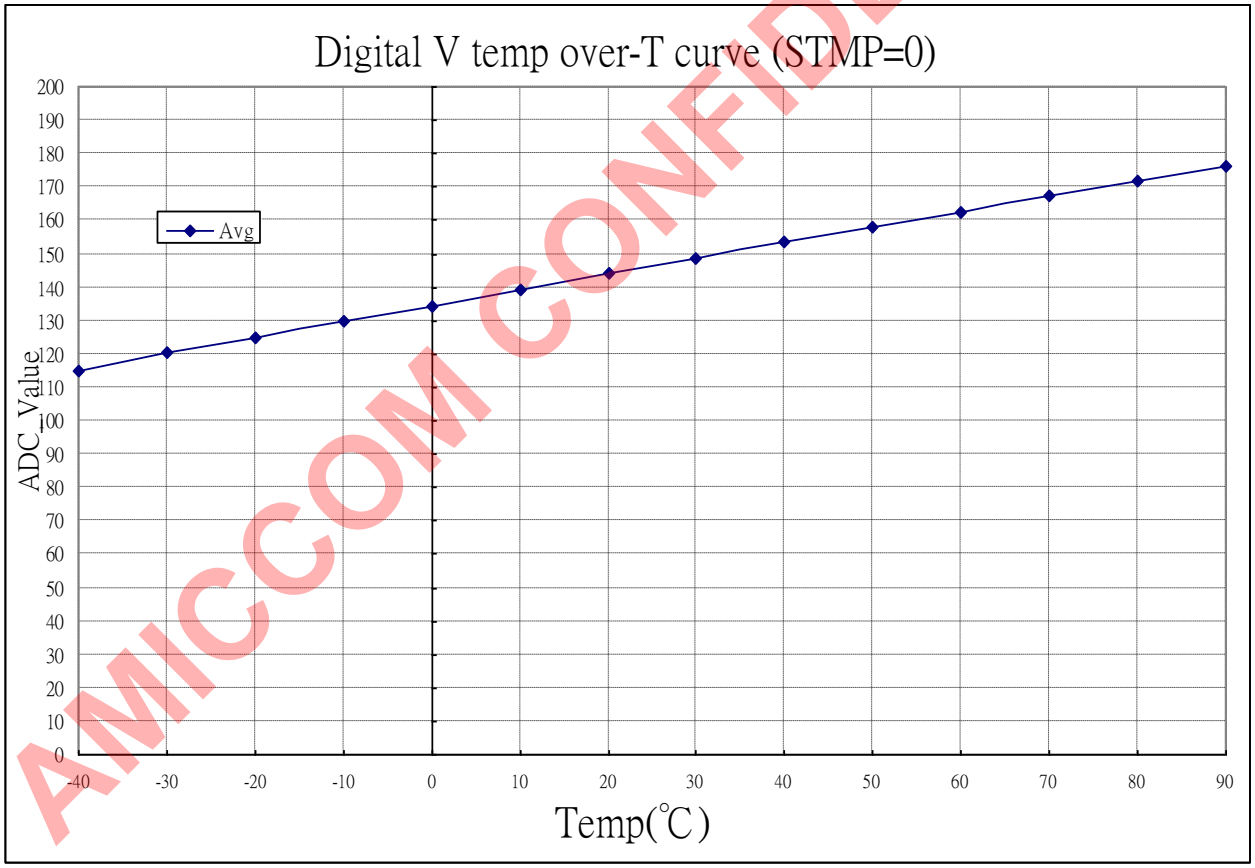

Fig. 6.1 Temperature curve

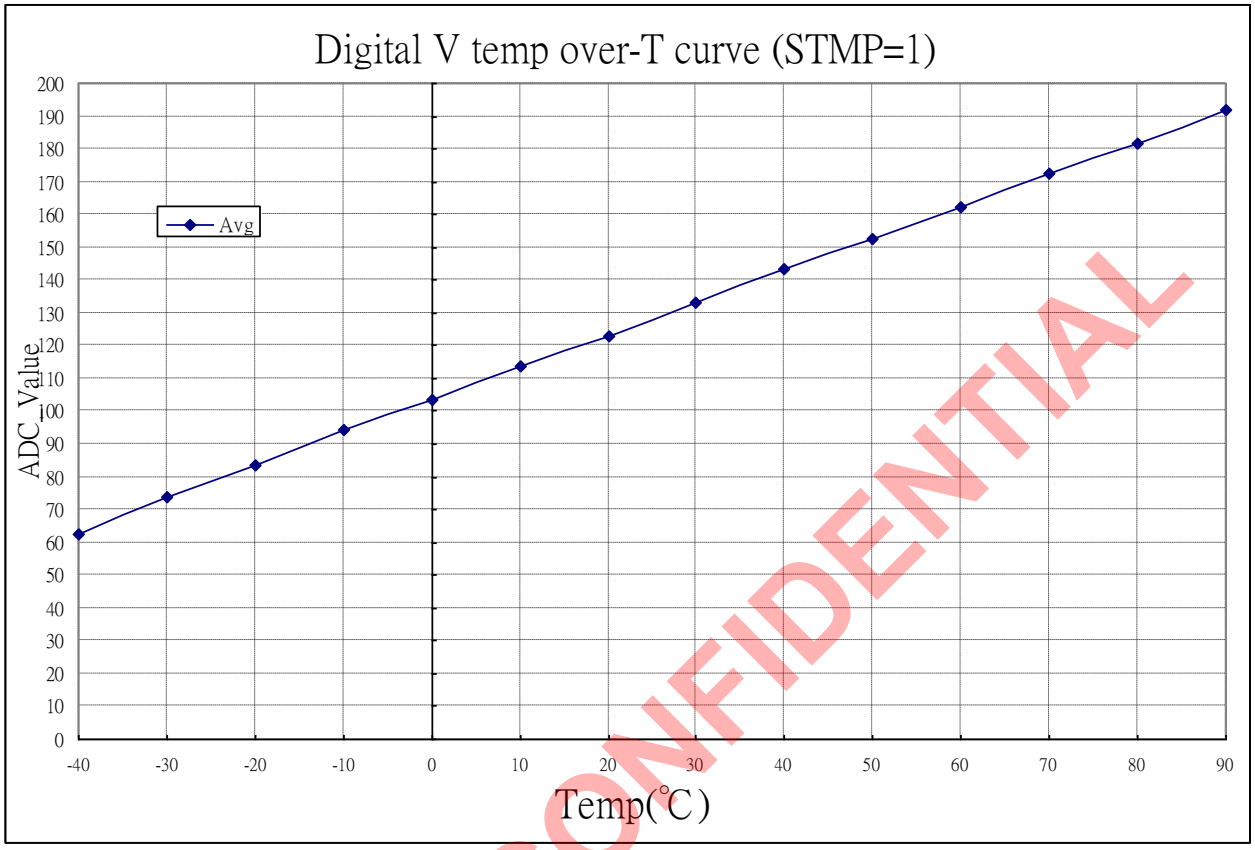

Fig. 6.2 Temperature curve