
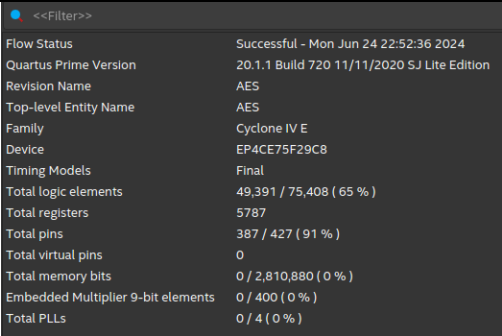



2024 Digital IC Design Homework 5

NAME	洪裕翔		
Student ID	P76124215		
Score = area*timing (ps)	49,391 * 1,221,750 = 60,343,454,250		
Cycle time (ns)	9.5 (ns)		
Simulation Result			
Functional simulation	Completed	Gate-level simulation	Completed
<pre>VSIM 667> run -all # ----- # -- Simulation Start -- # ----- # Correct: 100 ##### ### Pass! ##### # # ** Note: \$finish : /home/pulsar/Workspace/Advanced-Encryption-Standard/tb.v(90) # Time: 1221750 ps Iteration: 0 Instance: /tb # 1 # Break in Module tb at : /home/pulsar/Workspace/Advanced-Encryption-Standard/tb.v line 90</pre> 		 <pre>VSIM 665> run -all # ----- # -- Simulation Start -- # ----- # Correct: 100 ##### ### Pass! ##### # # ** Note: \$finish : /home/pulsar/Workspace/Advanced-Encryption-Standard/tb.v(90) # Time: 1221750 ps Iteration: 0 Instance: /tb # 1 # Break in Module tb at : /home/pulsar/Workspace/Advanced-Encryption-Standard/tb.v line 90</pre> 	
Description of your design			
<p>在本次作業中，我以 round 為單位，將其實作成 module，再將共計 11 個 round（我把第 1 個 AddRoundKey 也視為 1 個 round）逐一實例化並串連在一起。Pipeline 的部分，我的設計則是限制每 1 個 round 的所有行為都只能在 1 個 cycle 做完，這樣的設計雖然會使一個 cycle 的時間較長，但其勝在可以很好地應對本次作業輸入資料的要求（每個 cycle 都輸入一筆新資料），不需要設計額外的等待機制。</p>			