2024 Digital IC Design

Homework 4: Max-Priority Queue

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| NAME | |  | | | | | | |
| Student ID | |  | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | Score | | Gate-level simulation | Score | Clock  width | (ns) | Gate-level simulation time | simulation time (ns) |
| your pre-sim result of test patterns | | | | | your post-sim result of test patterns | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | |  | | | |
| Total memory bit | | | | |  | | | |
| Embedded multiplier 9-bit element | | | | |  | | | |
| your flow summary | | | | | | | | |
| **Description of your design** | | | | | | | | |
|  | | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element) (Total cycle used\*clock width)*