ALU Design **Yang Xie**

1. Abstract

In this project, a simple 8-bit Arithmetic Logic Unit (ALU) schematic design is implemented and verified using Cadence Virtuoso tools. The ALU performs four functionalities: Logical OR, Logical AND, Subtraction and Addition. Optimization techniques such as transistor sizing and gate reduction are performed in order to improve the ALU performance in terms of delay and power consumption. Simulation results show that the worst case propagation delay is 766.9ps and the power consumption is 1.3mW.

2. Introduction

The main motivation of this project is to implement an 8-bit ALU in schematic level using Cadence Virtuoso tool, and apply optimization techniques we learned from the class to improve its performance in terms of delay and power consumption.

ALU is a digital circuit that performs multiple arithmetic and bitwise logical operations based on input integer operands and operation selection signals. It's a basic building block of the central processing unit (CPU) in modern computers. The ALU implemented in this project performs four operations: Logical OR, Logical AND, Subtraction and Addition on two 8-bit input operands A[7:0] and B[7:0] according to the selection of a 2-bit operation selection signal OP[1:0]. The outputs of the ALU is a 8-bit result signal Y[7:0], and four flag signals: carry out flag CO, zero flag Z, negative flag N and overflow flag V. The operation selection specification is shown in Table 1 and the flag specification is given in Table 2.

Table Error! No sequence specified. - **ALU Functionality**

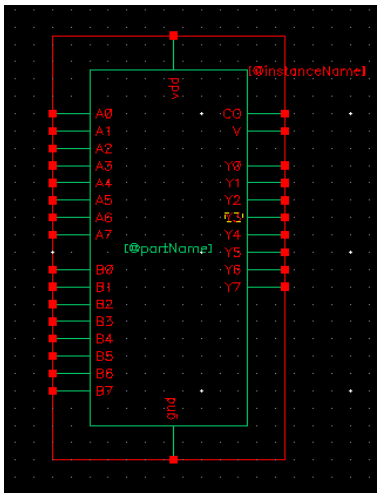
Function	OP[1:0]	Y
Add	00	A + B
Subtract	01	A - B
Logical AND	10	A & B
Logical OR	11	A | B

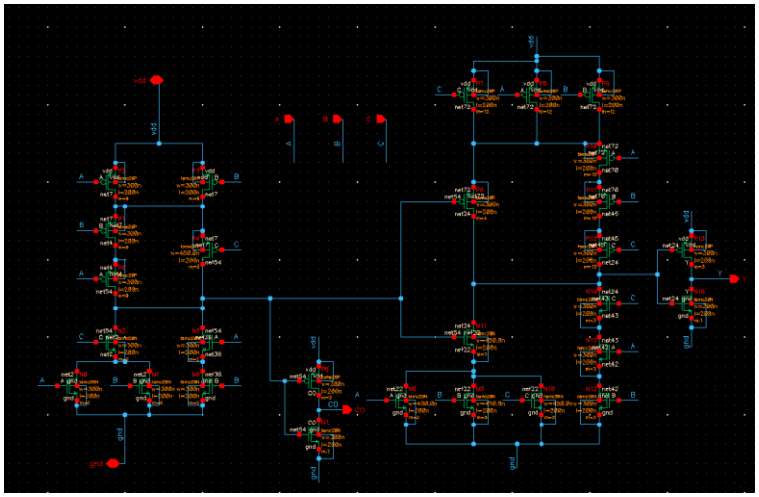
Table Error! No sequence specified. - **Flag Specifications**

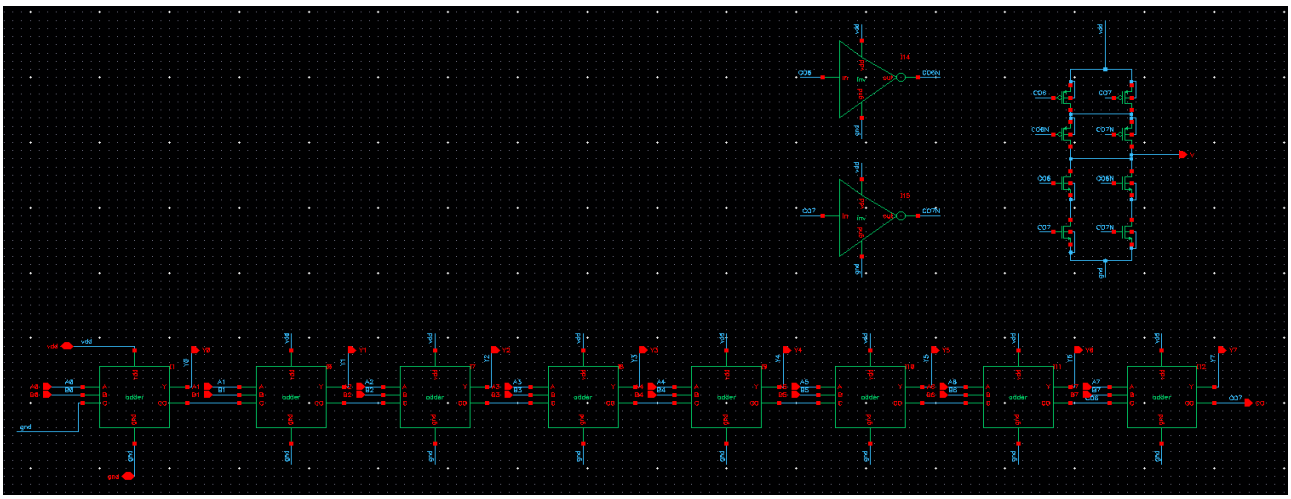
Signal Name	Description
CO	Carry Out should be set when the result of an operation cannot be represented as an 8-bit unsigned number
Z	Zero should be set when the result of an operation is zero
N	Negative should be set when the result of an operation is a negative when interpreted as a signed 8-bit number
V	Overflow should be set when the result of an operation cannot be represented as an 8-bit signed number

Optimization techniques such as transistor sizing and gate reduction are performed in order to improve the ALU performance in terms of delay and power consumption. Simulation results show that the worst case propagation delay is 766.1ps and the power consumption is 1.7mW.

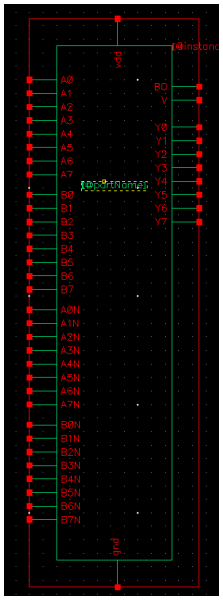
3. Design
3.1 Adder

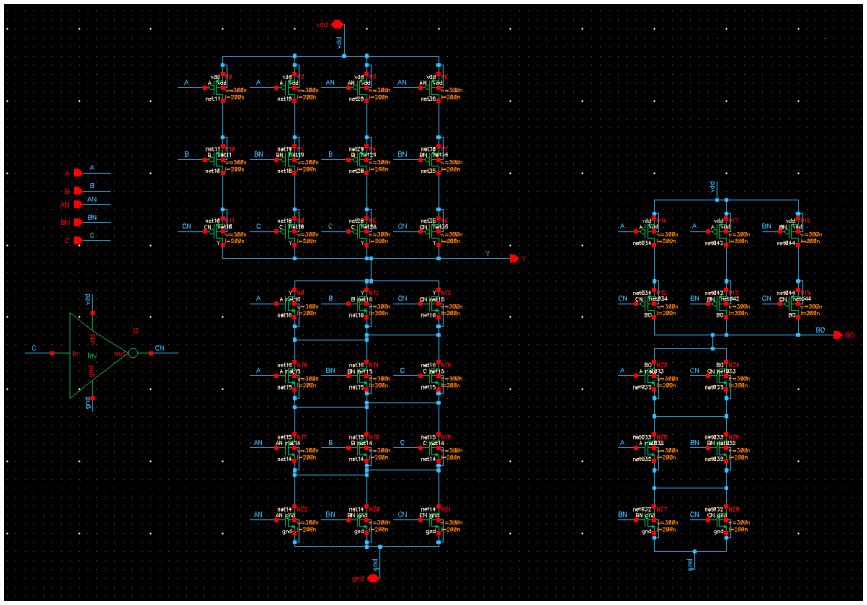


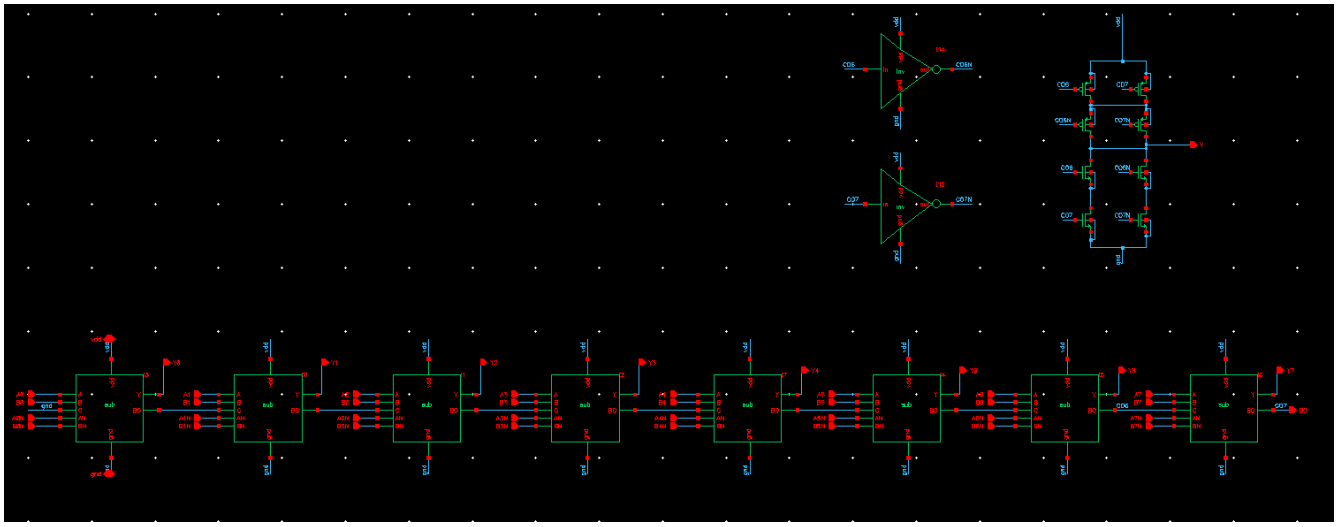




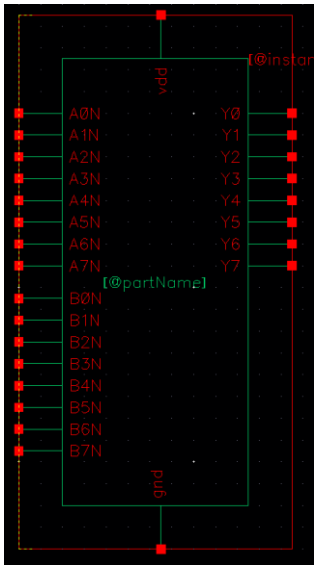
3.2 Subtracter

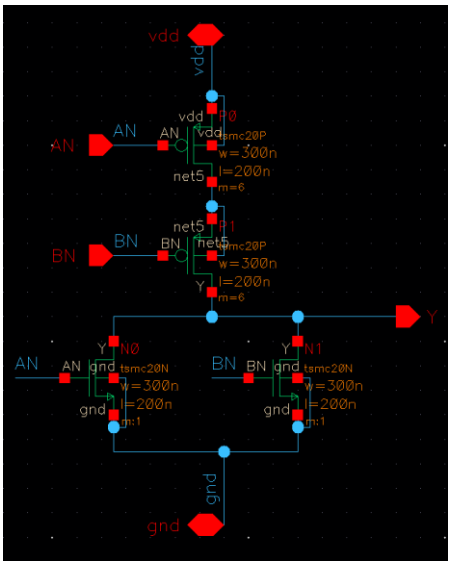


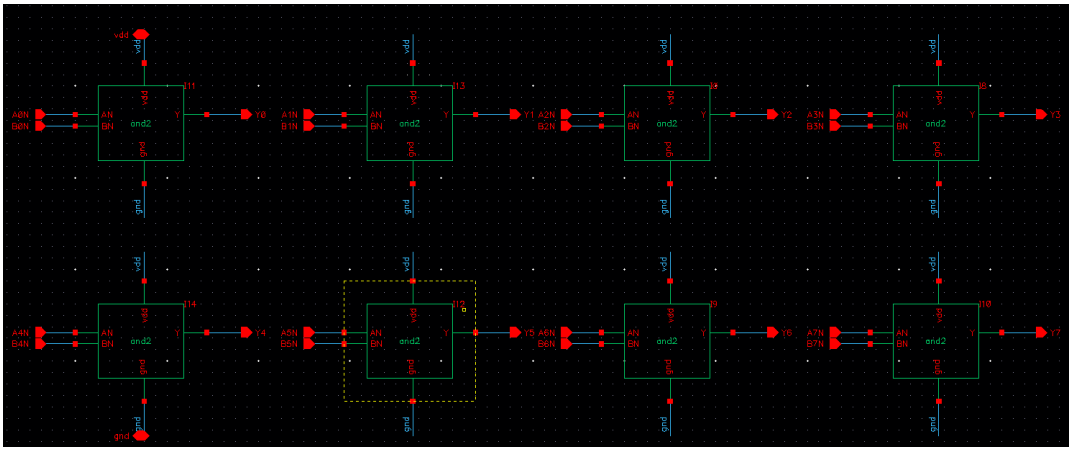




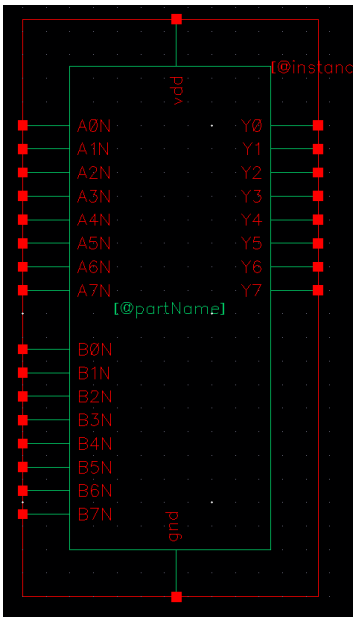
3.3 Logical AND

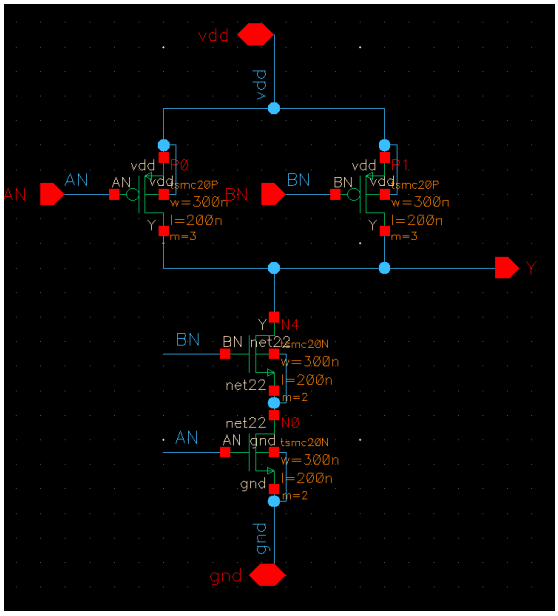


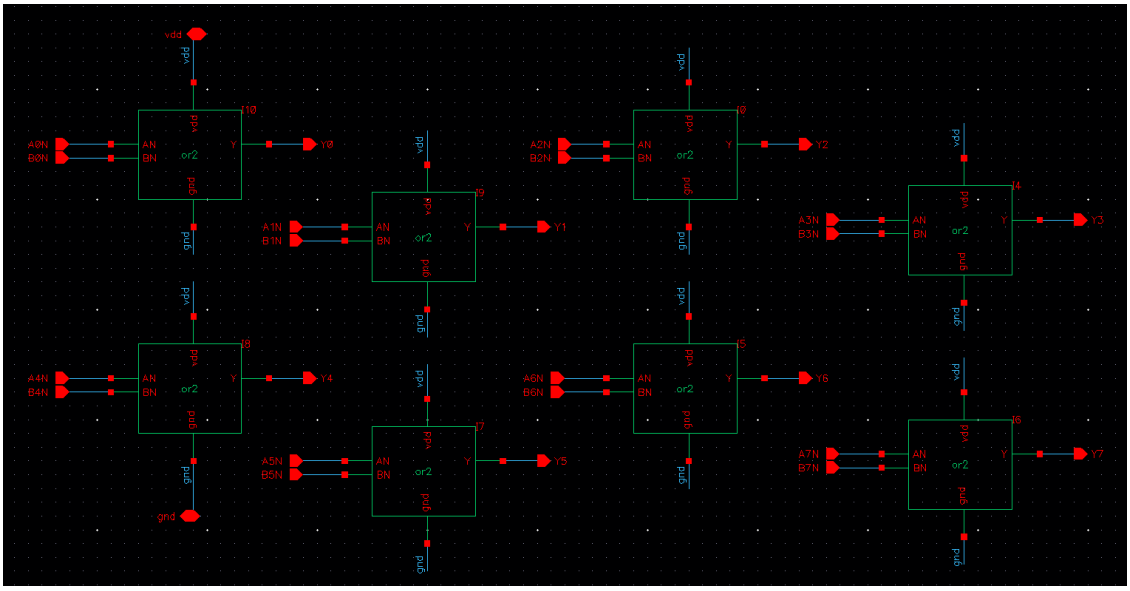




3.4 Logical OR







4. Results and Discussion

4.1 Delay

Output	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	CO	V	Z	N
Delay (ps)	N.A.	491.9	490.7	491.7	493.3	495.8	499.4	572.2	415.4	N.A.	599.6	766.1

4.2 Power