

Doping Effect of Sn on Group III monochalcogenide InSe Nanoflake FET Summary

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Starting from August 2021, the project aims to study the doping effect of group IV metal Tin (Sn) on group III monochalcogenide *InSe*. As *InSe* devices have shown great electron mobility due to its low electron effective mass, the endeavor to improve the electron mobility of *InSe* includes reducing the electron trapping state at the *InSe/SiO₂* interface as well as decreasing the oxidation of *InSe* under room temperature, and increasing the carrier concentration. By inducing a shallow donor Tin (Sn) into *InSe* crystalline structure, I aim to study the expected threshold voltage (V_{th}) shift, improved electron mobility (μ), and the flake thickness dependency. Throughout the study, though improved electron mobility occurs sporadically, electron saturation phenomenon is frequently observed in the majority of the devices. Below is a summary of the hypothetical reasons, solutions, and future plan.

I. INTRODUCTION

As indium selenide represents a promising two-dimensional (2-D) nanomaterial, researchers focusing on 2D monolayer and few-layer *InSe* nanosheets Field-Effect Transistor (FET) have shown that *InSe* devices reach electron mobility at room temperature as $10^3 \frac{cm^2}{V\cdot s}$.¹ In the virgin *InSe* crystal, though there are defects such as interstitial indium (In) atom and selenium (Se) vacancy contributing as shallow donors, the carrier concentration is still low under room temperature.² While electron trapping such as phonon scattering contributes significantly to the hysteresis behavior of the devices, the oxidation layer formed by the exposure of *InSe* to the air greatly affect the electron transport property.³ Therefore, one approach to increase the carrier concentration and improve the trapping defect is by purposely doping external donor impurity to form a ternary element.² It has been showed that Sn is the most efficient donor impurity in *InSe* since it allows the reduction of material's resistivity without affecting the electron mobility.⁴ For this study, *In_{1-x}Sn_xSe* ($x = 1\%, 10\%$) has been chosen, aiming to demonstrate that while enhancement of electron mobility was indeed observed irregularly, no periodical V_{th} shift can be quantified. Additionally, an electron saturation behavior occurs in the majority of the devices regardless of the flake thickness

II. EXPERIMENTAL

The *In_{1-x}Sn_xSe* sample used is the same as used by Paul in their study.³ The compound mixture In, Sn (1%, 10%) and Se is heated under 600°C for 48 hours for synthesis of crystal homogenization.³ Following, the *In_{1-x}Sn_xSe* flakes were fabricated by mechanical exfoliation using Scotch tape. Furthur, the exfoliated flakes were transferred to the degenerately doped Si substrate with 300 nm *SiO₂* dielectric, which

the wafer is cleaned with acetone in sonicator for 10 minutes and rinsed with ethanol and DI water. Ti/Ni contact metal for drain-source were deposited under electron-beam metal deposition after copper grid shadow masks. After the metal deposition, the excessive water molecule absorbed on the *InSe*/substrate interface was removed by annealing the devices in the single-tube furnace under 250°C for 2 hours.

III. RESULTS AND DISCUSSION

The purpose of this study is to observe the improved μ and devices' hysteresis behavior. High electron mobility was occasionally observed in all three flake thickness as shown in figure 1.

As shown in figure 1a, mono-layer, multi-thin layer, and multi-thick layer *In_{1-0.01}Sn_{0.01}Se* flakes all demonstrate moderate μ with the lowest at $13.40 \frac{cm^2}{V\cdot s}$ for multi-thick layer (1c) and highest reaches $86.40 \frac{cm^2}{V\cdot s}$ for mono-layer flake (1b). While devices generally demonstrate little to few hysteresis under vacuum when gate voltage sweeps from -20V-50V were performed, the threshold voltage (V_{th}) doesn't seem to be decreased in thin flakes, however relative low V_{th} is observed to be 9.77V in multi-thick layer flakes in figure 1c. The corresponding IV source-drain curves are shown in figure 2, where devices were measured under vacuum environment performed with V_{ds} sweeping at various constant V_g values.

In figure 2c, Schottky barrier clearly exists in the drain side (negative side). This can be explained by the poor contact between metal and *InSnSe*, where metal failed to appropriately diffuse into the semiconductor, thus creating larger resistance at one end.

It is important to notice that the stated behaviors only occurred sporadically. In most of the devices, μ is largely limited by the electron saturation phenomenon in the source-drain channel. In figure 3b, a "Z-shaped" I-V characteristic curve is observed when performing source-drain voltage vs. drain current. It can be seen that I_{ds} is saturated over the limit $V_{ds} > 0.02V$ and $V_{ds} < -0.02V$, and electrons only flow within the region $-0.02V < V_{ds} < 0.02V$. As the majority of *In_{1-0.01}Sn_{0.01}Se* devices showed electron saturation feature, the flowing region typically is limited within $-0.1V < V_{ds} <$

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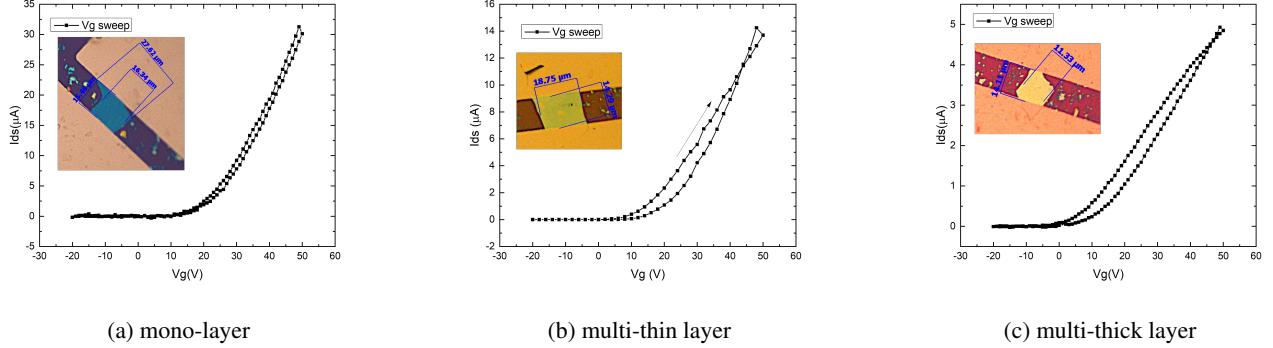


FIG. 1: $In_{1-0.01}Sn_{0.01}Se$ devices gate curve. Devices are bottom gated sweeping from -20V to 50V under vacuum environment at constant drain-source voltage $V_{ds} = 1V$, and the waiting time at each point is 0.5s.

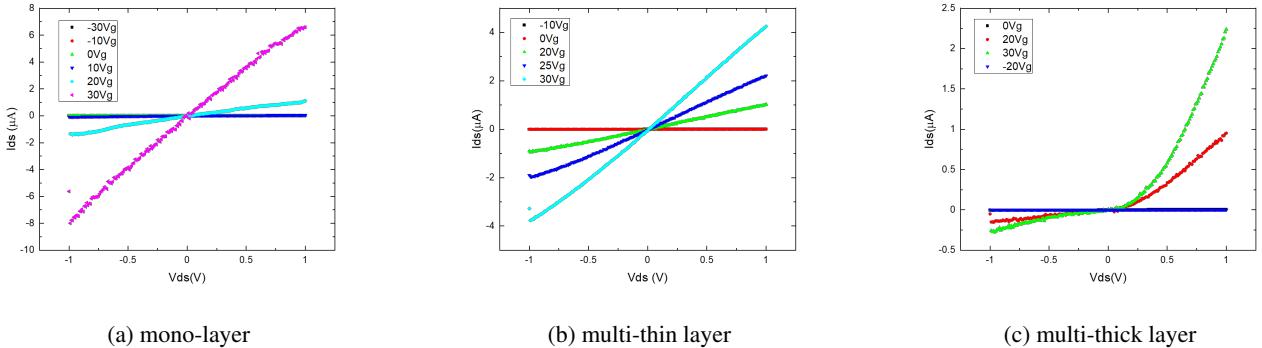


FIG. 2: $In_{1-0.01}Sn_{0.01}Se$ devices IV source-drain curve. Devices are bottom gated sweeping at various fixed V_g and measured under vacuum environment, V_{ds} was swept from -1V to 1V and the waiting time at each point is 0.2s.

0.1V. This, eventually limits μ in the interface thus leading to small I_{ds} .

With $In_{1-0.1}Sn_{0.1}Se$, devices shared the same electron saturation behavior occasionally, but the highest μ reached $180.5 \frac{cm^2}{V\cdot s}$ with a V_{th} at 0.913V (fig4a).

It is important to notice that upon gate voltage sweep is performed almost little to none hysteresis has been demonstrated among all the devices. According to Paul³, the key problem with the mobility of *InSe* devices is that the trap states at the *InSe*/substrate interface and the oxidation of *InSe* in ambient condition hinder the carrier transportation properties. Thus, while annealing and the vacuum environment had greatly reduced the water molecule trapping state, Sn doping impurity additionally provided us a good hysteresis behavior.

IV. THEORIES

A. Crystal Defects

InSe crystal has been realized to have layered structure where In and Se atoms are closely stacked in a sequence of Se-In-In-Se, where the bonding between two adjacent layers is through the weak Van der Waals type.² It has been found

that though some crystal defects such as interstitial In atom or Se vacancy exist in the interstitial state acting like donors in the virgin *InSe*⁵, the carrier concentration is relatively low.² By doping Sn impurity in *InSe*, shallow donor level can be formed in the band diagram, thus reducing the resistivity without affecting μ .⁵ In the study from Hou,² the group showed there are three arrangements that Sn atom can exist in *InSe* lattice site: on the interstitial In site, In lattice site, or on Se lattice site. It was calculated that the bandgap when Sn occupies the In lattice site is the nearest to the measured bandgap, thus postulating that Sn prefers In lattice site to Se site. However, when Sn occupies the interstitial In site, an intermediate band is formed from the creation of *In* – Se pockets upon the incorporation of Sn in crystal lattice.². This intermediate band acts like an annihilation centre for electrons and holes, which does not contribute to carrier concentration enhancement.

This conclusion offers me the insight to re-arrange the post-synthesis atomic structure by annealing the nanoflakes under high temperature for extended hours. The $In_{1-x}Sn_xSe$ crystal we obtained was synthesized under $600^{\circ}C$ for 48 h in the horizontal furnace.³ Knowing this, pre-shadow masking flakes were annealed in the single tube furnace under $500^{\circ}C$ for 3 h, hoping the atomic structure can be re-arranged so that Sn atom could occupy the desired In lattice site. However, the

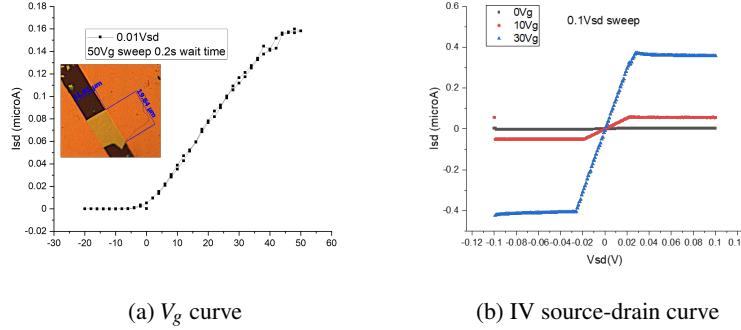


FIG. 3: Electron saturation. Under the same vacuum and room temperature condition, device demonstrates a "z"-shaped IV source-drain curve, where electron only flows within $-0.02\text{V} \leq V_{sd} \leq 0.02\text{V}$ and saturated in the outer region.

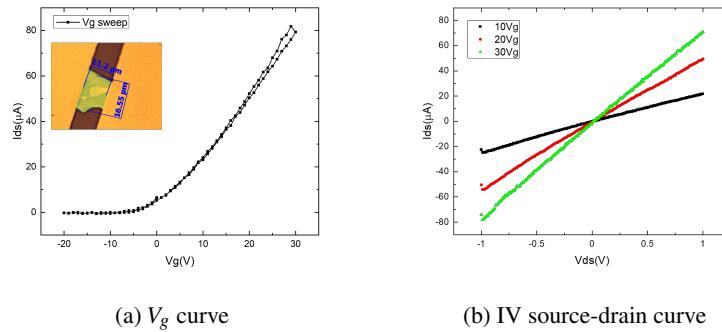


FIG. 4: $\text{In}_{1-0.1}\text{Sn}_{0.1}\text{Se}$ multi-thin layer device. The electron mobility reaches $180.5 \frac{\text{cm}^2}{\text{Vs}}$ with a V_{th} at 0.913V.

annealing method ended up destroying the flakes as shown in figure 5. It can be seen that holes start appearing in the flakes, which delivered an incomplete channel.

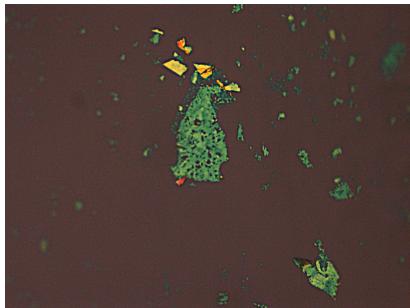


FIG. 5: $\text{In}_{1-0.01}\text{Sn}_{0.01}\text{Se}$ nanoflake upon heat treatment. The original complete flake became porous, which presents physical barrier stymies electron transportation.

V. CONCLUSION

During the study of the doping effect of Sn on group III monochalcogenide InSe , electron saturation phenomenon has been the major roadblock, puzzling me for not knowing the real

cause of this phenomenon. Regardless, occasional high mobility and low threshold voltage have been observed but evidence is not strong enough to conclude that the Sn dopant contributed to the improvement. Additionally, hysteresis-free devices have been occurring in InSe devices. The annealing method is worthy for further investigation since it can possibly re-arrange the lattice layout. Therefore different annealing temperature will be done for various length of time.

VI. REFERENCE

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