**Chung-Hao Huang**

[yyergg@gmail.com](mailto:yyergg@gmail.com)

**OBJECTIVE**

To obtain a full-time position as a staff software engineer

**KEY QUALIFICATIONS**

PhD student in Graduate Institute of Electronics Engineering from National Taiwan University, research interests including SW test automation, game theory, and temporal logic

**TECHNICAL SKILLS**

1. Highly self-motivated, self-learning and independent in problem solving
2. Ability to research, design, deploy and adopt new technology
3. Experience in NP-complete, PSPACE-complete, EXPTIME-complete algorithm implementation with C, C++ or python
4. X86 architecture and UEFI bios basic concept
5. Experience in parser generator (lex, yacc, ply, ANTLR, pyparsing) experience while implementing building tool chain
6. Experience in MVC model developing (Android app, JAVA based MIS system)

**WORK EXPERIENCE**

**Intel Corp.(2011-2012, 2014-present)**

**Various Internship Project**

* Deploying online hardware testing farm.
* Implementing auto SW deploying tool.
* Bios source code debugging.
* Bios build tool implementing.

**EDUCATION**

PhD student in Graduate Institute of Electronics Engineering

National Taiwan University

2008-present

Bachelor in Electronics Engineering

National Taiwan University

2003-2007

**MAJOR GRADUATE SCHOOL PROJECTS**

**SW Testing on Android apps**

* Auto test case generating tool with GUI object identification
* Tool to extract specific behavior which causes anomalies by applying data mining in test results
* Black box memory leakage and code coverage detection with deassamble technique

**Temporal logic and game theory**

* A Game-Theoretic Foundation for the Maximum Software Resilience against Dense Errors. IEEE Transactions on Software Engineering
* An Extension of ATL with Strategy Interaction. ACM Trans. Program. Lang. Syst.
* Model-Checking Iterated Games. TACAS
* A Temporal Logic for the Interaction of Strategies. CONCUR
* Rapid Recovery for Systems with Scarce Faults. GandALF
* Evolving a Test Oracle in Black-Box Testing. FASE
* Temporal Specification Mining for Anomaly Analysis. APLAS

**Logic Synthesis**

* G4LTL-ST: Automatic Generation of PLC Programs. [CAV](http://dblp.uni-trier.de/db/conf/cav/cav2014.html#ChengHRS14)