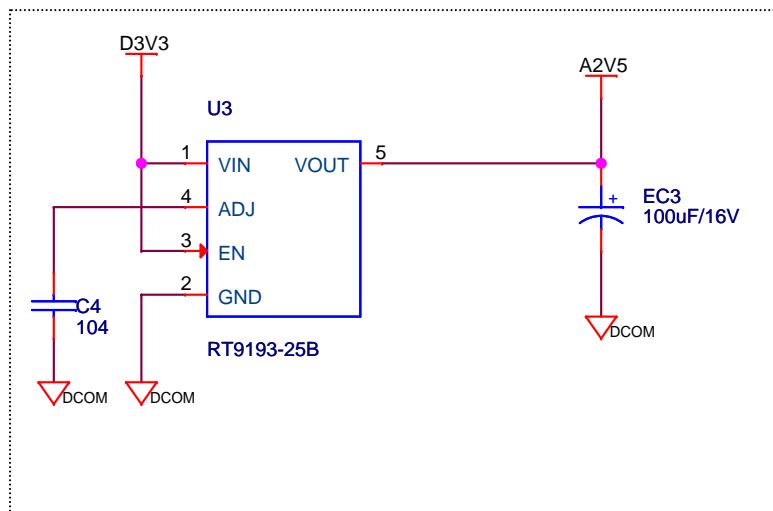
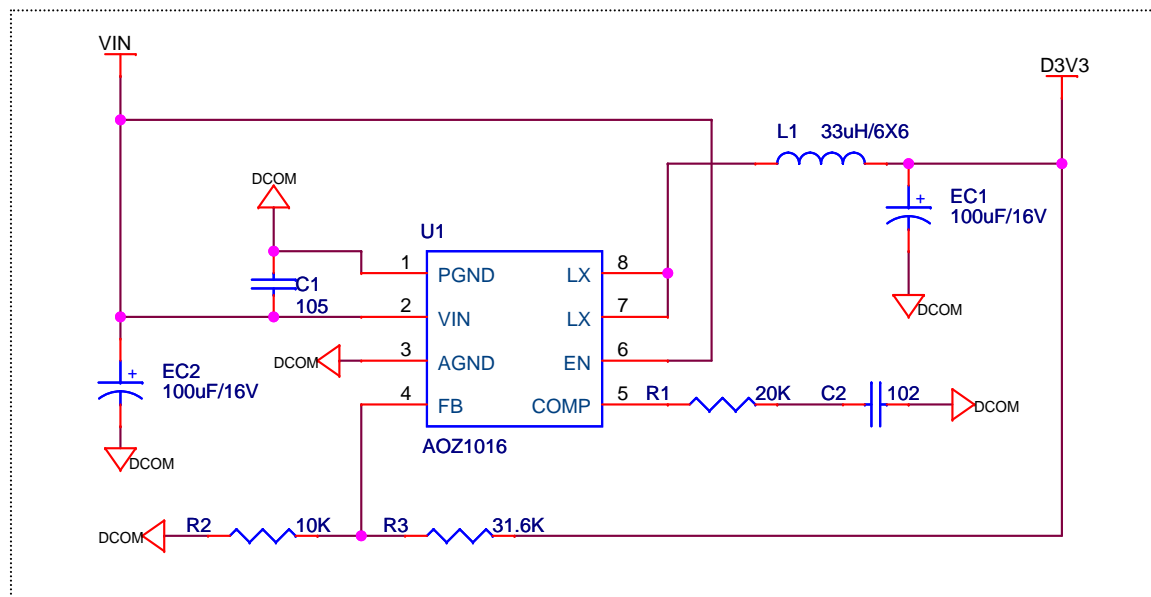


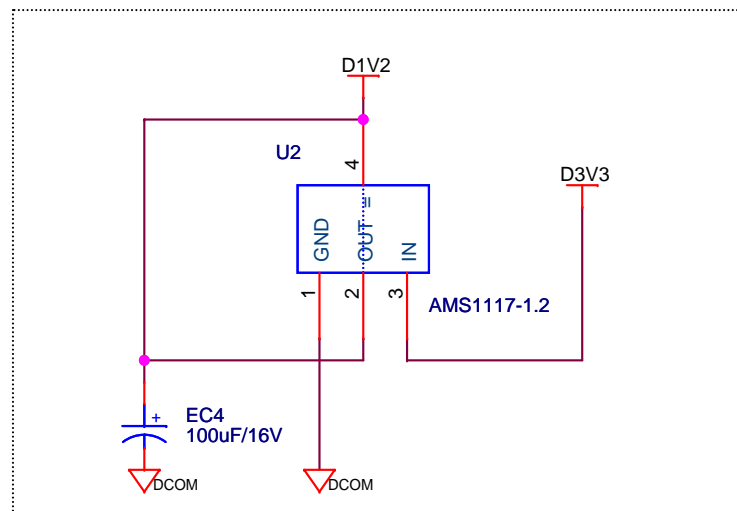
2.5V (LDO)

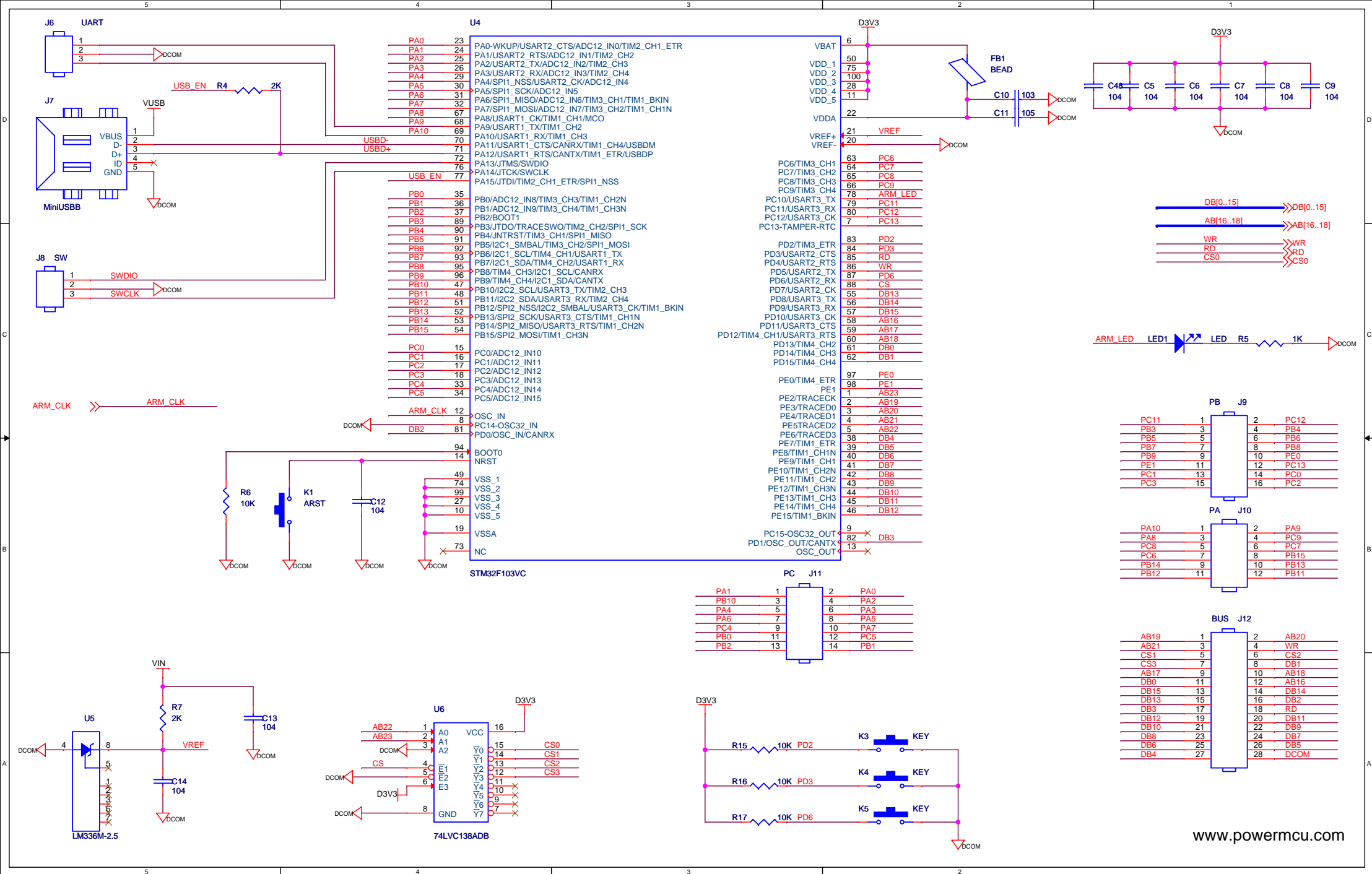


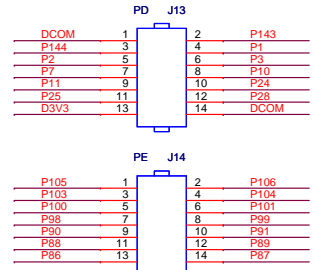
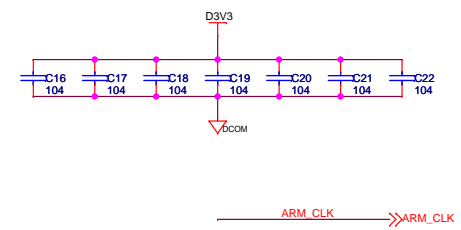
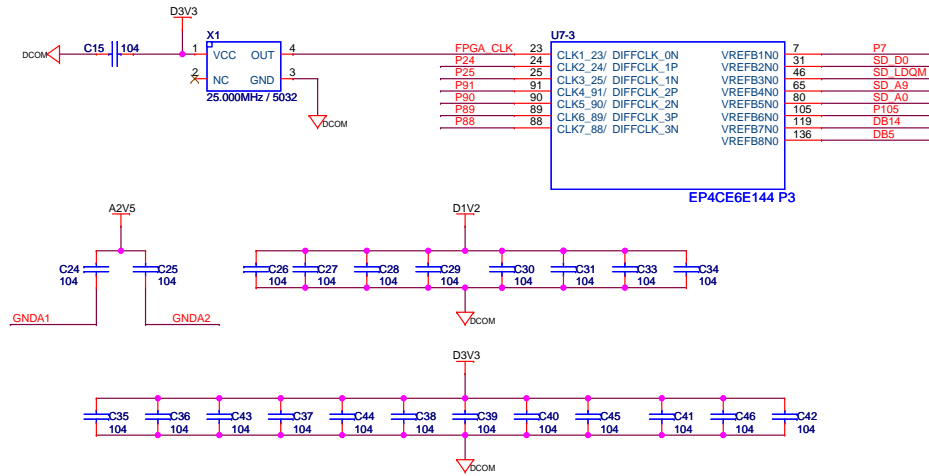
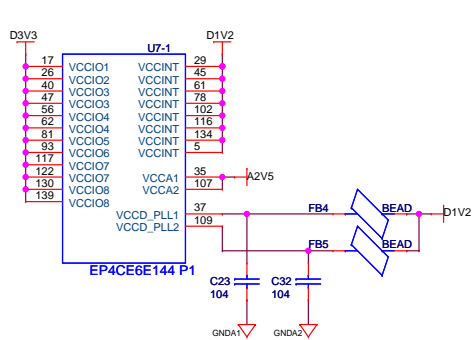
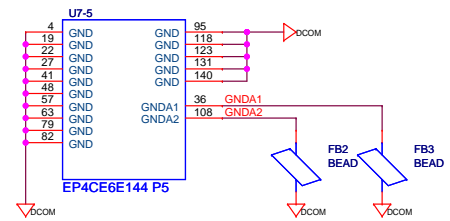
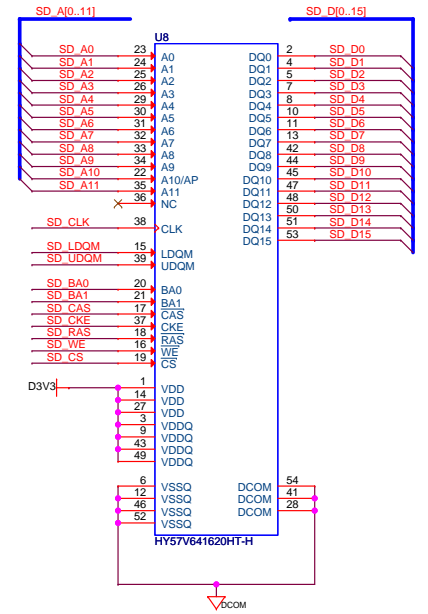
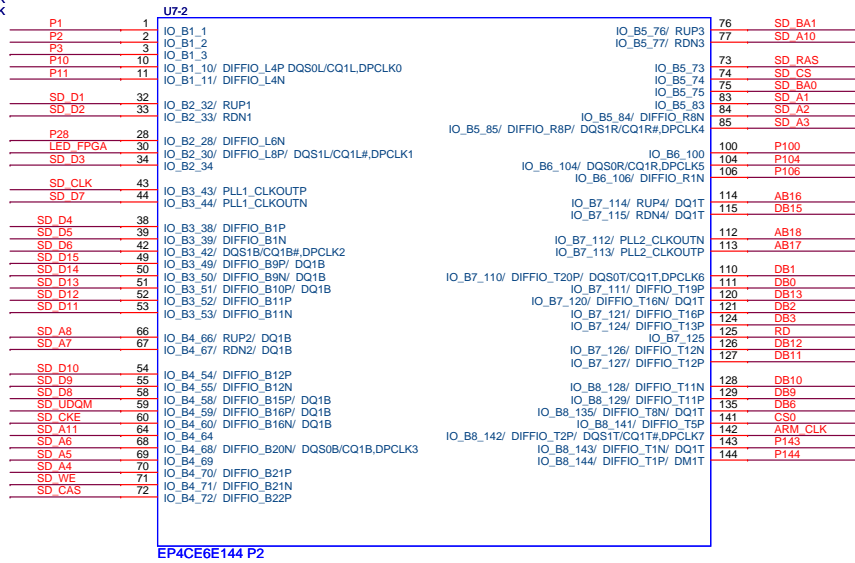
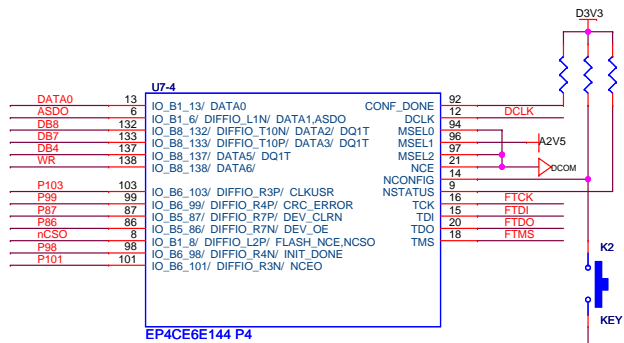
3.3V (BUCK)



1.2V (LDO)







FPGA JTAG

AS CONFIG

