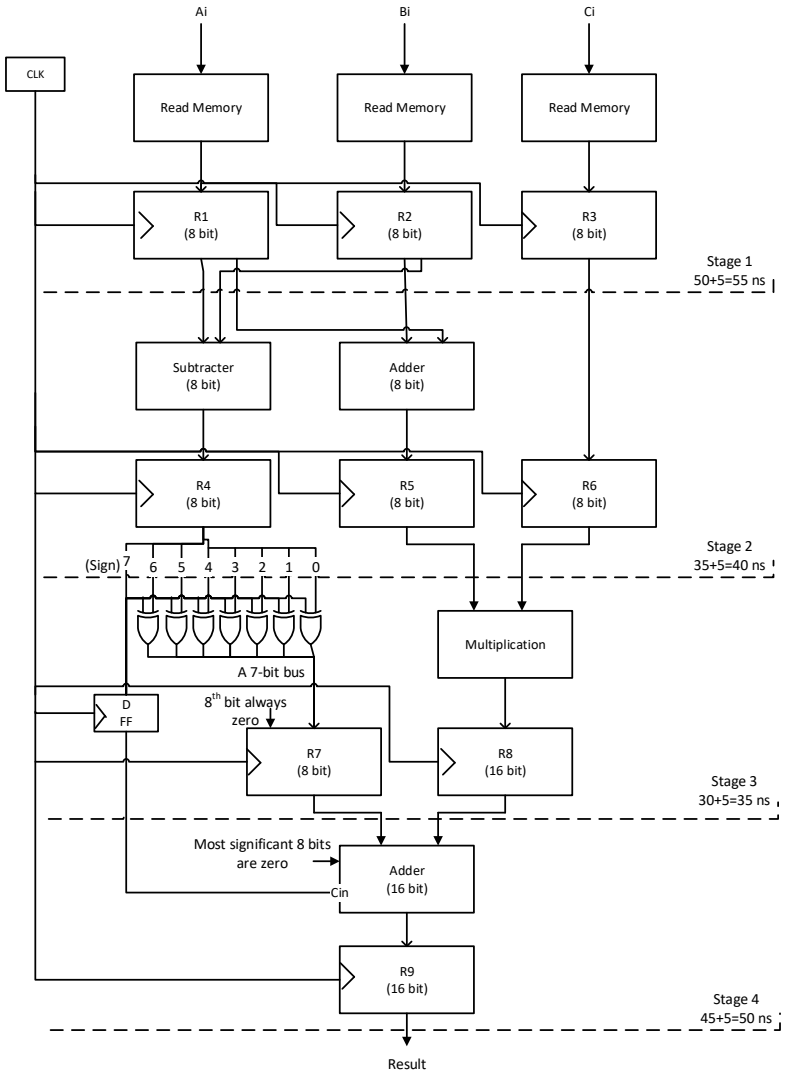
BLG 322E-Computer Architecture
Assignment 1-Solutions

a)



b) The cycle time is determined according to the slowest stage of the pipeline. Accordingly,

$$t_p = \max(\tau_i) + d_r = \tau_M + d_r$$

=50ns+5ns=**55 ns**

c) Total 4 cycles are required to complete the execution of the first task. Also, t_p=55 ns.

$$T(1) = k * t_p$$

=4*55ns=**220 ns**

d) t_n=50(memory access)+35(8-bit adder/subtracter)+30(multiplication)+45(16-bit adder)=160 ns

i. $n \to \infty$, $S = \frac{n * t_n}{(k+n-1) * t_p} = \frac{t_n}{t_p} = \frac{160}{55} = \mathbf{2.91\ ns}$

ii. $n \to 5$, $S = \frac{n * t_n}{(k+n-1) * t_p} = \frac{5 * 160}{(4+5-1) * 160} = \mathbf{1.82\ ns}$

e) The theoratical maximum speedup is equal to the stage number of the pipeline. Accordingly,

S_{max}=**4**