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COMPUTER ARCHITECTURE FINAL EXAM QUESTION 2

Rules:

1. The normal end time of this question is **16:35**. However, because of the 10-minute buffer period, the submission will be closed at **16:45**.
2. **Answer the question on its own sheet** and upload your files during the time allotted for that question, as explained in the file "Exam policies".
   You may write solution to a and b on the same sheet. Solution2ab.pdf
   You may write solution to c and d on the same sheet. Solution2cd.pdf
3. **You may not ask any questions during the exam.** State any assumptions you have to make.
4. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings.
5. Please **show ALL work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT!

QUESTION 2: (35 Points)
A single-CPU computer system has **16Mi bytes** of main memory and cache memory that is used only for data, not for instructions. Prefix Mi represents Megabinary as explained in Chapter 1 of lecture notes.

- Data transfer between main memory and cache is in blocks/frames of **64 bytes**.
- Cache memory can hold **256 frames**.
- The cache control unit uses **2-way** *set associative mapping*.
- For write operations, **Simple Write Back** (SWB) with **Write Allocate** (WA) is used.
- When necessary, **LRU** is used as the replacement algorithm. If a set is empty, assume that frame_0 is older than frame _1.

The CPU runs the piece of pseudocode given on the right.

```
...
B = A;
E = C + D;
F = F + 1;
...
```

- Variable A is read and written to variable B.
- Variables C and D are read, and the result is written to the variable E.
- The variable F is read, incremented, and the result is written to the same variable.
- Each variable is one byte.
- The addresses of the variables are given below (Symbol $ denotes hexadecimal):
  A: $000122, B: $002100, C: $00013C, D: $00013D, E: $00013E, F: $006100
- Initially, none of these variables are in cache memory.

a) Into what fields does the cache control unit divide the main memory address? Give the lengths of the fields. (5 p)

b) Consider the statement `B = A;` that runs first. (10 p)

i) Which set/frames of cache memory does the cache control unit place variables A and B into? Give your answers in decimal. (Example: "**set number: 73, frame: 0**" or "**set number 85, frame: 1**")

ii) How many read misses, read hits, write misses, write hits, and block transfers occur during the run of this statement?

c) Consider the statement `E = C + D;` that runs second. (10 p)

i) Which set/frames of cache memory does the cache control unit place variables C, D, and E into?

ii) How many read misses, read hits, write misses, write hits, and block transfers occur during the run of this statement?

d) Consider the statement `F = F + 1;` that runs third. (10 p)

i) Which set/frames of cache memory does the cache control unit place the variable F into?

ii) How many read misses, read hits, write misses, write hits, and block transfers occur during the run of this statement?