Istanbul Technical University
Department of Computer Engineering

BLG 322E – Computer Architecture
Assignment 3

Due Date: Wednesday, April 21, 2021**,** 23.00.

- Please **write your full name** (first name and last name) **and Student ID** at the top of your solution.
- You may draw the circuits by hand. Please use a ruler and draw neatly.
- Submit your solution as a **PDF file** to Ninova before the deadline (**Wednesday**, April 21, 2021, 23:00). You have one week for this assignment.
- **No late submissions** will be accepted. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official Ninova e-learning system before the deadline. Do not risk leaving your submission to the last few minutes.
- **Consequences of plagiarism:** Assignments have to be done individually. Any cheating will be subject to disciplinary action.
- If you have any questions, you may write to the message board or send an e-mail to **Doğukan Arslan** (arsland15@itu.edu.tr).

QUESTION 1 (20 points):

Suppose that you have a processor connected to an I/O device that can transfer data at an average of **2 MB/s** using interrupt-driven I/O (1 Megabyte = 10^6 Bytes). The interrupt service program transfers two bytes each time. Interrupt processing (including the interrupt service program that transfers two bytes and housekeeping operations) takes **740 ns**. Then, what is the percentage of time used for data transfer?

QUESTION 2 (80 points):

A CPU with an 8-bit data bus has two Interrupt Request inputs (**IRQ1, IRQ2**) and an Interrupt Acknowledge (**INTA**) output. All signals are active at "1". **IRQ1** has higher priority than **IRQ2**.

In this system, there are four interrupt sources (*A1*, *A2*, *B1*, and *B2*). Each interrupt source has an Interrupt Request (**IRQ**) output. These interrupt sources do not have any Interrupt Acknowledgement (**INTA**) inputs, and they are not capable of storing their vector addresses, either.

Priority (precedence) order of the devices: A1 > A2 > B1 > B2.

- A1 and A2: If the CPU receives a request from these devices, it works in autovectored mode and does not read a vector number.
- B1 and B2: These devices are connected over a serial priority controller (daisy chain) to the CPU. If the CPU receives a request from these devices, it works with vectored interrupts and reads the interrupt vector number after the acknowledgment (**INTA**=1) of the interrupt when its Data Acknowledgement (**DACK**) input is "1".

a) Design and draw the system with the CPU, the four I/O devices (A1, A2, B1, B2), and the necessary circuitry. Show the links of the daisy chain as a box. **(50 points)**

b) Assume that devices A2 and B2 assert their interrupt requests at the same time. Show step-by-step all of the signals that are sent in the system until the requests of both devices have been fulfilled. **(30 points)**