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COMPUTER ARCHITECTURE MIDTERM EXAM QUESTION 3

Rules:

1. The normal end time of this question is **19:25**. However, because of the 5-minute buffer period, the submission will be closed at **19:30**.
2. **Answer the question on its own sheet** and upload your files during the time allotted for that question, as explained in the file "Exam policies". Create your files in **PDF format**.
3. **You may not ask any questions during the exam.** State any assumptions you have to make.
4. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings.
5. Please **show ALL work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT!

QUESTION 3: (35 Points)
Note that Parts (a) and (b) below are not related.

a) A system consists of devices that work as interrupt sources and a CPU.

- The CPU has an Interrupt Request input (**IRQ**) and an Interrupt Acknowledgment output (**INTA**). All signals are active at "1". If the CPU receives a request over the IRQ input, it works with vectored interrupts and reads the interrupt vector number after the acknowledgment (INTA=1).
- Each of the interrupt sources has an Interrupt Request output (**IRQ**), an Interrupt Acknowledgment input (**INTA**), and a vector number output (**VN**). After the interrupt has been acknowledged (**INTA=1**), the device outputs its vector number at **VN** and removes its request (**IRQ=0**).

We designed a digital combinational circuit, DC, with four inputs (I_1, I_2, I_3, I_4) and four outputs (O_1, O_2, O_3, O_4) to use as a priority interrupt controller. The logic expressions for the outputs are given below:

$$\boldsymbol{O_1 = I_2 + I_3 + I_4}$$
$$\boldsymbol{O_2 = I_1 \cdot I_2}$$
$$\boldsymbol{O_3 = I_1 \cdot I_3}$$
$$\boldsymbol{O_4 = I_1 \cdot I_4}$$

Hint: The output O_1 of the DC is connected to the IRQ input of the CPU.

i. Since circuit DC is not properly designed, it cannot be used as a priority interrupt controller. Briefly explain the reason. (10 p)

ii. Modify the expressions for the outputs, where necessary. Write the modified expressions. Write which input/output of DC will be connected to which input/output of the CPU or interrupt sources. (10 p)

b) The instruction cycle of a CPU has the following **4 states** (cycles) with the given durations:
1. Instruction fetch: **60 ns**, **2.** Decode and Operand fetch: **50 ns**, **3.** Execution and Operand write: **70 ns**, **4.** Interrupt (housekeeping): **200 ns**.

- In this system, we have two interrupt sources (IS1, IS2). The duration of the interrupt service routine (ISR) including the RTI instruction for each source is 1000ns.
- The interrupts are disabled in the housekeeping operations and enabled again in the RTI instruction. Therefore, an ISR cannot be interrupted.
- The interrupt sources are connected to the CPU using Serial Priority Interrupt Hardware (Daisy Chain). IS1 has higher priority than IS2.

Assume that we start a clock (Clock = 0) when the CPU begins to run the main program.

- At Clock = **50ns**, device **IS2** issues an interrupt request.
- At Clock = **120ns**, device **IS1** issues an interrupt request.

i. State which ISR (the one for IS1 or the one for IS2) will run **first** and when (Clock =?) it will start to run. Show your calculations. (7 p)

ii. State which ISR (the one for IS1 or the one for IS2) will run **second** and when (Clock =?) it will start to run. Show your calculations. (8 p)