Istanbul Technical University
Department of Computer Engineering

BLG 322E – Computer Architecture
Assignment 5

Due Date: Wednesday, May 26, 2021**,** 23:00.

- Please prepare your homework **using a computer**. Points will be taken off for handwritten submissions.
- Please **write your full name** (first name and last name) **and Student ID** at the top of your solution.
- Submit your solution as two **PDF files** to Ninova before the deadline (**Wednesday**, May 26, 2021, 23:00).
- **No late submissions** will be accepted. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official Ninova e-learning system before the deadline. Do not risk leaving your submission to the last few minutes.
- **Consequences of plagiarism:** Assignments have to be done individually. Any cheating will be subject to disciplinary action.
- If you have any questions, you may send an e-mail to **Muhammed Raşit Erol** (erolm15@itu.edu.tr).

QUESTION:

A single-CPU computer system has

- **1Mi bytes** of main memory and
- **4Ki bytes** of cache memory

Data transfer between main memory and cache is in block of **16 bytes**.

Cache memory is used for data operations, not for instructions.

```
For i = 0 to 9
   Read A[i];
   Read B[i];
   Read A[i];
   Read C[i];
End of For
```

The CPU runs piece of pseudocode given at the top right. Only the memory-read instructions are shown in the code.

The starting addresses of the arrays are given below:

A: $0182F
B: $0382F
C: $07827

Each element is **one byte**.

Initially, cache memory is empty.

Answer the following questions based on two different types of mapping techniques:

1) The cache control unit uses 2-way set associative mapping. When necessary, LRU is used as the replacement algorithm. If a set is empty, assume that Frame Zero (first frame in the set) is older than Frame One (second frame in the set).

   a) Which set/frames of cache memory does the cache control unit place arrays A, B, and C into? Give your answers in decimal. (Example: "**set number: 73, frame: 0**" or "**set number 85, frame: 1**")

   b) How many read misses and read hits occur during the run of the given loop? Explain.

2) The cache control unit uses direct mapping

   a) Which frames of cache memory does the cache control unit place arrays A, B, and C into? Give your answers in decimal. (Example: "**frame number: 1**")

   b) How many read misses and read hits occur during the run of the given loop? Explain.