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June 20, 2021
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COMPUTER ARCHITECTURE FINAL EXAM QUESTION 3

Rules:

1. The normal end time of this question is **17:25**. However, because of the 5-minute buffer period, the submission will be closed at **17:30**.
2. **Answer the question on its own sheet** and upload your files during the time allotted for that question, as explained in the file "Exam policies". Create your files in **PDF format**.
3. **You may not ask any questions during the exam.** State any assumptions you have to make.
4. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings.
5. Please **show ALL work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT!

QUESTION 3: (35 Points)
Note that Parts (a) and (b) below are not related.

a) Assume that we use an 8:12 Hamming code. We receive the following bits (d_x represents data bit, p_x represents parity bit):

$d_7\ d_6\ d_5\ d_4\ d_3\ d_2\ d_1\ d_0\ p_3\ p_2\ p_1\ p_0$
`0 1 1 1 1 0 0 1 0 1 0 0`

Given the following syndrome impact table, determine if this received codeword is correct. Explain errors if there are any. (15 p)

Syndrome impact table

	d0	d1	d2	d3	d4	d5	d6	d7	p0	p1	p2	p3
s0	X	X		X	X		X		X			
s1	X		X	X		X	X			X		
s2		X	X	X			X	X			X	
s3					X	X	X	X				X

b) In a symmetric multiprocessor (SMP) system with a shared bus, there are three CPUs (CPU1, CPU2, and CPU3) that have local cache memories. The system does not have a shared L2 cache.
To provide cache coherence, the snoopy **MESI** protocol with **Write Back** (WB) is used.
There is a shared variable **X** in the system.

i. CPU1 attempts to access the variable X and issues the signal *read-with-intent-to-modify* on the bus. What are the states of the corresponding frames in cache memories of the CPUs (CPU1, CPU2, and CPU3), and is the data in main memory valid or not after the operation of CPU1? (5 p)

ii. After CPU1 has completed its operation on X, CPU2 attempts to read the variable X.

1. Which operations are performed and which control messages are sent by the MESI cache controllers during the operation initiated by CPU2? (10 p)
2. What are the states of the corresponding frames in cache memories of the CPUs (CPU1, CPU2, and CPU3), and is the data in main memory valid or not after the operation of CPU2? (5 p)