Istanbul Technical University
Department of Computer Engineering

BLG 322E – Computer Architecture
Assignment 4

Due Date: Sunday, May 10, 2021**,** 23:00.

- Please prepare your homework **using a computer**. Points will be taken off for handwritten submissions.
- Please **write your full name** (first name and last name) **and Student ID** at the top of your solution.
- Submit your solution as two **PDF files** to Ninova before the deadline (**Sunday**, May 10, 2021, 23:00).
- **No late submissions** will be accepted. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official Ninova e-learning system before the deadline. Do not risk leaving your submission to the last few minutes.
- **Consequences of plagiarism:** Assignments have to be done individually. Any cheating will be subject to disciplinary action.
- If you have any questions, you may write to the message board or send an e-mail to **Muhammed Raşit Erol** (erolm15@itu.edu.tr).

QUESTION 1 (100 points):

The instruction cycle of a CPU has the following 5 states (cycles) with the given durations:

1. Instruction Fetch (IF): **40ns**
2. Operand (Register) Read (OR): **20ns**
3. Execution (EX): **40ns**
4. Operand Write (OW): **30ns**
5. Interrupt (IR) (if necessary): **200ns**

Note that the CPU accesses memory in **instruction fetch** and **operand write** cycles but not in the operand read and execution cycles. The CPU enters the interrupt cycle only if an interrupt request is accepted. The housekeeping operations in the interrupt cycle (saving the return address, fetching the vector address, etc.) take **200ns**.

The memory access time and I/O interface access time are **50ns** each.

In this system, there are **four** 3-wire (BR, BG, BGACK) DMACs ($DMAC_1$, $DMAC_2$, $DMAC_3$, and $DMAC_4$.) which are connected to the 68000-like processor over a bus arbiter (see lecture notes slide 5.23).

The order of the precedence is $DMAC_1 > DMAC_2 > DMAC_3 > DMAC_4$.

Given this information, answer the following two questions that are based on two different DMAC types:

1. For all four DMACs, the DMAC type is **flow-through** (explicit) (i.e., data passes through the DMAC). $DMAC_1$ and $DMAC_4$ are in **cycle-stealing** mode, and $DMAC_2$ and $DMAC_3$ are in **burst** mode. Assume that we start a clock (Clock = 0) when the CPU begins to run a program and all DMACs attempt to start transfer for 5 words when Clock = **20ns**.

   Draw a table that shows the time (1st column), the activity of the CPU (2nd column) and the activities of the DMACs in the next four columns. Answer the following questions:

   a. When (Clock = ?) will $DMAC_1$ complete the transfer of the third word? Why? (10 points)
   b. When (Clock = ?) will the CPU complete the first instruction cycle? Why? (15 points)
   c. When (Clock = ?) will $DMAC_4$ complete the transfer of all 5 words? Why? (15 points)

2. In this system, there is also a single interrupt source (**IS**). For all four DMACs, the DMAC type is **fly-by** (implicit) (i.e., data does not pass through the DMAC). $DMAC_1$ is in **cycle-stealing** mode, and $DMAC_2$, $DMAC_3$ and $DMAC_4$ are in **burst** mode. The I/O interface is always ready to transfer data. Assume that and we start a clock (Clock = 0) when the CPU begins to run a program and all DMACs attempt to start transfer for 5 words when Clock = **20ns**. Also, at Clock = **10ns**, the device IS sends an interrupt request.

   Draw a table that shows the time (1st column), the activity of the CPU (2nd column) and the activities of the DMACs in the next four columns. Answer the following questions:

   a. When (Clock = ?) will $DMAC_1$ complete the transfer of all 5 words? Why? (30 points)
   b. When (Clock = ?) will the ISR (Interrupt Service Routine) of the IS start to run? Why? (30 points)