3D scanning by means of dual-projector structured light illumination

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ABSTRACT

This document shows the desired format and appearance of a manuscript prepared for the Proceedings of the SPIE. It contains general formatting instructions and hints about how to use LaTeX. The LaTeX source file that produced this document, `article.tex` (Version 3.3), provides a template, used in conjunction with `spie.cls` (Version 3.3).

Keywords: Manuscript format, template, SPIE Proceedings, LaTeX

1. INTRODUCTION

Structured light illumination

2. HDMI

HDMI is the abbreviation of High-Definition Multimedia Interface, it is one of the most popular display interfaces. The newest release, HDMI Version 2.1 supports up to $10K$ video at $120Hz$. A standard HDMI connector has 19 pins as listed in Table 1.

Data channel 2, 1, 0 are mainly used to transfer red, green and blue components of the video respectively. The HDMI does not only transfer video data, but also some auxiliary data, for example audio data, packet header. The auxiliary data, video data as well as some control signals are encoded in data channel 2, 1, 0 and then digitally transmitted in serial. In between any two adjacent video periods, one or more data island period and control period are inserted. There are six important control signals, HSYNC indicates the beginning and end of a row in a frame of the video, VSYNC indicates the beginning and end of a frame, CTL0 CTL3 indicate the data type of the following data period. The three data channels are transmitted through a differential signaling technology called Transition-Minimized Differential Signaling (TMDS) to reduce the impact of electromagnatic interference and enable high clock skew tolerance. Another common application of TMDS is in the Digital Visual

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Table 1: HDMI pinout

PIN	DATA
Data2+, Data2 Shield, Data2-	red pixel component, CTL2, CTL3 and auxiliary data
Data1+, Data1 Shield, Data1-	green pixel component, CTL0, CTL1 and auxiliary data
Data0+, Data0 Shield, Data0-	blue pixel component, HSYNC, VSYNC and auxiliary data
Clock+, Clock Shield, Clock-	pixel clock
SCL, SDA	DDC channel, the source reads the EDID from the sink
CEC	data or commands from remote control
Reserved/HEAC+	reserved for v1.3 and before, Ethernet and audio since v1.4
HOT PLUG DETECT/HEAC-	indicate the hot plug or paired with HEAC+
+5V, Ground	power from external or HDMI source, ground

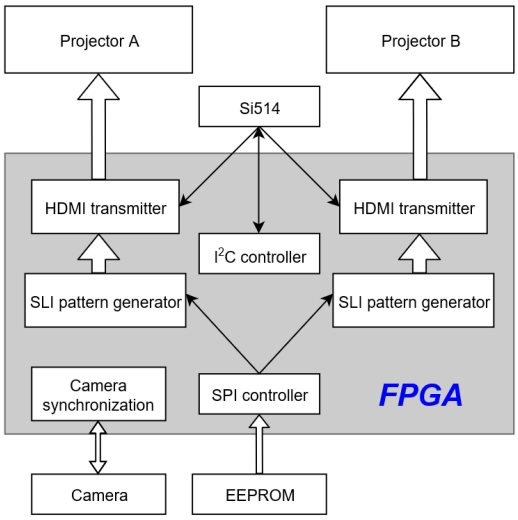

Figure 1: System diagram

Interface (DVI).
The 5 volts power signal is provided by the HDMI source or an external source. After the HDMI sink receives an 5 volts signal at the corresponding pin, it immediately asserts the pin Hot Plug Detect. Once the HDMI source detects the presence of a sink by the assertion of the pin Hot Plug Detect, it sends an I^2C-based command of a read request to the sink. The pins SCL and SDA compose the display data channel (DDC) via which the Extended Display Identification Data (EDID) is read by the HDMI source from the sink as the response to the read request. The EDID is usually 128 or 256 bytes long, it contains various information related to the features of display system, including but not limited to, manufacturer ID, serial number, week and year of manufacture, screen size, supported timing, etc.
The pin CEC is used for high-level CEC stands for Consumer Electronics Control, it is also a one-wire bus protocol, the implementation of CEC is optional, because not all the HDMI devices support this feature. Since HDMI 1.4, the previously reserved pin has become the HDMI Ethernet and Audio Returen Channel (HEAC),

3. SYSTEM IMPLEMENTATION BASED ON FPGA

The system diagram is shown in Figure 1. The system generates structured light patterns at the resolution of $800x600$, the refresh rate of $120Hz$. According to the document provided by VESA,[1] the HDMI timing should be set as Table 2.

Table 2: HDMI timing of $800x600@120Hz$

Pixel Clock	73.250MHz
Hor. Front Porch	48 pixels
Hor. Sync Time	32 pixels
Hor. Back Porch	80 pixels

Ver. Front Porch	3 lines
Ver. Sync Time	4 lines
Ver. Back Porch	29 lines

We utilize an I^2C programmable oscillator Si514 to generate the unusual 73.25MHz pixel clock.

LUT used to adjust the linearty of the projector

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REFERENCES

1. Video Electronics Standards Association, *VESA and industry standards and guidelines for computer display monitor timing* (May 2007). Version 1.0.