3D scanning by means of dual-projector structured light illumination

Daniel L. Lau[a] and Ying Yu[a]

[a]University of Kentucky, Address, Lexington, US;

ABSTRACT

This document shows the desired format and appearance of a manuscript prepared for the Proceedings of the SPIE. It contains general formatting instructions and hints about how to use LaTeX. The LaTeX source file that produced this document, `article.tex` (Version 3.3), provides a template, used in conjunction with `spie.cls` (Version 3.3).

Keywords: Manuscript format, template, SPIE Proceedings, LaTeX

1. INTRODUCTION

Structured light illumination

2. HDMI OVERVIEW

HDMI is the abbreviation of High-Definition Multimedia Interface, it is one of the most popular display interfaces. The newest release, HDMI Version 2.1 supports up to $10K$ video at $120Hz$. A standard HDMI connector has 19 pins as listed in Table 1.

Data channel 2, 1, 0 are mainly used to transfer red, green and blue components of the video respectively. The HDMI does not only transfer video data, but also some auxiliary data, for example audio data, packet header. The auxiliary data, video data as well as some control signals are encoded in data channel 2, 1, 0 and then digitally transmitted in serial. In between any two adjacent video periods, one or more data island period and control period are inserted. There are six important control signals, HSYNC indicates the beginning and end of a row in a frame of the video, VSYNC indicates the beginning and end of a frame, CTL0 CTL3 indicate the data type of the following data period. The three data channels are transmitted through a differential signaling technology called Transition-Minimized Differential Signaling (TMDS) to reduce the impact of electromagnetic interference and enable high clock skew tolerance. Another common application of TMDS is in the Digital Visual Interface (DVI).
The 5 volts power signal is provided by the HDMI source or an external source. After the HDMI sink receives an

Further author information: (Send correspondence to A.A.A.)
A.A.A.: E-mail: aaa@tbk2.edu, Telephone: 1 505 123 1234
B.B.A.: E-mail: bba@cmp.com, Telephone: +33 (0)1 98 76 54 32

PIN	DATA
Data2+, Data2 Shield, Data2-	red pixel component, CTL2, CTL3 and auxiliary data
Data1+, Data1 Shield, Data1-	green pixel component, CTL0, CTL1 and auxiliary data
Data0+, Data0 Shield, Data0-	blue pixel component, HSYNC, VSYNC and auxiliary data
Clock+, Clock Shield, Clock-	pixel clock
SCL, SDA	DDC channel, the source reads the EDID from the sink
CEC	data or commands from remote control
Reserved/HEAC+	reserved for v1.3 and before, Ethernet and audio since v1.4
HOT PLUG DETECT/HEAC-	indicate the hot plug or paired with HEAC+
+5V, Ground	power from external or HDMI source, ground

Table 1: HDMI pinout

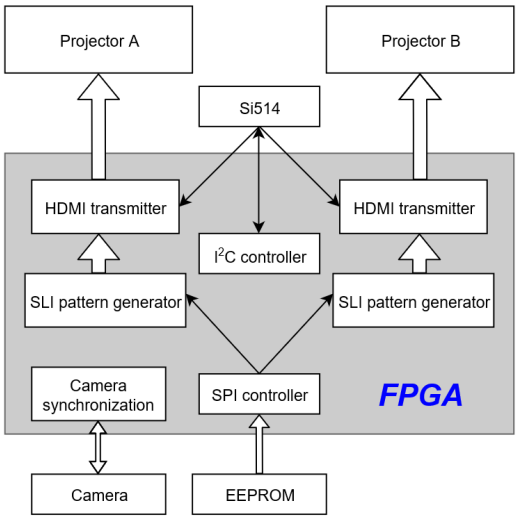

Figure 1: System diagram

5 volts signal at the corresponding pin, it immediately asserts the pin Hot Plug Detect. Once the HDMI source detects the presence of a sink by the assertion of the pin Hot Plug Detect, it sends an I^2C-based command of a read request to the sink. The pins SCL and SDA compose the display data channel (DDC) via which the Extended Display Identification Data (EDID) is read by the HDMI source from the sink as the response to the read request. The EDID is usually 128 or 256 bytes long, it contains various information related to the features of display system, including but not limited to, manufacturer ID, serial number, week and year of manufacture, screen size, supported timing, etc.
The pin CEC is used to add some advanced functionalities for the HDMI systems. Usually it is a remote control that issues different high-level commands to the devices connected by HDMI cables. CEC stands for Consumer Electronics Control, it is also a one-wire bus protocol, the implementation of CEC is optional, because not all the HDMI devices support this feature. Since HDMI 1.4, the previously reserved pin has become the HDMI Ethernet and Audio Returen Channel (HEAC). While it is in audio return channel mode, only the HEAC+ line is used to transmit audio data; in HDMI Ethernet channel mode, the HEAC+ line pairs up with the HEAC- line as a differential signal to establish a high speed Ethernet communication.

3. SYSTEM IMPLEMENTATION BASED ON FPGA

Our FPGA-based dual-projector Structured Light Illumination (SLI) system generates two synchronized SLI patterns which are then fed to two projectors via HDMI. Meanwhile, the projectors and the camera need to be synchronized to ensure that the camera images are taken at the right timing. The system diagram is shown in Figure 1.

The two SLI pattern generators output two synchronized phase-shifting fringe patterns which are later encoded into TMDS data streams by the HDMI transmitters and eventually move to projectors. The camera synchronization module controls the timing of the camera trigger signal, it detects the end of the camera's exposure time and makes sure that during the whole camera's exposure time, there is no different pattern projected and every unique phase-shifting fringe pattern is pictured sequentially by the camera. The projector in our SLI system operates at the resolution of $800x600$ and the refresh rate of $120Hz$. According to the document from VESA,[1] the HDMI timing should be set as Table 2 lists.

To obtain the uncommon 73.25MHz pixel clock, we utilize a programmable oscillator Si514. By configuring the internal registers through I^2C bus, Si514 can generate any frequency from 100kHz to 250MHz with a tuning resolution of 0.026 ppb. Therefore, an I^2C master controller was incorporated into the system. One last module in the system is a lookup table (LUT) that is used to linearize the output of the projector. Ideally, the input

Pixel Clock	73.250MHz
Hor. Front Porch	48 pixels
Hor. Sync Time	32 pixels
Hor. Back Porch	80 pixels

Ver. Front Porch	3 lines
Ver. Sync Time	4 lines
Ver. Back Porch	29 lines

Table 2: HDMI timing of $800x600@120Hz$

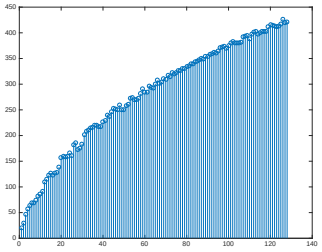

Figure 2: output without LUT

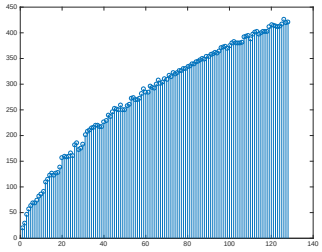

Figure 3: output with LUT

digital values of the projector is proportional to the light intensity at the output side of the projector. The light intensity is measured by reading the pixel value of the photo taken by the camera. However, in practice, they are non-linear for most of the times due to gamma distortion. Introducing a LUT to compensate the gamma distortion is an effective way to address this problem of non-linearity, as shown in the Figure 2 and Figure 3. This LUT can be hard-coded into the configuration file of the FPGA, but the drawback is that once the lookup table changes, the FPGA configuration file has to be changed. It is quite inconvenient especially when the system needs to be often applied to a different projector. We devise a method that the user stores the LUT in an EEPROM which can be erased and written by any computer via serial port or USB, and the SPI master module in the FPGA reads the EEPROM every time the system is powered on. With this approach, users can load a new LUT much simpler and faster.

Our tested system looks as Figure 3 shows.

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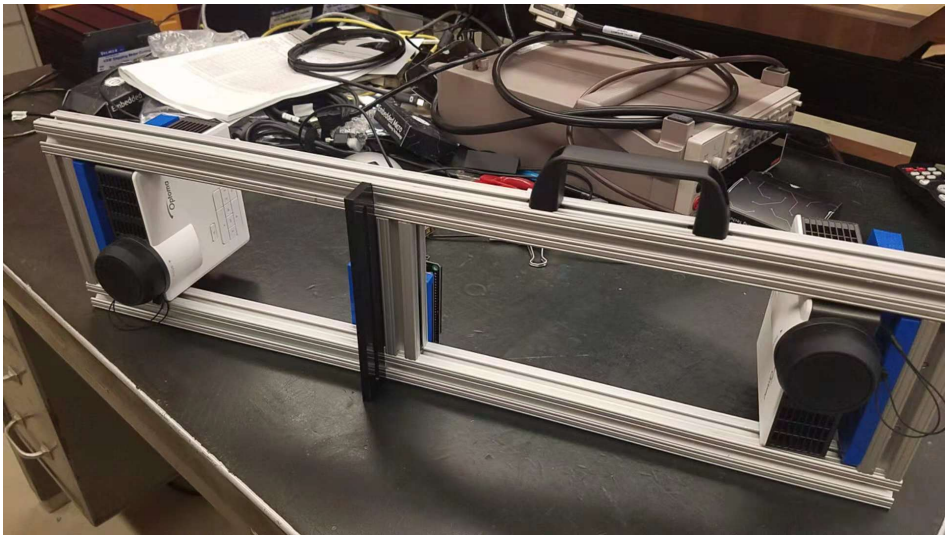

Figure 4: the dual-projector SLI system

REFERENCES

1. Video Electronics Standards Association, *VESA and industry standards and guidelines for computer display monitor timing* (May 2007). Version 1.0.