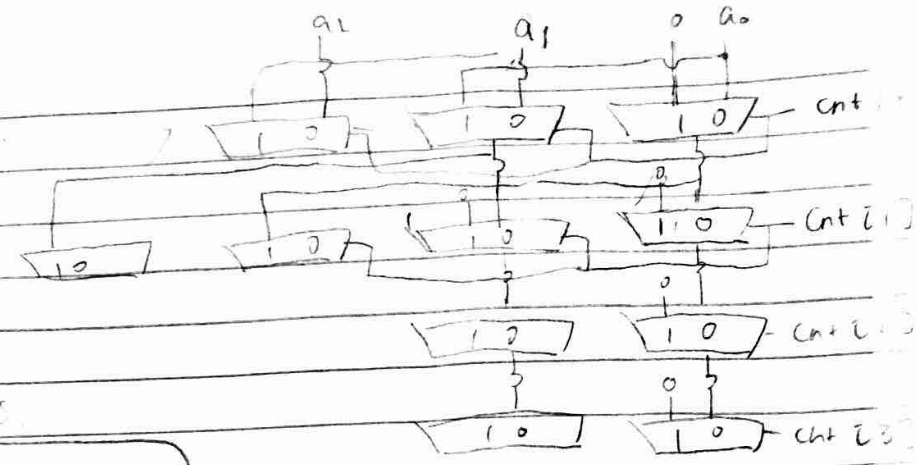
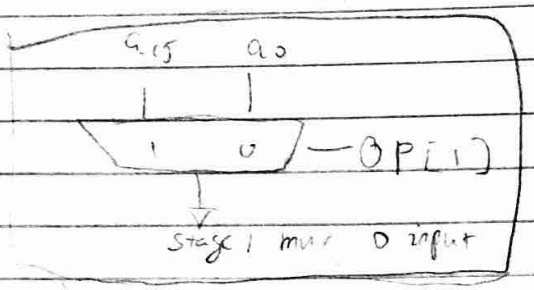
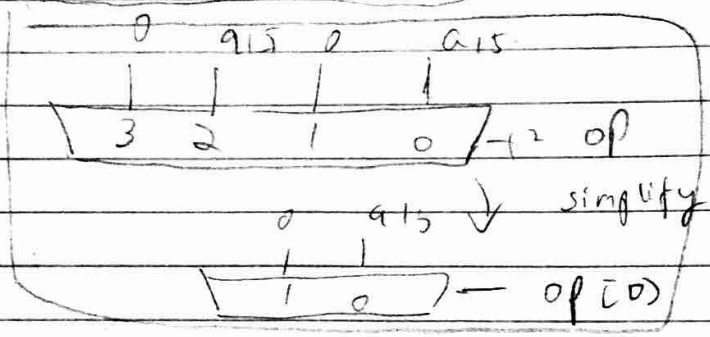
4 stages cnt[0] cnt[1] cnt[2] cnt[3]
Shift amount: 1 2 4 8

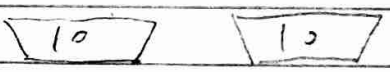


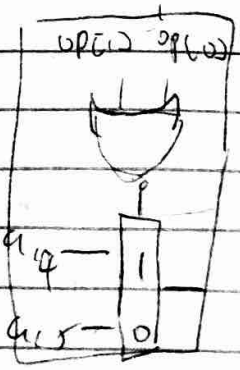
S=0 1
in A in B





00 Rot L
01 SL
10 ASR
11 SR

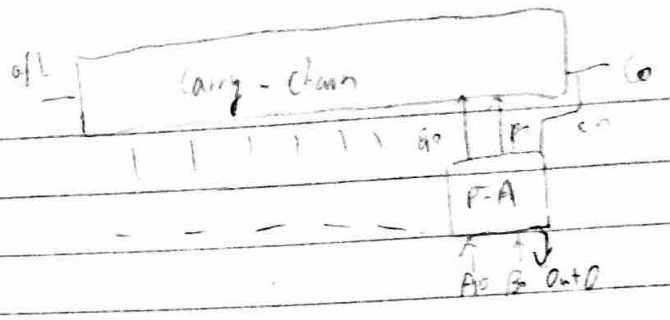




16bit ALU

Inputs: 16-bit A, B, Cin, 3-bit op, invA, invB, sign

Output: 16-out, ofl, zero



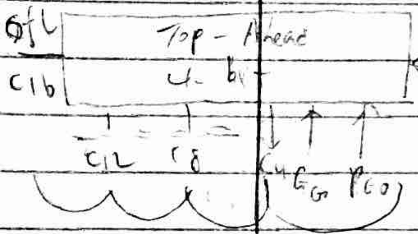
OpCode	Function
000	rll
001	sll
010	sra
011	srl
100	ADD
101	OR
110	XOR
111	AND

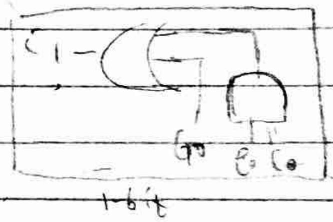
$C_1 = G_0 + P_0 \cdot C_0$

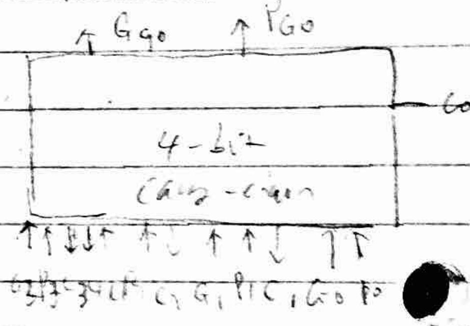
$C_2 = G_1 + P_1 \cdot C_1 = G_1 + P_1 \cdot G_0 + P_1 P_0 C_0$

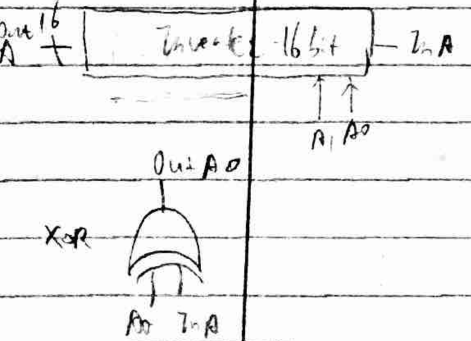
$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$







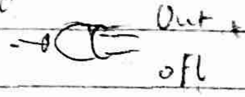


A0	InA	Out A0
1	1	0
0	1	1
1	0	1
0	0	0

Zero Detector:

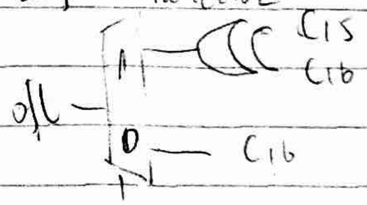
UB: $\rightarrow$ if ofl == 0

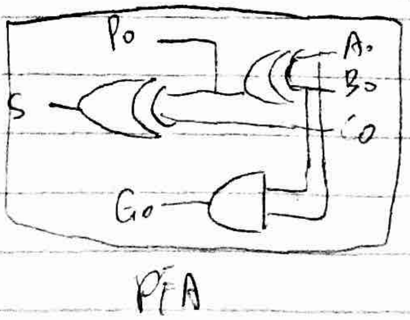
Out == 0



out	ofl	Z
0	1	0
0	0	1
1	0	0
1	1	0

Overflow Detector





PFA