Input
Read: R
Write: W
Hit (from cache): H
Valid (from cache): V
Dirty (from cache): D
Stall (from mem): S

Output
Done: D
Stall: S
Cache Hit: H

Output (to cache)
Enable: E
Comp: C
Write: W_c
Valid_in: V

Output (to mem)
Write: W_m
Read: R_m