2022 ICLAB fall

Syllabus

Instructor:

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Lecture Time:

- 3EF (13:30 ~ 15:30, Wednesday) @ ED415

Teaching Assistant:

name	ext	email	office
黃子芸	54238	hyty.c@nycu.edu.tw	ED430
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Prerequisites:

- Introduction to VLSI, Logic Design, Digital System Design, Computer Organization (Opt)

Course Objectives:

This course aims to convey to the senior and graduated EE students techniques to design the VLSI chips using state-of-the-art CAD tools. In addition to learning CAD tools for performance-driven and cost-effective IC designs, a top-down design flow and related environment will also be addressed. Upon completion of the course, the student will be able to design the integrated circuits and systems based on standard cell library as well as full-custom layout approaches. As such he/she will be able to work with a team of designers or stand-alone.

Course Schedule:

Week	Date	Course Content	TA
1	9/14	00、Introduction (VIM)、Environment	黃子芸
2	9/21	01、Verilog Combination Syntax	賴傳允
3	9/28	02、Verilog Sequential Syntax + generate	黃柏雅
4	10/5	03、Test Bench Programming Syntax	張晏榕
5	10/12	04、Sequential Logic Design II (Pipeline + Synopsys DesignWare IP)	張方睿
6	10/19	05、Memory & coding style	曹家輔
7	10/26	06、Design Compiler + IP Design with genvar	劉恆宇
8	11/2	(Special topic)	
8	11/05 (Sat.)	**Midterm Exam** **(Project deadline + Online Test)**	黃子芸
9	11/9	07、Synthesis　Static Time Analysis + Cross Clock Domain	張晏榕
10	11/16	08、Low Power Design	張方睿
11	11/23	09、System Verilog (Design)	張柏康
12	11/30	10、System Verilog II (Verification)	賴傳允
13	12/7	System Verilog (Formal Verification) (Bonus)	張柏康
14	12/14	11、APR I　: From RTL to GDSII	黃柏雅
15	12/21	12、APR II : IR-Drop Analysis	曹家輔
16	12/28	**Final Exam** **(Final project deadline)**	黃子芸

Grading Policy

Weekly Lab Exercise(5%)　x　12	**(60%)**
Midterm Project	**(10%)**
Midterm Exam	**(6%)**
Online Test	**(8%)**
Final Project	**(10%)**
Final Exam	**(6%)**
Bonus (Formal Verification)	**(5%)**