verilog代码层面关键信号检测报告

报告介绍：

本报告是关于在verilog代码层面对安全性进行检测的生成报告，对于verilog中命名的变量进行重要性排序，下列是代码中一位寄存器的重要性排序，并给出了他们所在的文件名,程序更改后代码另存于newverilog文件夹。

单位寄存器变量			
0	valid_wb_q	0.003039	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_pipe
1	mem_writeback_q	0.002121	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
2	mem_invalidate_q	0.001528	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
3	mem_flush_q	0.001528	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
4	mem_cacheable_q	0.000967	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
5	pc_fault_q	0.000473	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
6	load_fault_q	0.000473	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
7	store_fault_q	0.000473	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
8	mem_load_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
9	mem_xb_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
10	mem_xh_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
11	mem_ls_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_lsu.v
12	load_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
13	itlb_valid_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
14	lsu_out_cacheable_r	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
15	mem_req_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
16	src_mmu_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_mm
17	squash_e1_e2_q	0.00036	/Users/yunyingye/Desktop/desktop/pyqt/Pyverilog-develop/riscv_pipe