verilog代码层面关键信号检测报告

报告介绍：

本报告是关于在verilog代码层面对安全性进行检测的生成报告，对于verilog中命名的变量进行重要性排序，下列是代码中一位寄存器的重要性排序，并给出了他们所在的文件名,程序更改后代码另存于newverilog文件夹。

单位寄存器变量			
0	skid_valid_q	0.010184	riscv_fetch.v
1	div_busy_q	0.008134	riscv_divider.v
2	branch_q	0.007293	riscv_fetch.v
3	reset_q	0.005631	riscv_csr.v
4	branch_r	0.004407	riscv_exec.v
5	icache_fetch_q	0.004239	riscv_fetch.v
6	branch_d_q	0.003985	riscv_fetch.v
7	branch_taken_r	0.003639	riscv_exec.v
8	active_q	0.003557	riscv_fetch.v
9	branch_ret_r	0.003304	riscv_exec.v
10	set_r	0.003148	riscv_csr.v
11	clr_r	0.003148	riscv_csr.v
12	ifence_q	0.002705	riscv_csr.v
13	branch_taken_q	0.002705	riscv_exec.v
14	branch_ntaken_q	0.002705	riscv_exec.v
15	icache_invalidate_q	0.002705	riscv_fetch.v
16	branch_call_r	0.002697	riscv_exec.v
17	div_inst_q	0.002658	riscv_divider.v
18	csr_write_r	0.002603	riscv_csr.v
19	csr_fault_r	0.002598	riscv_csr.v
20	csr_mip_upd_q	0.00256	riscv_csr_regfile.v
21	m_enabled_r	0.002487	riscv_csr_regfile.v
22	csr_mtime_ie_r	0.00234	riscv_csr_regfile.v
23	s_enabled_r	0.002332	riscv_csr_regfile.v
24	invert_res_q	0.002262	riscv_divider.v
25	branch_r	0.002202	riscv_csr_regfile.v
26	branch_jmp_r	0.002202	riscv_exec.v
27	csr_readonly_r	0.002158	riscv_csr.v
28	csr_mtime_ie_q	0.002108	riscv_csr_regfile.v
29	rd_valid_e1_q	0.001866	riscv_csr.v
30	take_interrupt_q	0.001866	riscv_csr.v
31	tlb_flush_q	0.001866	riscv_csr.v
32	branch_q	0.001866	riscv_csr.v

33	valid_q	0.001866	riscv_divider.v
34	branch_call_q	0.001866	riscv_exec.v
35	branch_ret_q	0.001866	riscv_exec.v
36	branch_jmp_q	0.001866	riscv_exec.v
37	stall_q	0.001866	riscv_fetch.v