verilog代码层面关键信号检测报告

报告介绍：

本报告是关于在verilog代码层面对安全性进行检测的生成报告，对于verilog中命名的变量进行重要性排序，下列是代码中一位寄存器的重要性排序，并给出了他们所在的文件名,程序更改后代码另存于newverilog文件夹。

单位寄存器变量			
0	opcode_issue_r	0.010473	riscv_issue.v
1	mem_unaligned_e2_q	0.007152	riscv_lsu.v
2	take_interrupt_q	0.006587	riscv_csr.v
3	skid_valid_q	0.006347	riscv_fetch.v
4	mem_unaligned_e1_q	0.005935	riscv_lsu.v
5	mem_rd_q	0.005747	riscv_lsu.v
6	valid_q	0.005564	riscv_divider.v
7	pending_lsu_e2_q	0.005097	riscv_lsu.v
8	csr_pending_q	0.004364	riscv_issue.v
9	mem_writeback_q	0.004146	riscv_lsu.v
10	mem_invalidate_q	0.004146	riscv_lsu.v
11	mem_flush_q	0.004146	riscv_lsu.v
12	reset_q	0.004125	riscv_csr.v
13	squash_e1_e2_q	0.004009	riscv_pipe_ctrl.v
14	div_busy_q	0.003881	riscv_divider.v
15	branch_q	0.003866	riscv_csr.v
16	div_pending_q	0.003415	riscv_issue.v
17	opcode_accept_r	0.003394	riscv_issue.v
18	branch_q	0.003288	riscv_fetch.v
19	store_fault_q	0.003266	riscv_mmu.v
20	load_fault_q	0.003266	riscv_mmu.v
21	valid_e2_q	0.002574	riscv_pipe_ctrl.v
22	pc_fault_q	0.002069	riscv_mmu.v
23	branch_r	0.002007	riscv_exec.v
24	csr_wr_wb_q	0.001908	riscv_pipe_ctrl.v
25	icache_fetch_q	0.001802	riscv_fetch.v
26	branch_taken_r	0.001749	riscv_exec.v
27	store_fault_r	0.001659	riscv_mmu.v
28	branch_d_q	0.001655	riscv_fetch.v
29	load_fault_r	0.001653	riscv_mmu.v
30	dtlb_req_q	0.001555	riscv_mmu.v
31	active_q	0.001509	riscv_fetch.v
32	pc_fault_r	0.001501	riscv_mmu.v

33	mem_req_q	0.001375	riscv_mmu.v
34	mem_unaligned_r	0.001346	riscv_lsu.v
35	branch_r	0.001322	riscv_csr_regfile.v
36	read_hold_q	0.001143	riscv_mmu.v
37	src_mmu_q	0.001143	riscv_mmu.v
38	branch_ret_r	0.001109	riscv_exec.v
39	set_r	0.001089	riscv_csr.v
40	clr_r	0.001089	riscv_csr.v
41	ifence_q	0.001068	riscv_csr.v
42	icache_invalidate_q	0.001068	riscv_fetch.v
43	valid_wb_q	0.001021	riscv_pipe_ctrl.v
44	dtlb_valid_q	0.000995	riscv_mmu.v
45	mulhi_sel_e1_q	0.000989	riscv_multiplier.v
46	load_q	0.000977	riscv_mmu.v
47	branch_taken_q	0.000908	riscv_exec.v
48	branch_ntaken_q	0.000908	riscv_exec.v
49	branch_call_r	0.000905	riscv_exec.v
50	itlb_valid_q	0.000896	riscv_mmu.v
51	div_inst_q	0.000895	riscv_divider.v
52	csr_fault_r	0.000889	riscv_csr.v
53	csr_write_r	0.000885	riscv_csr.v
54	m_enabled_r	0.000872	riscv_csr_regfile.v
55	csr_mip_upd_q	0.000859	riscv_csr_regfile.v
56	tlb_flush_q	0.000859	riscv_csr.v
57	csr_wr_e2_q	0.000841	riscv_pipe_ctrl.v
58	mem_cacheable_q	0.00084	riscv_lsu.v
59	lsu_out_cacheable_r	0.00084	riscv_mmu.v
60	s_enabled_r	0.00082	riscv_csr_regfile.v
61	mem_load_q	0.000807	riscv_lsu.v
62	mem_xb_q	0.000807	riscv_lsu.v
63	mem_xh_q	0.000807	riscv_lsu.v
64	mem_ls_q	0.000807	riscv_lsu.v
65	mem_rd_r	0.000793	riscv_lsu.v
66	csr_mtime_ie_r	0.000785	riscv_csr_regfile.v
67	valid_e1_q	0.000781	riscv_pipe_ctrl.v
68	invert_res_q	0.000761	riscv_divider.v
69	load_byte_r	0.000739	riscv_lsu.v
70	load_half_r	0.000739	riscv_lsu.v

71	branch_jmp_r	0.000739	riscv_exec.v
72	csr_readonly_r	0.000726	riscv_csr.v
73	csr_mtime_ie_q	0.000707	riscv_csr_regfile.v
74	rd_valid_e1_q	0.000702	riscv_csr.v
75	load_signed_r	0.000702	riscv_lsu.v
76	branch_call_q	0.000626	riscv_exec.v
77	branch_ret_q	0.000626	riscv_exec.v
78	branch_jmp_q	0.000626	riscv_exec.v
79	stall_q	0.000626	riscv_fetch.v