2A) Rearranging the code statement

```
add $s2, $t2, $t3
add $t5, $s2, $t6
sub $t4, $s2, $t5
and $t5, $t4, $t6
```

2B)

```
add $s2, $t2, $t3
nop
nop
sub $t4, $s2, $t5
nop
add $t5, $s2, $t6
nop
nop
and $t5, $t4, $t6
```

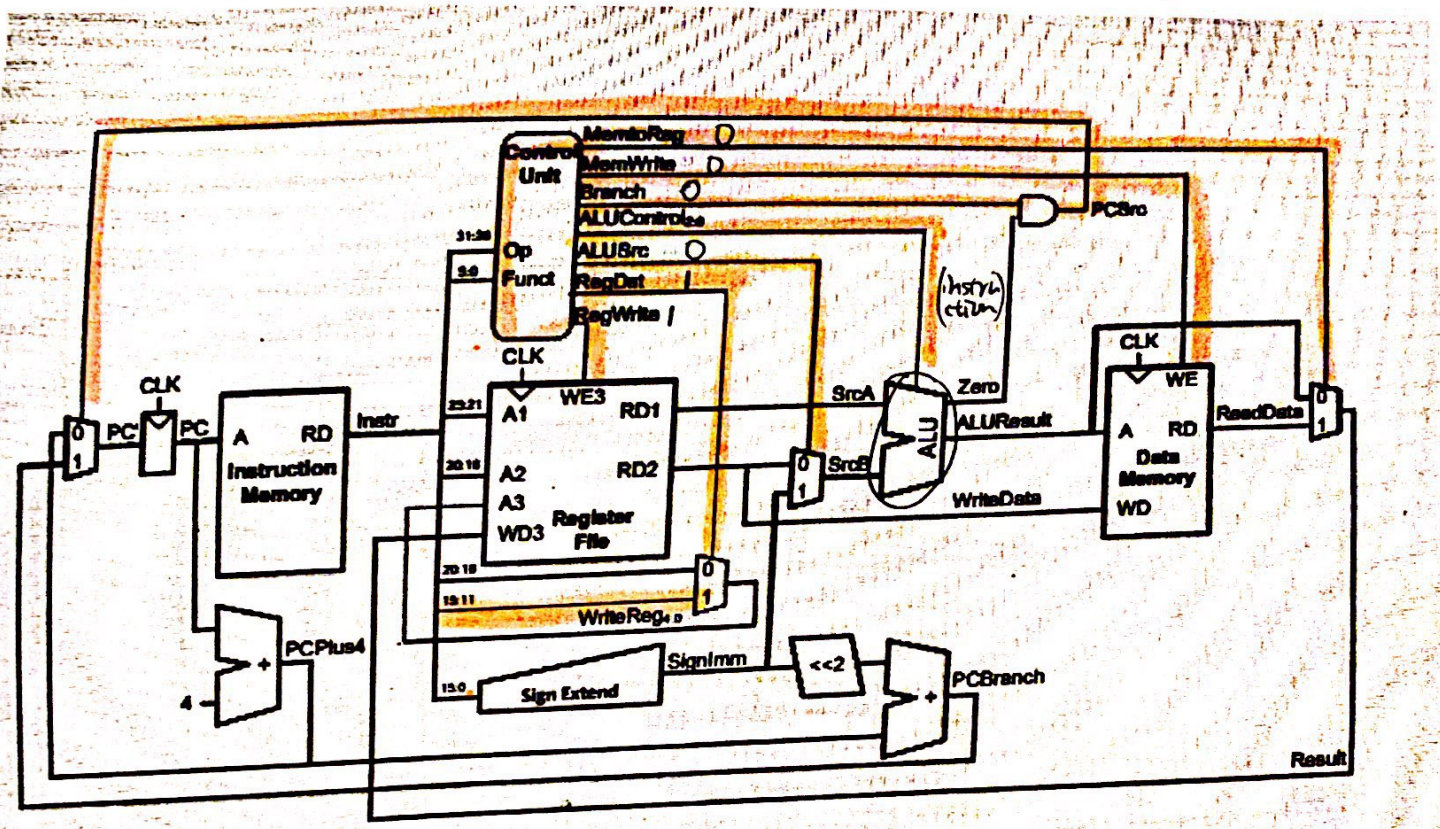
2C)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Instruction 1	F	D	X	M	W									
instruction 2		*	*	F	D	X	M	W						
instruction 3					*	F	D	X	M	W				
instruction 2							*	F	D	X	M	W		

2D)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
instruction 1	F	D	X	M	W									
Instruction 2		F	D	X	M	W								
Instruction 3			F	D	X	M	W							
instruction 2				F	D	X	M	W						

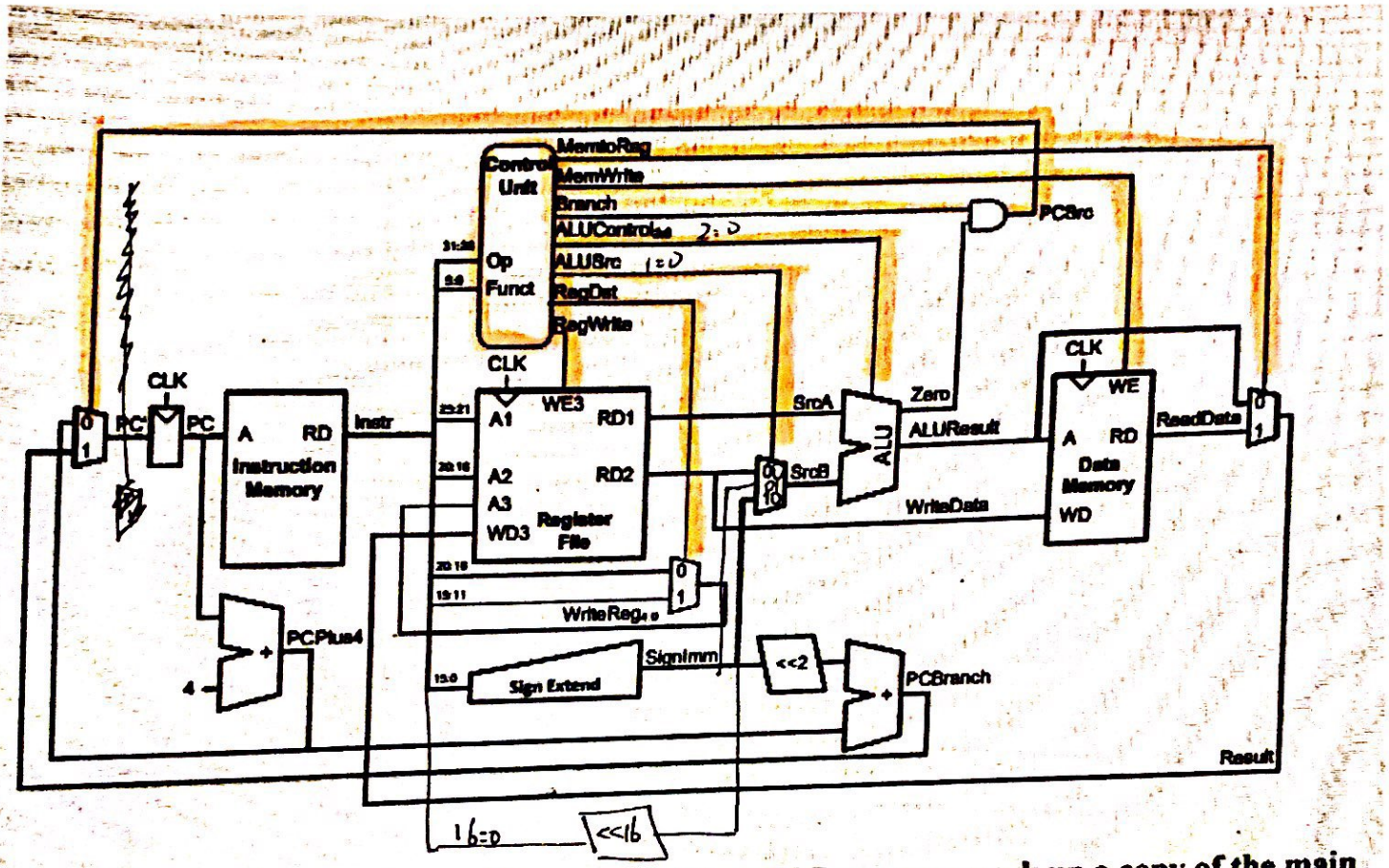
3A) sll



Similarly, for each of the instructions in 3A, 3B, and 3C you may mark up a copy of the main decoder truth table given below to show the changes to it.

Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp
R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	1	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01
sll	000110	1	0	1	0	0	0	11

3B) lui



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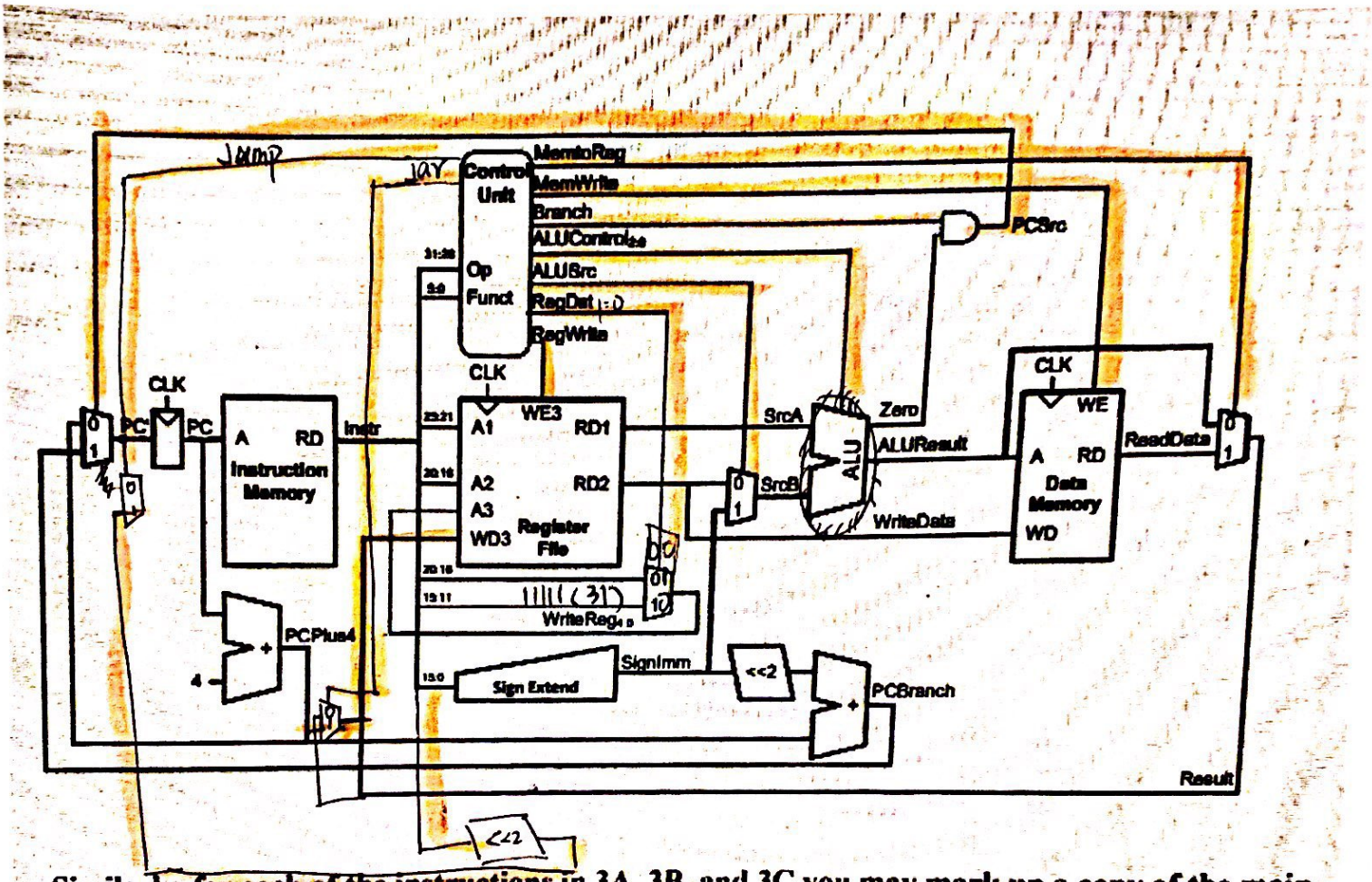
Instruction	Opcode	RegWrite	RegDst	ALUSrc	Branch	MemWrite	MemtoReg	ALUOp
R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	1	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01
lui	001111	1	0	1	0	0	0	00

3C) jal



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R-type	000000	1	1	0	0	0	0	10
lw	100011	1	0	1	0	0	1	00
sw	101011	0	X	1	0	1	X	00
beq	000100	0	X	0	1	0	X	01
jal	000011	1	10	X	X	0	X	X